Hierarchical Current Density Verification for Electromigration Analysis in Arbitrarily Shaped Metallization Patterns of Analog Circuits

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Abstract

Electromigration is caused by high current density stress in metallization patterns and is a major source of breakdown in electronic devices. It is therefore an important reliability issue to verify current densities within all stressed metallization patterns. In this paper we propose a new methodology for hierarchical verification of current densities in arbitrarily shaped analog circuit layouts, including a quasi-3D model to verify irregularities such as vias. Our approach incorporates thermal simulation data to account for the temperature dependency of electromigration. The described methodology, which can be integrated into any IC design flow as a design rule check (DRC), has been successfully tested and verified in commercial design flows.

1. Introduction

The term “electromigration” is applied to mass transport in metals when the metals are stressed at high current densities. This results in a change of conductor dimensions, thereby causing high resistive spots and eventual failure due to destruction of the conductor at this spot. Electromigration has been recognized as a potential wear-out failure mode in VLSI circuits employing metal layers of inadequate cross-sectional area.

The ongoing reduction of circuit feature sizes has especially aggravated the problem of electromigration in analog circuits. And yet, to the best of our knowledge there does not exist any commercial tool for electromigration analysis of arbitrarily shaped metallization patterns as commonly used in analog circuits. Since manual current density verification of complex analog circuits is extremely time consuming and error prone, we have developed an automatic verification methodology tailored especially for electromigration analysis of arbitrary metallization shapes in analog circuits.

The main contributions of our approach are:

- a new methodology for *hierarchical* verification of current densities in *arbitrarily* shaped analog circuit layouts,
- a quasi-3D model for verifying irregularities like vias and via edge stress, using “bee-comb”-like structures,
- a current-density verification method which incorporates thermal simulation data to account for temperature dependence of electromigration, and
- the option of integrating the proposed methodology as an automated current-density-DRC in virtually *any* IC-design flow.

2. Previous Works

The effect of electromigration and its relation to the mean time to failure (MTTF) of an electronic circuit has been extensively studied over the last three decades [4][5][19]. Despite the fact that the basic understanding of the failure mechanism has improved in recent years, many aspects are still not fully understood. A good summary of electromigration can be found in [12][15].

A closely linked topic is the relation between the current waveform and the estimated MTTF. Studies in [10][11] show an increased estimated lifetime for bi-directional and pulsed current stress compared to single direction current and constant current stress (due to the process of "self-healing"). The discussed “on-time-model,” based on root mean square (RMS) current, and “average-model,” based on average current, show a frequency dependence. The transition between these two models occurs at about 1 Hz, with the on-time-model having a better lifetime prediction quality below 1 Hz [11]. Furthermore, the use of RMS current values represents the more conservative approach and hence is the preferred model for critical applications.

Two electromigration analysis systems which are limited to the verification of *digital* designs have been presented [6][16]. Hajj et al. [6] reported a CAD system for electromigration analysis based on current density investigation for relatively simply shaped layout patterns in CMOS circuits. The approach divides the layout structure into several simple shapes which are combined in an RC-network. Each element of the network is then simulated independently. In 1997 Simplex Solutions [16] introduced ”Thunder & Lightning,” a commercial tool set for electromigration analysis of power and ground networks as well as for digital signal nets.

To the best of our knowledge, only one current-density simulator for *analog* applications has been published [1]. It decomposes all wires into rectangles and irregularities. The resistance of the rectangles is calculated and then used to extract a netlist which incorporates references to the corresponding geometrical dimensions. Irregularities with inhomogeneous current distribution such as wire bends, pins and vias cannot be validated with the proposed algorithm.

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3. Current Density Verification Flow

3.1 Overview

The current density verification flow of our approach is illustrated in Figure 1.

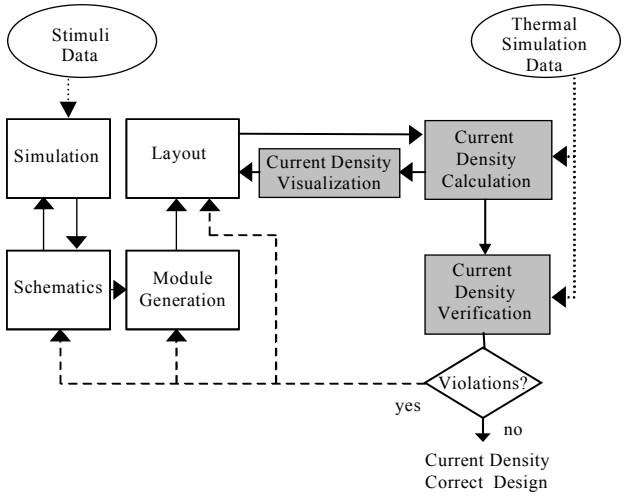

Figure 1: Our current density verification flow

Each cell within a hierarchical design has to be simulated in order to verify its specification (Section 3.2). The simulation stimuli should include the entire range of possible input values, including worst case conditions. The simulation results in a set of post-processed current values which are attached to the cell pins (Section 3.3).

Based on the processed simulation data, a module generator creates a layout representation of the schematic devices. During the subsequent layout step placement and routing is performed. Current-critical nets are routed with a width derived from the expected currents.

Both the layout geometry of a completed net and process relevant data are transferred to a *current density calculation* tool which calculates the current density within each layout element such as paths, vias and via arrays (Sections 4.1, 4.2). The results can be visualized in the layout tool (*current density visualization,* Section 4.3) or can be further used to perform *current density verification* (Section 4.4).

Invoking current density verification, current density-related violations are detected by using a set of defined current density design rules. Depending on the type of violation, the verification results are returned (1) to the layout step (e.g., if encountering paths with insufficient widths), (2) to the module generator (e.g., if pins cannot carry the attached currents) or (3) to the schematic entry (e.g., if a cell in another hierarchy must be changed).

Both current density calculation and verification can make use of thermal simulation data in order to detect possible electromigration problems near heat sources, such as output-stage transistors.

3.2 Verification of Hierarchical Cells

An important aspect of hierarchical design is the necessity of *independent* testability of hierarchical elements. The pin current values of a cell interface are attached as cell port properties. In the next higher hierarchy level, these values are visible as instance pin properties. In order to allow an independent verification of cells in different hierarchies, current values at the cell interfaces have to obey the following rule (Figure 2):

The equivalent current value $|I_{Pi}|$ attached to a cell port P_i has to be equal or greater than the equivalent current value $|I_{Qj}|$ attached to the derived instance pin Q_j of the cell in the next higher hierarchy level.

The *equivalent current value* depends on the lifetime estimation model used. It represents the RMS-current value for the on-time-model or the average current for the average-model [11][12][15].

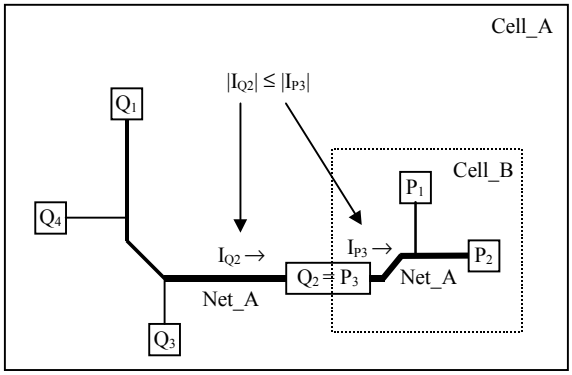

Figure 2: Routed in two cells in different hierarchies, net Net_A is separated into subnet Cell_A:Net_A and Cell_B:Net_A. In order to verify the subnet in Cell_B independently of the subnet in cell Cell_A, the "higher level" pin current $|I_{Q2}|$ must not exceed the assumed "lower level" pin current $|I_{P3}|$.

3.3 Representation of Pin Currents

We use a standard circuit simulator for simulation of the circuit netlist, where parasitic wiring resistances are neglected. The results from one or more simulations are post-processed by calculating a set of pin current values satisfying Kirchhoff's current laws at particular points of time. Specifically, they represent a snapshot of the circuits operation at the time of minimum and maximum currents at each pin. This reduces the simulation results to a set of "worst case" current values. For a net with *n* pins this may lead to up to *2n* current values to be stored. Hence, up to 2*n* current values are attached to each pin.

4. Calculation, Visualization and Verification of Current Densities

Common approaches to the current density calculation include the Finite Element Method (FEM) [2][8][17], the Boundary Element Method (BEM) [8] and the Finite Difference Method (FDM). Our current density calculation utilizes the well known Finite Element Method due to its excellent ability to handle arbitrarily shaped layout geometry and its ability to deliver fairly good approximations even for calculations with lower resolution.

Since the wire width of interconnects carrying high current always exceeds the layer thickness by at least a

factor of 2, current flow in common layout structures can be considered as a two-dimensional problem.

Any current density calculation method requires at minimum (1) a set of current values as boundary constraints, (2) an appropriate representation of the layout geometry, (3) technology dependent data (e.g., layer thickness), and (4) specified application data (e.g., average chip temperature or a temperature field plot).

Additionally, the verification step needs information about technology dependent restrictions on the maximum permitted steady current density in each layer. To improve the prediction quality of the verification, a plot of thermal simulation data can be used to account for temperature gradients near significant heat sources, which can further expedite the material migration process due to thermal migration.

4.1 Geometry Extraction

In order to apply the Finite Element Method (FEM) it is necessary to split the original layout net into smaller "pieces," so called finite elements. The use of triangles ensures a good matching of arbitrary layout geometry, including holes and circles and other "oddly shaped" geometrical patterns.

We used the Delaunay triangulation [9] with Ruppert's Delaunay refinement algorithm [13] to create a triangle mesh. Figure 3 (a) depicts a regular triangulation mesh of a layout structure. The smallest possible mesh size is applied around corners to account for increased current density at corners within the current flow (Figure 3 (b)). The mesh size in all other areas is derived from a user-controlled magnification factor k and the size of the polygon region. This variable mesh adjustment allows a good compromise between solution quality and calculation time.

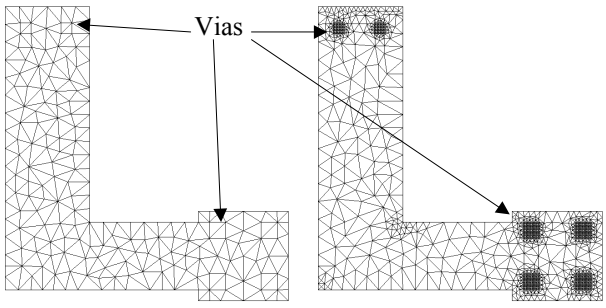

Figure 3: Generated mesh for a layout structure (a), refined mesh around corners and within vias (b)

We introduce a three-dimensional "bee-comb"-like structure of triangles to be able to model asymmetric current density stress within contact and via structures (Figure 4). Two "modes" are possible: A low resolution mode of the via structure permits the check of the via's capability to carry a given current (i.e., to check if the cross-section area of the via is sufficiently large). Via edge stress is additionally detectable with higher resolution (examples in Sections 5.1, 5.3).

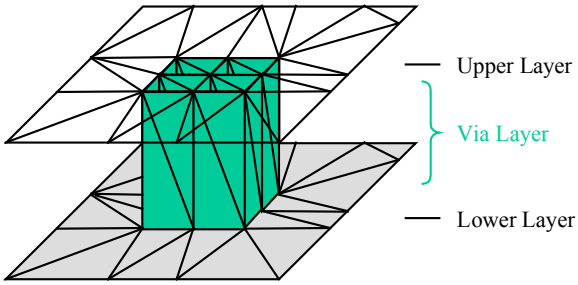

Figure 4: Via modeled in a quasi-3D model similar to a "bee-comb" structure

4.2 Calculation of Current Densities

Based on Maxwell's equations for both conducting and homogeneous materials, the Laplacian equation

$$\Delta\varphi = \frac{\partial^2\varphi}{\partial x^2} + \frac{\partial^2\varphi}{\partial y^2} + \frac{\partial^2\varphi}{\partial z^2} = 0 \quad \text{in } \boldsymbol{G} \qquad (1)$$

has to be solved (1) in the field $\boldsymbol{G}$ ($G \in R^3$) and (2) within the given current boundary constraints from the pins (with φ representing the voltage potential and x,y,z denoting the coordinates in $\mathbf{R}^3$). Since we consider current flow as a two-dimensional problem, the z-related third term can be omitted. Hence, Equation (1) can be rewritten as a mathematical variation problem which can be solved by the Finite Element Method.

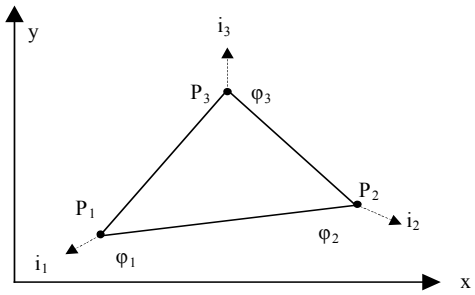

Figure 5: Representation of a finite element using a triangle (φ voltage potentials, i currents, P mesh nodes)

Due to the linear relation between voltage and current in a conductor, a suitable linear assumption for a single triangle can be made (Figure 5):

$$\varphi = a_0 + a_1 x + a_2 y \ . \qquad (2)$$

The determination of the integral parts of a single triangle within the above mentioned mathematical variation problem (derived from Equation (1)) leads to the coefficients a_0, a_1 and a_2:

$$\begin{bmatrix} a_0 \\ a_1 \\ a_2 \end{bmatrix} = \frac{1}{S} \begin{bmatrix} x_2y_3 - x_3y_2 & x_3y_1 - x_1y_3 & x_1y_2 - x_2y_1 \\ y_2 - y_3 & y_3 - y_1 & y_1 - y_2 \\ x_3 - x_2 & x_1 - x_3 & x_2 - x_1 \end{bmatrix} \cdot \begin{bmatrix} \varphi_1 \\ \varphi_2 \\ \varphi_3 \end{bmatrix} \qquad (3)$$

where φ_1, φ_2, φ_3 denote the voltage potential at the mesh nodes P_1, P_2 and P_3, and S denotes the determinant of the transformed triangles Jacobi matrix (with S representing twice the triangle area size).

Derived from the known definition of the current density $|\underline{J}| = di/dA$ we obtain:

$$i = \int_A |\underline{J}| \cdot dA \tag{4}$$

with i denoting the current and A representing the area. Current density is also given by Maxwell's equation:

$$\underline{J} = \frac{1}{\rho}\left(\frac{\partial\varphi}{\partial x}, \frac{\partial\varphi}{\partial y}, \frac{\partial\varphi}{\partial z}\right)^{\mathbf{T}} \tag{5}$$

which can be rewritten as:

$$\underline{J} = \frac{1}{R'_{SQ}(T,x,y)\cdot d}(a_1, a_2, 0)^{\mathbf{T}} \tag{6}$$

with $R'_{SQ}(T,x,y)$ representing the effective sheet resistance at temperature T at a specific mesh node (x,y) and d denoting the layer thickness. The absolute value $|\underline{J}|$ of the current density $\underline{J}$ is given by

$$|\underline{J}| = \frac{1}{R'_{SQ}(T,x,y)\cdot d} \cdot \sqrt{a_1^2 + a_2^2}\ . \tag{7}$$

This leads to the triangle *element equations:*

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \frac{1}{k}\begin{bmatrix} -c_1c_1 - d_1d_1 & c_2c_1 + d_2d_1 & c_3c_1 + d_3d_1 \\ c_1c_2 + d_1d_2 & -c_2c_2 - d_2d_2 & -c_3c_2 - d_3d_2 \\ c_1c_3 + d_1d_3 & -c_2c_3 - d_2d_3 & -c_3c_3 - d_3d_3 \end{bmatrix} \cdot \begin{bmatrix} \varphi_1 \\ \varphi_2 \\ \varphi_3 \end{bmatrix} \tag{8}$$

with $k = 2 * S * R'_{SQ}(T,x,y) * d$ and

$$\underline{c} = (y_3 - y_2, y_3 - y_1, y_1 - y_2)^{\mathbf{T}} \quad \text{and}$$

$$\underline{d} = (x_3 - x_2, x_3 - x_1, x_1 - x_2)^{\mathbf{T}}. \tag{9}$$

The element equations of all triangles have to be assembled to the *system matrix*

$$\underline{i} = \underline{Y} \cdot \underline{\varphi} \tag{10}$$

where $\underline{\mathbf{Y}}$ denotes the sparse, diagonal dominant and positive definite conductance matrix. In order to solve Equation (10), the boundary constraints must be applied:

$$\underline{i_{BC}} = \underline{Y} \cdot \underline{E^{BC}} \cdot \underline{\varphi}\ . \tag{11}$$

$\underline{\mathbf{E}}^{\mathbf{BC}}$ is an altered unitary matrix $\underline{\mathbf{E}}$ with all bulk node elements set to 0. $\underline{i_{BC}}$ contains all current boundary constraint values of the constrained mesh nodes n (and 0 otherwise). A current share i_n of

$$i_n = \frac{i_{constr}}{m}, \tag{12}$$

is applied to each single mesh node n of a given current constraint i_{constr} (with m representing the number of FEM mesh nodes assigned to this current boundary constraint).

Finally, the equation system (11) can be solved with an iterative equation solving method. We utilize the conjugate gradient method [3][14] with preconditioning. This method guarantees robustness and a good convergence behavior for our applications.

The described algorithm does not account for self-heating within wire segments. Results from practical experiments and theoretical research [7] have shown no significant temperature rise for usually applicable current densities up to 2mA/µm. Therefore we assume no significant self-induced temperature gradients which may influence the material migration process.

4.3 Visualization of Current Densities and Voltage Potentials

The resulting solution vector $\underline{\varphi}$ from Equation (11) can be used to visualize either the progression of the current density or the voltage potential. Each current density value or voltage potential value is translated into a color using a predefined set of visualization colors.

The current density view helps to identify inadequate cross-sectional layout structures, such as wires, vias and via arrays. The voltage potential view enables the detection of mismatched nets that have matching requirements, such as connections to differential pairs of transistors. Additionally, the voltage offset and resistance between two arbitrary points as well as IR-drop can be retrieved from the data set.

4.4 Verification of Current Densities

The simple visualization of current densities and voltage potentials is not sufficient in order to be used as a commercial current density verification method. A verification method must also take temperature, characteristics of the process, and the combination of the materials into account and relate it with the current density that has been measured. For example, different metallization materials in a given process technology may have different restrictions on their permitted permanent current densities.

Hence, we need to correlate a measured current density with temperature and material characteristics in order to determine if an actual current density violation occurs. Based on Black's law [4] and the requirement of equal lifetimes for wires (MTTF(T) = MTTF(T_{ref})) which are exposed to a temperature $T \neq T_{ref}$, we derived Equation (13). It determines the relation between an acceptable current density $J_{max}(T)$ at an actual temperature T and a material-dependent maximum current density $J_{max}(T_{ref})$ at a given reference temperature T_{ref}, respectively:

$$|\underline{J}_{\max}(T)| \le |\underline{J}_{\max}(T_{ref})| \cdot \exp\left(-\frac{Q}{n \cdot k \cdot T_{ref}}\left(1 - \frac{T_{ref}}{T}\right)\right) \tag{13}$$

(With Q denoting the experimentally determined activation energy for electromigration failure mechanism ($Q \approx$ 0.5 .. 1.4 eV), n set to 2 according to Black's law [4], k denoting the Boltzmann's constant (k=1.38e-23 J/K), T_{ref} denoting the reference temperature (usually T=150°C) and T representing the actual maximum working temperature.)

In order to enable an efficient current density verification methodology for an arbitrary net structure, we perform a layout segmentation of the net. This segmentation step translates the layout structure into a segment tree with the end points of each segment representing either a pin or a Steiner point. The worst case current values for each segment are derived from the current values attached to the pins. The current values for Steiner points are determined by propagating current values within the segment tree with regard to Kirchhoff's current law.

Each net segment is transferred to the Current-Density-Calculator and the simulation result is verified according to the given set of design rules.

Nets with internal loops cannot be verified with this methodology. They have to be filtered out prior to the current density verification step and verified as complete layout structure without layout segmentation.

An appropriate parameterized filter within the current density verification tool separates intrinsically increased current density spots around corners from "real" design rule violations.

The verification results are written to a standardized DRC file format which can be used within most commercial DRC result browsers.

5. Implementation and Results

The described algorithms have been implemented in about 50,000 lines of C++ code.

An ASCII-based interface reads in layout data (including pin current values) from virtually any layout tool and returns graphical and digital data to the layout tool. Our verification method has been extensively tested in commercial analog designs of various sizes.

The benchmarks reported here were performed on a Sun-Ultra10 workstation with 440 MHz. Since commercial tools for current verification in arbitrarily shaped metallization patterns do not exist, we compare our automatic methodology with a conventional current density verification method requiring manual model preparation and subsequent current density calculation (using ANSYS version 5.7 [18]). Table 1 shows some results. The examples (Net_1 and Heater) are described in more detail in Sections 5.1 and 5.3, respectively.

Table 1: Comparison of our current density verification approach (labeled CDV) with a conventional method based on ANSYS

	FEM nodes	Verification time [sec]	Model preparation time [min]	Memory usage [MBytes]
Net_1 (CDV) [1]	4122	2.1	none	2.5
Net_1 (ANSYS) [1,2]	*2889*	*2.0*	*10*	*3.75*
Net_1 (CDV) [3]	4856	3.5	none	1.2
Net_1 (CDV-M) [3]	4856	1.9	none	1.9
Net_1 (ANSYS) [2,3]	*5x2889*	*5x2.0*	*10*	*3.75*
Heater (CDV)	5241	3.4	none	3.8
Heater (ANSYS)[2]	*3376*	*3.3*	*10*	*4.2*

[1] – Check of one current value at each pin
[2] – Usage of ANSYS shell element 157 and the Frontal Solver
[3] – Check of entire set of pin current values (use segmentation for CDV)
CDV-M – Multiprocessor option (2xCPU Sun-Ultra60-450)

The use of multiprocessor systems including clusters of workstations supports a time efficient full chip verification of commercial analog circuits. For example, typical verification times for commercial analog and mixed signal circuits (20,000 to 60,000 devices) range from 30 to 120 minutes.

5.1 Example of a Net with Via Arrays

Figure 6 depicts an *excerpt* of Net_1 (Table 1) laid out in three metallization layers. The current density in layer Metal_1 as well as within a tongue in layer Metal_2 violates current density constraints. The zoomed view of layer Metal_1 shows increased current density stress at the edges of the Metal_1 to Metal_2 vias, indicating a via array with an inappropriate layout.

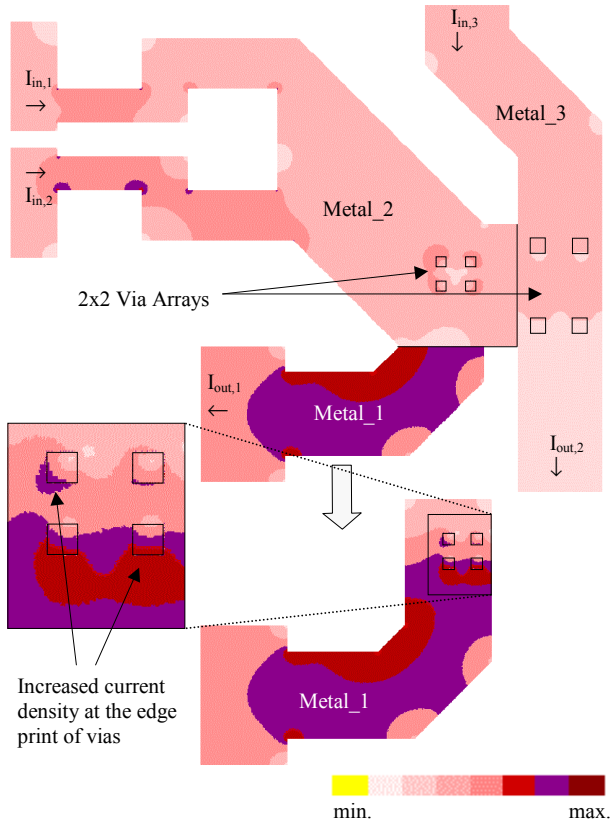

Figure 6: Excerpt from current density visualization of a net covering three layers. Current density design rule violations (darker colors) are visible in layer Metal_1 and at corners of the Metal_2 shape. The enlarged view of the Metal_1 shape shows the current density stress print of the via edges in the 2x2 via array.

5.2 Different Corner Bend Angles

Any corner is a natural obstacle for a current flow. Electrons follow the least resistance path and hence are "jammed" close to a corner leading to a high current density at this point. Figure 7 shows a current density simulation of different bend angles (90, 135, 150 degree) indicating the need for avoiding 90-degree corners in layout structures with higher currents.

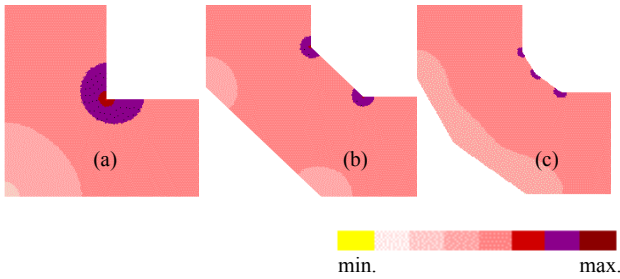

Figure 7: Current density simulation of different corner bend angles (a) 90 degree, (b) 135 degree, (c) 150 degree

5.3 Via Example

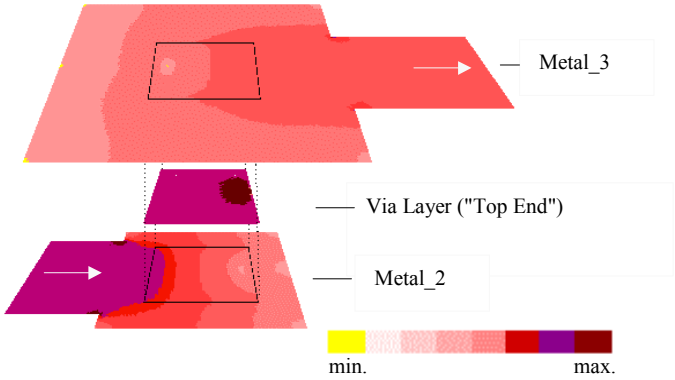

Figure 8: Quasi-3D current density distribution in a Metal_2 to Metal_3 via driven by an interconnect with increased current density. Please note that the via layer can be analyzed at both the top and the bottom end. In this example, the top surface of the via layer (adjacent to Metal_3) is depicted, showing an excessive current density on the side of the outgoing current.

5.4 A Heater Structure of a Sensor

In addition to current density verification of on-chip interconnects, the developed verification tool can also be used for "non-IC" applications with arbitrarily shaped metallization patterns, such as various MEMS structures. A heater structure ("Heater" in Table 1) as part of a sensor device is depicted in Figure 9. Increased current density stress is clearly visible at the inner edges of the ring elements.

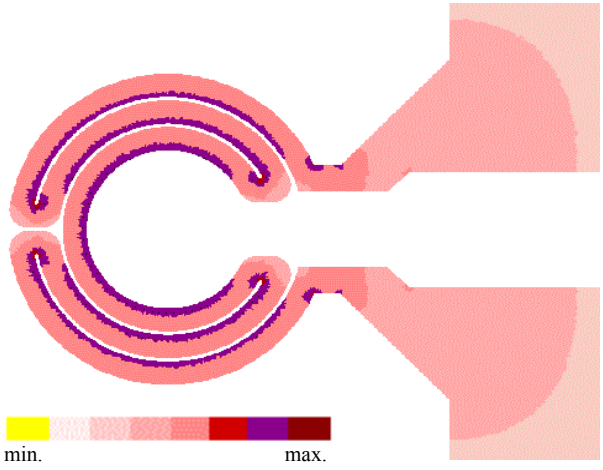

Figure 9: Part of a sensor heater structure with an increased current density at the inner edges of the ring elements.

6. Conclusion

We presented a new current density verification method which has been developed in order to cope with the steadily increasing problems of high current density stress in modern analog circuits. Our methodology allows an automatic, time-efficient verification of current densities in arbitrarily shaped layouts. The presented methodology has been verified in commercial design flows thereby leading to significantly shorter development times in combination with more reliable electronic devices.

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