Invited Talk: Introduction to Electromigration-Aware Physical Design

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ABSTRACT
Electromigration is increasingly relevant to the physical design of electronic circuits. It is caused by excessive current density stress in the interconnect. The ongoing reduction of circuit feature sizes has aggravated the problem over the last couple of years. It is therefore an important reliability issue to consider electromigration-related design parameters during physical design. In this talk, we give an introduction to the electromigration problem and its relationship to current density. We then present various physical design constraints that affect electromigration. Finally, we introduce components of an electromigration-aware physical design flow.

Categories and Subject Descriptors
B7.2[**Integrated Circuits**]: Design Aids

General Terms
Algorithms, Design, Verification.

Keywords
Electromigration, current density, physical design, layout, interconnect, interconnect reliability

1. INTRODUCTION

The reliability of an electronic system is a central concern for developers. This concern is addressed by a variety of design measures, for example the choice of materials that are suitable for the intended applications. As the structural dimensions of electronic interconnects become ever-smaller, new factors come to bear, which reduce reliability and which previously were negligible. In particular, there are material migration processes in electrical wires, which cannot be ignored anymore during the development of electronic circuits.

"Material migration" is a general term for various forced material transport processes in solid bodies. These include (1) chemical diffusion due to concentration gradients, (2) material migration caused by temperature gradients, (3) material migration caused by mechanical stress, and (4) material migration caused by an electrical field. This last case is often referred to as "electromigration", which is the subject of this talk.

The copper or aluminum interconnects of an electronic circuit are polycrystalline, that is, they consist of grains containing crystal lattices of identical construction but different orientation. As current flows through such a wire, there is interaction between the moving electrons – a sort of "electron wind" – and the metal ions in these lattice structures. Atoms at the grain boundaries especially will fall victim to the electron wind, that is, they will be forced to move in the direction of the flow of electrons. Thus, in time, copper or aluminum atoms will accumulate at individual grain boundaries, forming so-called "hillocks" in the direction of the current. At the same time, so-called "voids" can appear at the grain boundaries (Figure 1). While the hillocks can short-connect adjacent interconnects, the voids reduce the current flow in particular locations until the point of interconnect failure.

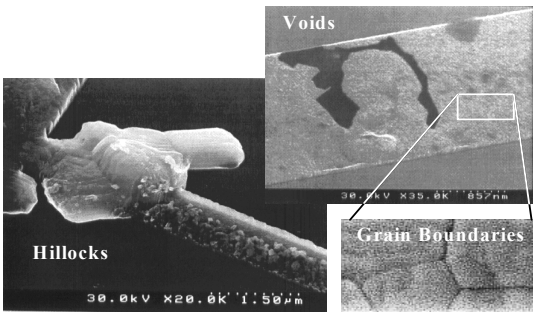

Figure 1. Hillock and void formations in wires due to electromigration (Photo courtesy of G. H. Bernstein und R. Frankovic, University of Notre Dame)

Many electronic interconnects, for example in integrated circuits, have an intended MTTF (mean time to failure) of at least 10 years. The failure of a single interconnect caused by electromigration can result in the failure of the entire circuit. At the end of the 1960s the physicist J. R. Black developed an empirical model to estimate the MTTF of a wire, taking electromigration into consideration [1]:

$$MTTF = \frac{A}{J^n} \cdot \exp\left(\frac{E_a}{k \cdot T}\right) \quad (1)$$

This is a minor revision of the work published in the proceedings of SLIP'05, pp. 81-88,
http://doi.acm.org/10.1145/1053355.1053374.

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where A is a constant based on the cross-sectional area of the interconnect, J is the current density, E_a is the activation energy (e.g. 0.7 eV for grain boundary diffusion in aluminum), k is the Boltzmann constant, T is the temperature and n a scaling factor (usually set to 2 according to Black [1]). It is clear that current density J and (less so) the temperature T are deciding factors in the design process that affect electromigration.

This talk concentrates on the possibilities during physical design of manipulating current density in order to obviate the negative effects of electromigration on the reliability of electronic interconnects. We will first explain the physical causes of electromigration, and then introduce ways of influencing current density during the physical design of an electronic circuit. Although the observations mainly concern analog circuits or power supply lines in digital circuits, they are also of relevance for most of today's digital designs.

2. THE ELECTROMIGRATION PROCESS

Current flow through a conductor produces two forces to which the individual metal ions in the conductor are exposed. The first is an electrostatic force F_{field} caused by the electric field strength in the metallic interconnect. Since the positive metal ions are to some extent shielded by the negative electrons in the conductor, this force can be ignored in most cases. The second force F_{wind} is generated by the momentum transfer between conduction electrons and metal ions in the crystal lattice. This force works in the direction of the current flow and is the main cause of electromigration.

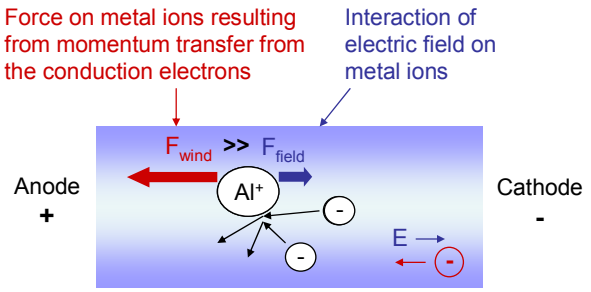

Figure 2. Two forces are acting on metal ions which make up the lattice of the interconnect material. Electromigration is the result of the dominant force, i.e. the momentum transfer from the electrons which move in the applied electric field.

In a homogeneous crystalline structure, because of the uniform lattice structure of the metal ions, there is hardly any momentum transfer between the conduction electrons and the metal ions. However, this symmetry does not exist at the grain boundaries and material interfaces, and so here momentum is transferred much more vigorously from the conductor electrons to the metal ions. Since the metal ions in these regions are bonded much more weakly than in a regular crystal lattice, once the electron wind has reached a certain strength, atoms become separated from the grain boundaries and are transported in the direction of the current. This direction is also influenced by the grain boundary itself, because atoms tend to move along grain boundaries.

If the current direction of an excessive current is kept constant over an extended period of time, voids and hillocks appear in the wire. For this reason, analog circuits or power supply lines in digital circuits are particularly susceptible to the effects of electromigration. When the current direction varies, for example in digital circuits with their alternating capacitive charging and discharging in conductors, there is a certain amount of compensation due to a material flow back (self-healing effect). Nonetheless, interconnect failures are still possible, with thermal migration playing a major role.

Furthermore, the susceptibility of wires to electromigration depends on grain size and thus on the distribution of grain sizes. Smaller grains encourage material transport, because there are more transport channels than in coarse-grained material. The result of this is that voids tend to appear at the points of transition from coarse to fine grains, since at these points atoms flow out faster than they flow in. Conversely, where the structure turns from fine grains to coarse, hillocks tend to form, since the inflowing atoms cannot disperse fast enough through the coarse structure.

These sorts of variations in grain size appear in interconnects at every contact hole or via. Because the current here commonly encounters a narrowing of the conductive pathway, contact holes and vias are particularly susceptible to electromigration.

Diffusion processes caused by electromigration can be divided into grain boundary diffusion, bulk diffusion and surface diffusion (Figure 3). In general, grain boundary diffusion is the major migration process in aluminum wires [5][7], whereas surface diffusion is dominant in copper interconnects [4][6][8][9].

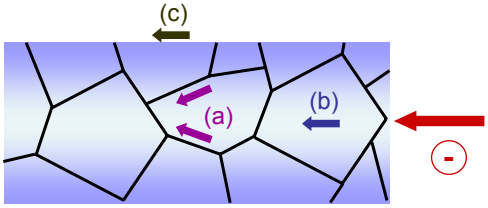

Figure 3. Illustration of various diffusion processes within the lattice of an interconnect: (a) grain boundary diffusion, (b) bulk diffusion, and (c) surface diffusion.

Detailed investigations of the various failure mechanisms of electromigration can be found in [2] - [5].

3. DESIGN CONSTRAINTS AFFECTING ELECTROMIGRATION

3.1 Wire Material

It is known that pure copper used for Cu-metallization is more electromigration-robust than aluminum. Copper wires can withstand approximately five times more current density than aluminum wires while assuming similar reliability requirements. This is mainly due to the higher electromigration activation energy levels of copper caused by its superior electrical and thermal conductivity as well as its higher melting point [4][6]. Alternatively, the Al-metallization material can be alloyed with small amounts of copper and silicon (AlSiCu) in order to reduce

the migration effect by increasing its electromigration activation energy as well [5][7].

Furthermore, a good selection and deposition of the passivation over the metal interconnect reduces electromigration damage by limiting extrusions and suppressing surface diffusion.

3.2 Wire Temperature

In Equation (1), the temperature of the conductor appears in the exponent, i.e. it strongly affects the MTTF of the interconnect. The temperature of the interconnect is mainly a result of the chip environment temperature, the self-heating effect of the current flow, the heat of the neighboring interconnects or transistors, and the thermal conductivity of the surrounding materials.

The following example demonstrates the significance of thermal conductivity: While conventional household copper wires would melt at current densities of over 10^4 A/cm^2, a silicon chip can tolerate current densities up to 10^{10} A/cm^2 without the wire melting [10]. What is responsible for this is the significantly higher thermal conductivity of the silicon substrate. (So the limiting factor in chip wiring is no longer the melting point, but the occurrence of electromigration.)

There is a further, often overlooked connection between the temperature of a conductor and the current density: In Equation (1), the temperature T is on the same side as current density J. For an interconnect to remain reliable in rising temperatures, the maximum tolerable current density of the conductor must necessarily decrease.

Figure 4 shows the relationship between maximum current density and temperature, as demonstrated by the constant reliability of the aluminum wiring in Equation (1). It becomes clear, that for example when the working temperature of an interconnect is raised from 25ºC (77ºF) to 125ºC (257ºF), the maximum tolerable current density is reduced by about 90%.

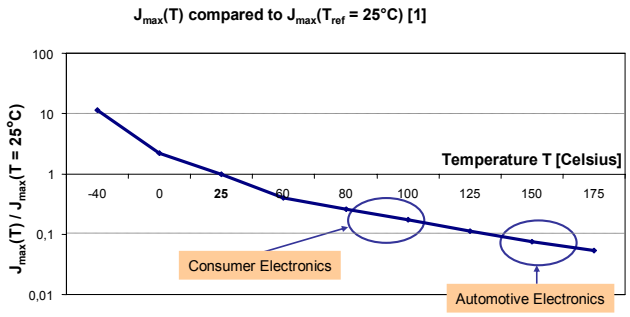

Figure 4. The maximum permissible current density of an aluminum metallization, calculated at e.g. 25°C, is reduced significantly when the temperature of the interconnect rises.

3.3 Wire Size and Metal Slotting

As Equation (1) shows, apart from the temperature, it is the current density that constitutes the main parameter affecting the MTTF of a wire. Since the current density is obtained as the ratio of current I and cross-sectional area A, and since most process technologies assume a constant thickness of the printed interconnects, it is the wire width that exerts a direct influence on current density: The wider the wire, the smaller the current density and the greater the resistance to electromigration.

However, there is an exception to this accepted wisdom: If you reduce wire width to below the average grain size of the wire material, the resistance to electromigration increases, despite an increase in current density. This apparent contradiction is caused by the position of the grain boundaries, which in such narrow wires as in a bamboo structure lie perpendicular to the width of the whole wire (Figure 5). As we have already mentioned, material transport occurs as much in the direction of the current flow as along the grain boundaries (so-called grain boundary diffusion). Because the grain boundaries in this type of bamboo structure are at right angles to the current flow, the boundary diffusion factor is excluded, and material transport is correspondingly reduced.

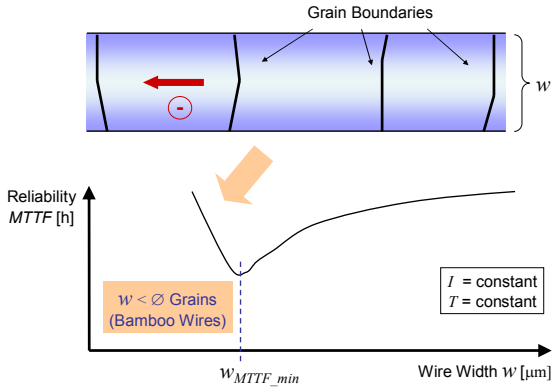

Figure 5. Reduced wire width below the average grain size increases the reliability of the wire with regard to electromigration. So-called bamboo wires are characterized by grain boundaries which lie perpendicular to the direction of the electron wind and thus permit only limited grain boundary diffusion.

So the bamboo structure increases reliability, and in order to exploit this, wire widths are deliberately kept so narrow that a bamboo structure is maintained; also, the wire material can be selectively annealed during IC processing in order to support bamboo formation.

However, the maximum wire width possible for a bamboo structure is usually too narrow for signal lines of large-magnitude currents in analog circuits or for power supply lines. In these circumstances, slotted wires are often used, whereby rectangular holes are carved in the wires. Here, the widths of the individual metal structures in between the slots lie within the area of a bamboo structure, while the resulting total width of all the metal structures meets power requirements.

On the same principle, often a fine-grain power mesh is laid over the circuit. Because it has so many wires, their individual widths are within the area of a bamboo structure.

It is also noteworthy that process variations play an important role in variations of wire widths (e.g. etch loss, lithography issues) and of wire heights (e.g. variations of metal deposition) as well as affecting the via fill rate. Hence, related worst-case process

variations must always be considered to establish reliable interconnect dimensions.

3.4 Wire Length

There is also a lower limit for the length of the interconnect that will allow electromigration to occur. It is known as "Blech length", and any wire that has a length below this limit (typically in the order of 10-100 µm) will not fail by electromigration. Here, a mechanical stress buildup causes a reversed migration process which reduces or even compensates the effective material flow towards the anode (Figure 6). Specifically, a conductor line is not susceptible to electromigration if the product of the wire's current density J and the wire length l is smaller than a process-technology-dependent threshold value $(J \cdot l)_{threshold}$ [3].

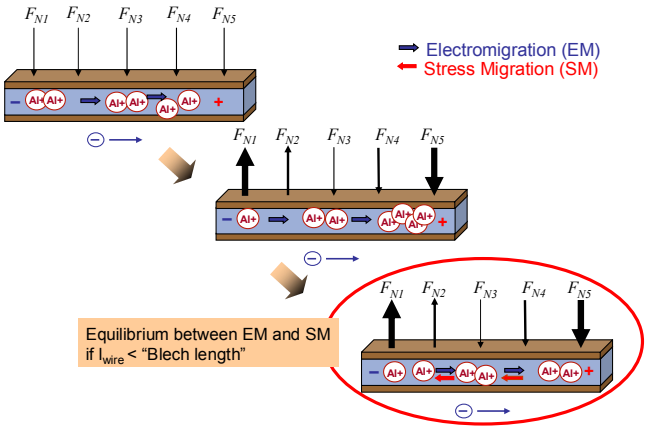

Figure 6. An illustration of stress migration caused by the hillock area in a short wire. This reversed migration process essentially compensates the material flow due to electromigration.

The Blech length must be considered when designing test structures for electromigration. Due to various implementation problems, exploiting this compensation effect in order to generate so-called "immortal wires" has shown only limited applicability in real-world circuits so far.

3.5 Via Arrangements and Corner Bends

Particular attention must be paid to vias and contact holes, because generally the ampacity of a (tungsten) via is less than that of a metal wire of the same width. Hence multiple vias are often used, whereby the geometry of the via array is very significant: Multiple vias must be organized such that the resulting current flow is distributed as evenly as possible through all the vias (Figure 7).

The so-called "Reservoir effect" [11] can be utilized to significantly improve the via array lifetime. Here, increased metal-via layer overlaps enlarge the material reservoir in the via.

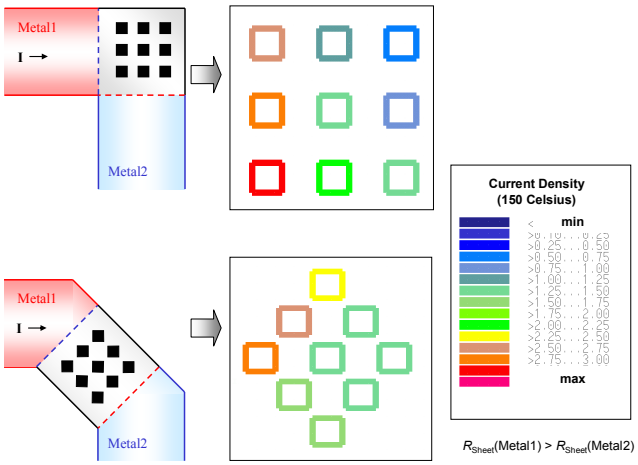

Figure 7. Current-density distribution within various vias of a via array. In the upper example, the lower left via is overloaded while the upper right vias hardly carry any current at all. A better arrangement is presented below.

Attention must also be paid to bends in interconnects. In particular, 90-degree corner bends must be avoided, since the current density in such bends is significantly higher than that in oblique angles of, for example, 135 degrees (Figure 8).

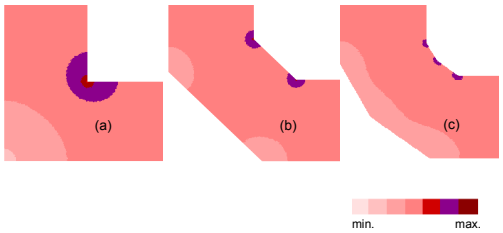

Figure 8. Current-density visualization of different corner bend angles of (a) 90°, (b) 135°, and (c) 150°.

3.6 Terminal Connections

Analog terminals (pins) are distinguished by a great variety of shapes and sizes. When connecting such a terminal to a wire, designers must bear in mind that different connection positions of a wire to this terminal can cause different current loads within the terminal structure. For this reason, a current density verification should include not only the interconnects, but also all terminal structures.

While designing the interconnects (the routing step), it is advisable to determine the ampacities of the various terminal regions (Figure 9) and compare them with the maximum current of the wire(s) reaching the terminal. The terminal areas of ampacity below the expected maximum wire current should then be eliminated as candidates for circuit connections.

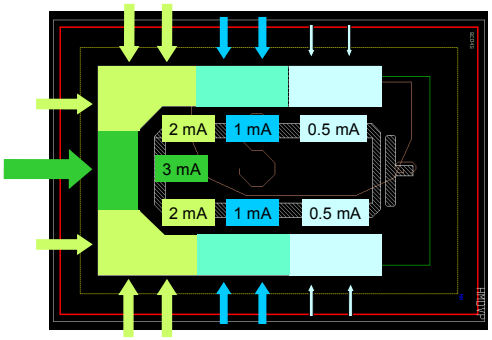

Figure 9. Terminal regions of a U-shaped pin consisting of one metallization layer. Current-density correct terminal connections require the verification of all terminal regions with regard to their maximum permissible currents and a subsequent consideration of these values when connecting the wire(s) to the terminal.

4. CURRENT CONSIDERATIONS

4.1 Current Models

As we mentioned already, the current waveform and the electromigration-robustness of the interconnect are closely related. Studies (such as in [12] - [15]) show an increased electromigration-robustness of the interconnect for bi-directional and pulsed current stress compared to single direction current and constant current stress. One of the reasons for this dependency is the so-called self-healing effect – due a material flow back caused by alternating current directions –, which reduces the effective material migration [12][13].

When considering terminal and wire currents in an electromigration-aware design flow, various models are applied based on the frequency of the current flow: (1) the effective current model based on the root-mean-square value of the currents (RMS currents) for frequencies smaller than 1 Hz, (2) the average current model for frequencies greater than 1 Hz, and (3) the peak current model which considers ESD (electrostatic discharge) events.

The RMS-current-based does not take into account the self-healing effect. This model represents a more conservative approach and so it is suitable for all analog DC nets and reliability-critical applications in general.

The average-current-based model considers the self-healing effect of alternating current directions. It is commonly applied to current flows within digital signal nets.

A peak-current flow (such as short-time current flows due to an ESD event) has to be considered separately from RMS- or average-current-based models. This is due to different damaging effects within the metallization resulting in different design rules for conductor dimensioning.

4.2 Terminal Currents

A problem for any electromigration-aware physical design methodology is the determination of realistic current values for each net terminal. Extensive studies have been conducted to address this issue (such as in [12] - [15]). Most approaches use a *single* so-called "equivalent current value" per terminal by considering the current waveform, duty cycle and frequency. However, single current values are not sufficient in order to calculate currents in various Steiner point connections. For example, a "current value propagation problem" arises within a Steiner point if two connected net terminals are characterized by *reversed* worst case currents flows.

We suggest two current value models that are capable of resolving the above mentioned current value propagation problem by utilizing either a single current value pair or a vector of current value pairs.

In our first current value model, the results from one or more simulations are post-processed by calculating a set of **current vectors** satisfying Kirchhoff's current law. They represent a snapshot of the circuits operation at the time of minimum and maximum currents *at each terminal* (Figure 10). This reduces the simulation results to a vector of worst case current value ranges. For a net with m terminals, this may lead to up to m current value pairs (i.e. $2m$ current values) attached to each terminal $i_{terminal}$:

$$i_{terminal} = [[i_{i\_min(terminal\_1)}, i_{i\_max(terminal\_1)}], [i_{i\_min(terminal\_2)}, i_{i\_max(terminal\_2)}], \ldots [i_{i\_min(terminal\_m)}, i_{i\_max(terminal\_m)}]],$$

(e.g. $i_{terminal} = [[-0.5mA, 1.8mA], [0, +0.4mA], \ldots, [-0.2mA, 0]]$).

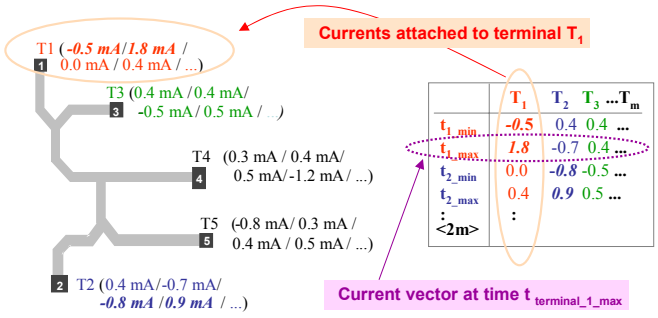

Figure 10. An illustration of the first approach utilizing current vectors. Current values assigned to terminals are their respective minimum and maximum values (shown in *italic*) and the current values at the other terminals' minimum and maximum points of time. Every current vector satisfies Kirchhoff's current law, i.e., its current sum is zero.

The second approach uses **a vector with one current value pair for each of *n* time slots S_x** ($x = 1 \ldots n$). The minimum and maximum current values of a current value pair are determined between the start and end time of the particular time slot. The current values are obtained either by circuit simulation, by manual

attachment to the net terminal in the schematic, or determined from a device library. This model accounts for independent current flow events originated from multiple net terminals.

$$i_{terminal} = [[S_1, i_{min\_1}, i_{max\_1}], [S_2, i_{min\_2}, i_{max\_2}], \ldots, [S_n, i_{min\_n}, i_{max\_n}]]$$

$$(\text{e.g. } i_{terminal} = [[S_1, -1mA, +3mA], [S_2, +2mA, +3mA], \ldots]).$$

5. ELECTROMIGRATION-AWARE DESIGN FLOW

We propose an electromigration-aware physical design flow that has been implemented and verified in a commercial design environment tailored to analog and mixed-signal ICs for automotive applications [16] - [18]. This flow includes three modules that have been specifically developed to address electromigration-relevant physical design constraints: current-driven routing, current-density verification, and current-driven layout decompaction (Figure 11).

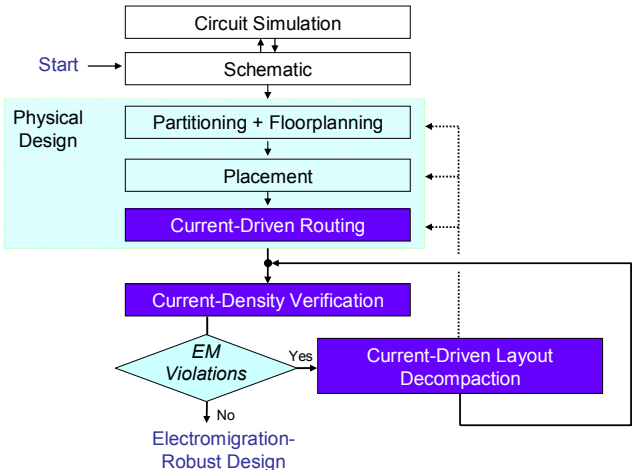

Figure 11. Our electromigration-aware analog and mixed-signal design flow includes current-driven routing, verification and layout decompaction tools intended for an electromigration-robust IC layout.

Current-driven routing ensures that the widths of all automatically routed interconnect structures are laid out correctly to fulfill all predefined electromigration and ESD reliability requirements.

The subsequently applied current-density verification tool automatically checks current densities within all layout segments, including arbitrarily shaped terminal and routing fragments and any manually routed interconnects. It also verifies the homogeneity of the current flow. (Homogeneity can be achieved during routing only to a certain level. This is due to the effects of the sequential character of any routing procedure as well as the limited capabilities of global interconnect planning. An inhomogeneous current flow favors the occurrence of electromigration.)

Finally, current-driven layout decompaction performs a post-route adjustment of layout segments with current-density violations and inhomogeneous current flows, respectively. Current-driven decompaction has been shown to be an effective point tool when addressing current-density-related violations without invoking a repetition of the entire place and route cycle.

5.1 Current-Driven Routing

A current-driven routing procedure consists of three basic steps:

(1) wire planning comprising net topology planning and terminal connection checking,

(2) calculation of required wire and via array dimensions, and

(3) final routing of the point-to-point-connections utilizing a detailed router.

The major challenge facing any current-driven signal routing is the inherent feature that segment currents are only known *after* the entire topology of the net has been laid out. In other words, currents strengths are altered in a previously routed sub-net whenever a new terminal is linked to the net (Figure 12). However, segment currents should be considered when deciding the routing sequence of net segments.

To address this cyclic conflict, a wire planning step is introduced. Its major characteristic is *concurrent* net topology planning and segment current calculation.

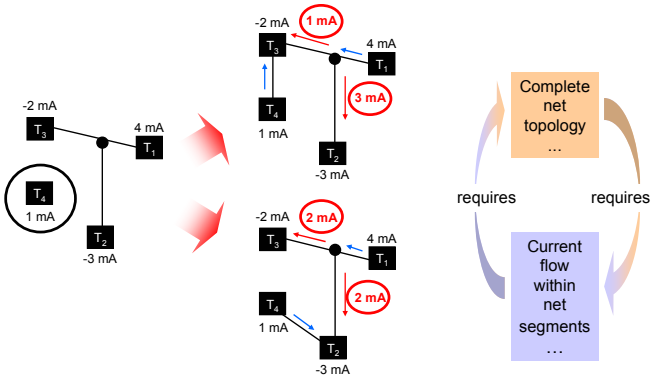

Figure 12. Illustration of the cyclic conflict whereby the sequence of all terminals to be connected must be known in order to allow for a current calculation within net segments. At the same time, laying out the sequence of connections requires currents to be known in order to fulfill certain optimization criteria. (Single terminal current values instead of boundary current values are used here for simplicity.)

During wire planning, a current-driven net topology is determined by calculating an optimized routing tree. Its major optimization goal is a minimization of the interconnect *area* (rather than simple length minimization), i.e. current-intensive segments are kept as short as possible. At the same time, the current-strength capabilities of net terminals to be connected have to be verified (Section 3.6).

After the net topology is defined, the net segment currents obtained are used to calculate the correct layout sizes for wires and via arrays.

Since currents have already been taken into account during the wire planning phase, the detailed routing is then considered to be a point-to-point routing between the planned net terminals with known wire and via array sizes.

Please refer to [16] for a detailed description of the current-driven routing algorithm, including experimental results and implementation remarks.

5.2 Current-Density Verification

The task of current-density verification is to check that the maximum current densities occurring within the interconnect and the device metallization do not exceed the maximum permitted layer-dependent current densities for the predefined working temperature of the chip.

Our suggested approach includes a quasi-3D model to verify irregularities such as vias arrays. It also incorporates thermal simulation data to account for the temperature dependency of the electrical field configuration and the electromigration process. There are four basic steps:

(1) current-density verification of net terminals (intrinsic reliability),

(2) determination and de-selection of non-critical nets,

(3) calculation of current densities within the given metallization layout, and

(4) evaluation of the violations obtained.

First, a current-density verification of net terminals is performed to ensure that the metallization of the net terminals sustain the assigned current values.

Non-critical nets are excluded from further checking. The criticality of a net is determined by considering the sum of the worst-case current values of each net terminal. The net is excluded if this sum is smaller than the maximum permitted current on the minimum sized metallization layer.

The layout topology of critical nets is then extracted for a subsequent determination of worst-case equivalent and ESD-current-flow conditions, which is done by calculating all possible up- and down-stream current strengths. This methodology makes it possible to cut the net layout into smaller and independent segments. The determined worst-case currents are then assigned to the segment cuts. This allows a simultaneous verification of all given worst-case currents with only one detailed current density calculation cycle per independent layout segment.

The current density within the metallization of a layout segment is calculated by using the finite element method (FEM). Here, the layout is segmented further into finite elements (triangles) and the current density is calculated using the potential field gradient. Afterwards, the current density is compared with its maximum permissible value within each finite element.

After the violating layout regions have been determined, the verification results must be evaluated to separate “dummy errors” (e.g. current-density spots at corner coordinates) from real violations.

An example of a verification result is shown in Figure 13.

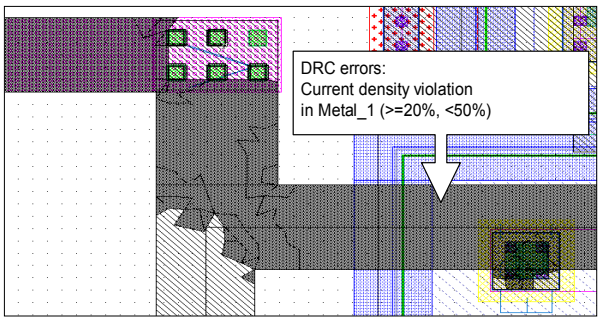

Figure 13. Excerpt of a current-density verification layout with a flagged violation area marked in dark grey.

We refer the reader to [17] for a detailed description of our verification approach.

5.3 Current-Driven Layout Decompaction

As already mentioned, current-driven layout decompaction has been shown to be an effective point tool to avoid repeated place and route cycles when addressing current-density verification errors. Its major goals are the post-route adjustment of layout segments according to their actual current density and a homogenization of the current flow.

Our decompaction approach utilizes the current-density verification tool (Section 5.2) to identify regions with excessive current-density stress. Based on these data, four steps are performed:

(1) layout decomposition,

(2) wire and via array sizing,

(3) addition of support polygons, and

(4) layout decompaction.

During layout decomposition, all net segments are retrieved from the given net layout. The end points of each segment (i.e. net terminals or layout Steiner points) then represent either (artificial) current sources or current sinks.

The current within a net segment is determined using the location-dependent current-density data obtained from the prior current-density calculation. The subsequent calculation of the appropriate cross-section areas of critical wires and via arrays is based on these current values.

The addition of so called “support polygons” to critical layout corners (e.g. wire bends) and around net terminals is required to reduce the local current-density stress if wire widening is not applicable (e.g. at terminals) or sufficient (e.g. addressing current-density spots in corner bends).

The final layout decompaction with cross-section area adjustment can be performed with any layout decompaction tool capable of simultaneous compaction and decompaction of layout structures while preserving the net topology.

An example of current-driven layout decompaction is shown in Figure 14.

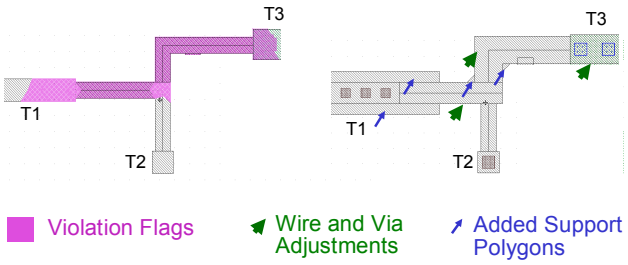

Figure 14. Net with current-density violation flags (left) and net and via layout after current-driven layout decompaction (right).

Please refer to [18] for a detailed description of the decompaction methodology.

6. CONCLUDING REMARKS

Electromigration is growing as a design problem due to increased interconnect current densities related to IC down-scaling. If not properly dealt with, it could constitute a major threat to interconnect reliability, especially in analog interconnect and power supply lines in digital circuits. Ongoing down-scaling is also increasing the risk of electromigration in digital signal interconnects.

In order to address this problem, this talk has focused on basic design issues that affect electromigration during interconnect physical design. Here, most measures aim at limiting the current densities in all parts of the circuits, notably the interconnect and terminal connections. We also mentioned various technology solutions to the electromigration problem, such as generating a bamboo structure, replacing aluminum with copper wires and depositing a passivation over the metal interconnect.

Finally, we introduced an electromigration-aware physical design flow. In addition to the regular design steps, this flow contains three current-density-driven design and verification tools which allow an effective consideration of electromigration-related constraints during physical design.

We believe that the consideration of electromigration-related design constraints and an efficient verification of current densities should be an integral part of any future design flow.

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