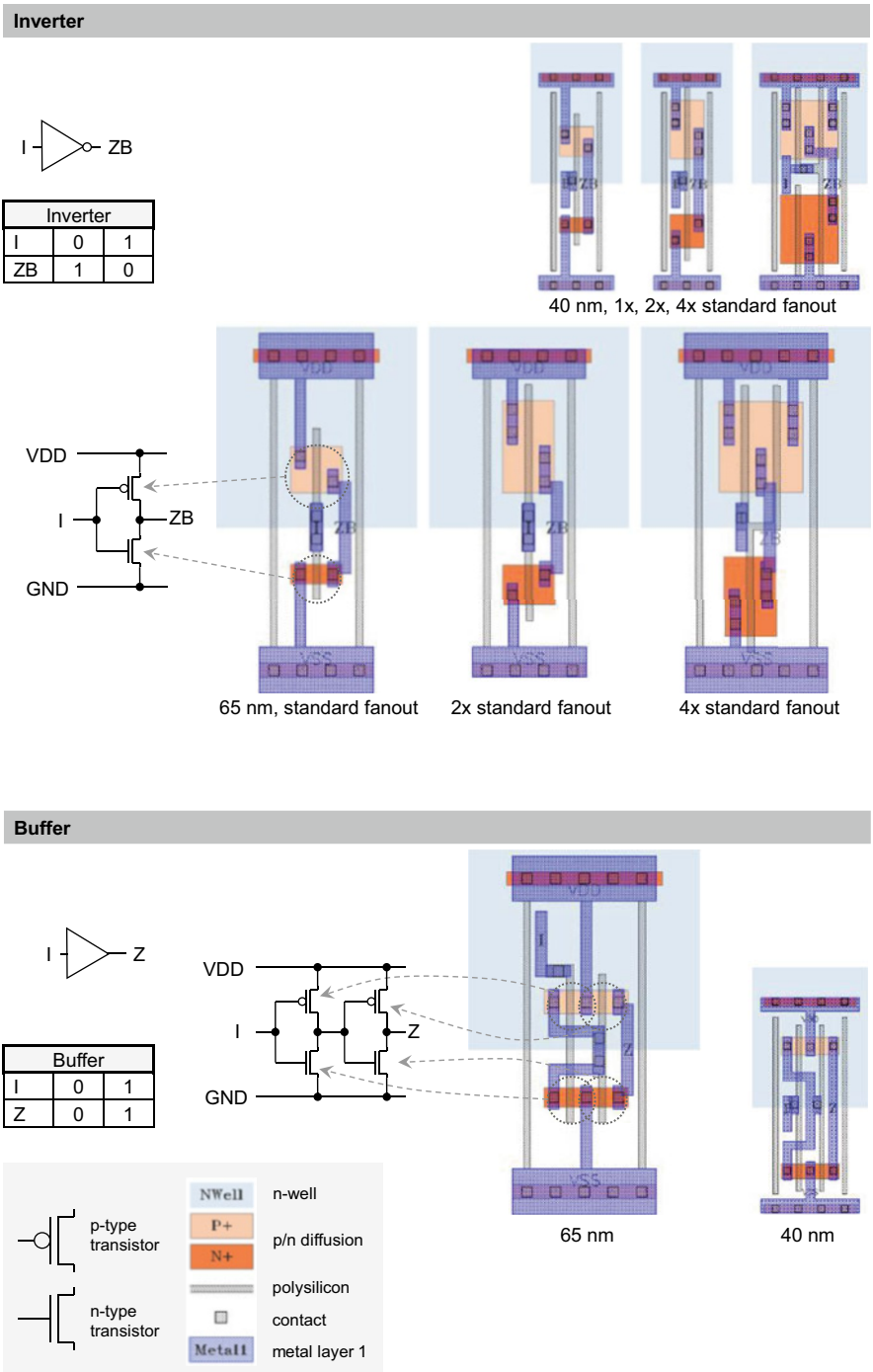
9.3 Example CMOS Cell Layouts



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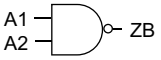
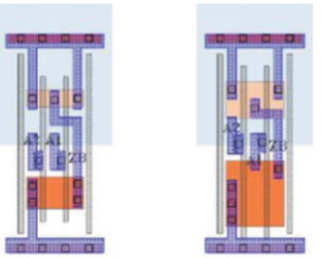
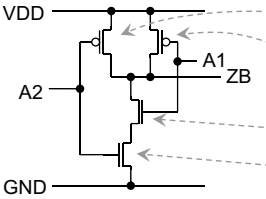
NAND gate (2-input)

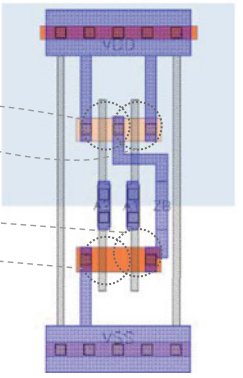


NAND				
A1	0	0	1	1
A2	0	1	0	1
ZB	1	1	1	0

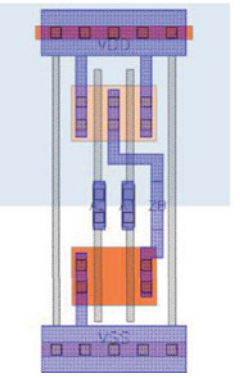


40 nm, 1x and 2x standard fanout



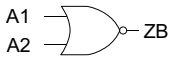


65 nm, standard fanout

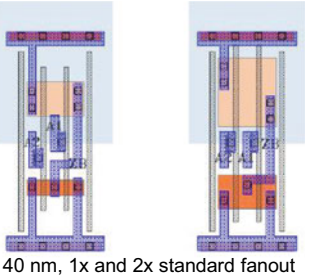


65 nm, 2x standard fanout

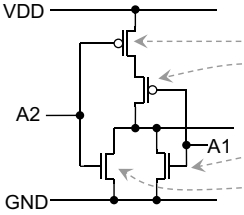
NOR gate (2-input)

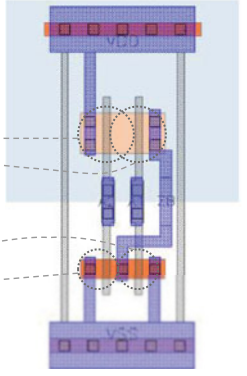


NOR				
A1	0	0	1	1
A2	0	1	0	1
ZB	1	0	0	0

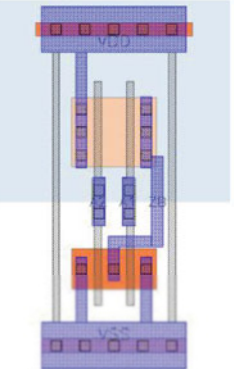


40 nm, 1x and 2x standard fanout



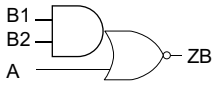


65 nm, standard fanout

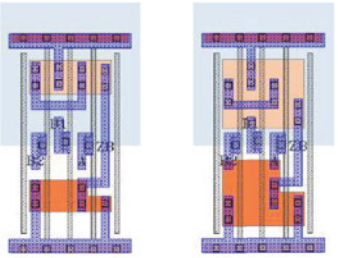


65 nm, 2x standard fanout

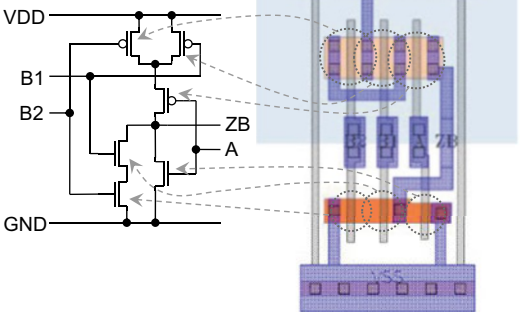
AND-OR-Invert (AOI) gate (2-1)



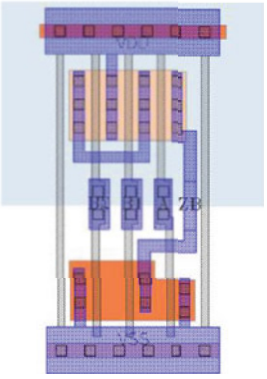
AOI								
A	0	0	0	0	1	1	1	1
B1	0	0	1	1	0	0	1	1
B2	0	1	0	1	0	1	0	1
ZB	1	1	1	0	0	0	0	0



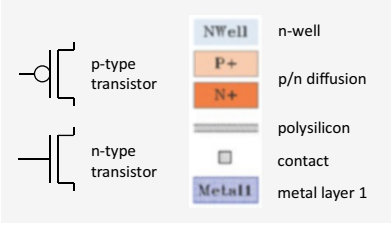
40 nm, 1x and 2x standard fanout



65 nm, standard fanout



65 nm, 2x standard fanout



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