VLSI Physical Design: From Graph Partitioning to Timing Closure

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VLSI Physical Design: From Graph Partitioning to Timing Closure

Second Edition

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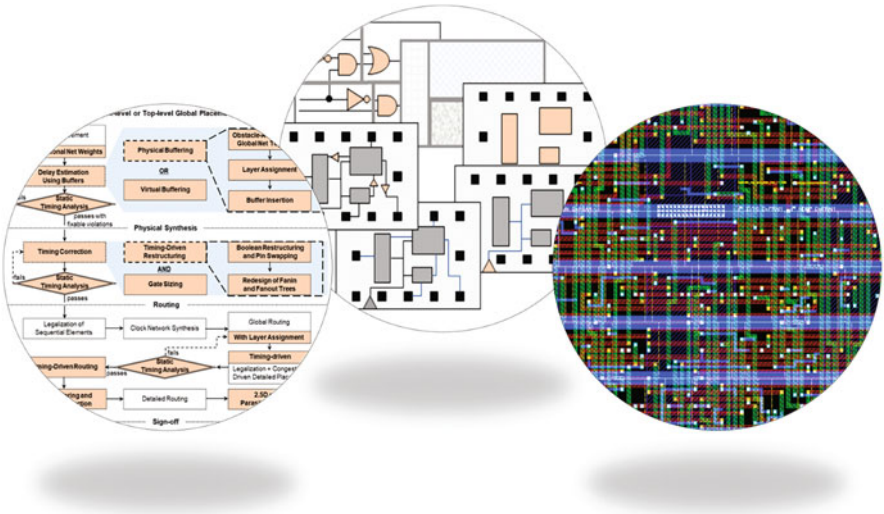
Physical Buffering
OR
Virtual Buffering
Layer Assignment
Buffer Insertion
Static Timing Analysis
passes with fixable violations
Physical Synthesis
Timing Correction
Timing-Driven Restructuring
AND
Gate Sizing
Boolean Restructuring and Pin Swapping
Redesign of Fanin and Fanout Trees
Static Timing Analysis
passes
Routing
Legalization of Sequential Elements
Clock Network Synthesis
Global Routing
With Layer Assignment
Timing-driven
Static Timing Analysis
Detailed Routing
Sign-off

Foreword

Physical design of integrated circuits remains one of the most interesting and challenging arenas in the field of electronic design automation. The ability to integrate more and more devices on our silicon chips requires the algorithms to continuously scale up. Nowadays, we can integrate 12 billion transistors on a single 5 nm-technology chip. This number will continue to scale up for the next couple of technology generations, requiring more transistors to be automatically placed on a chip and connected. In addition, more and more of the delay is contributed by the wires that interconnect the devices on the chip. This has a profound effect on how physical design flows need to be put together. In the 1990s, it was safe to assume that timing goals of the design could be reached once the devices were placed well on the chip. Today, one does not know whether the timing constraints can be satisfied until the final routing has been completed.

As far back as 15 or 20 years ago, people believed that most physical design problems had been solved. But the continued increase in the number of transistors on the chip, as well as the increased coupling between the physical, timing, and logic domains, warrants a fresh look at the basic algorithmic foundations of chip implementation. That is exactly what this book provides. It covers the basic algorithms underlying all physical design steps and shows how they are applied to current instances of the design problems. For example, Chap. 7 provides a great deal of information on special types of routing for specific design situations.

Several other books provide in-depth descriptions of core physical design algorithms and the underlying mathematics, but this book goes a step further. The authors very much realize that the era of individual point algorithms with single objectives is over. Throughout the book, they emphasize the multi-objective nature of modern design problems, and they bring all the pieces of a physical design flow together in Chap. 8. A complete flowchart, from design partitioning and floorplanning all the way to electrical rule checking, describes all phases of the modern chip implementation flow. Each step is described in the context of the overall flow with references to the preceding chapters for the details. New advances in semiconductor technology such as nano-sheet transistors and backside power distribution will require us to once more revisit our core optimization strategies and algorithms. Recent advances in machine learning have shown that there is more room for optimization in the commonly practiced design flows.

This book will be appreciated by students and professionals alike. It starts from the basics and provides sufficient background material to get the reader up to speed on the real issues. Each of the chapters by itself provides sufficient introduction and depth to be very valuable. This is especially important in the present era, where experts in one area must understand the effects of their algorithms on the remainder of the design flow. An expert in routing will derive great benefit from reading the chapters on planning and placement. An expert in design for manufacturability (DFM) who seeks a better understanding of routing algorithms, and of how these algorithms can be affected by choices made in setting DFM requirements, will benefit tremendously from the chapters on global and detailed routing. Any technologist participating in design technology co-optimization (DTCO) should have a good understanding of the key algorithms in this book to push the boundaries of what is physically possible and maximally beneficial to the design tools and designers.

The book is completed by a detailed set of solutions to the exercises that accompany each chapter. The exercises force the student to truly understand the basic physical design algorithms and apply them to small but insightful problem instances.

This improved, second edition of the book will continue to serve the EDA and design community well. It is a foundational text and reference for the next generation of professionals who will be called on to continue the advancement of our chip design tools and design the most advanced microelectronics.

Poughkeepsie, NY, USA
Spring 2022

Leon Stok
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Preface to the 2nd Edition

Since its publication more than 10 years ago, this book has been met with widespread positive response in both teaching and practice, making the publication of a second edition a logical step. We have used this opportunity to incorporate corrections and improvements, and added a new section on machine learning, without fundamentally changing the proven structure of the book. Many readers have come to appreciate the clear, graphically descriptive structure, which allows them to understand complex algorithmic relationships. This recipe for success also led to the translation of the book into traditional Chinese, and this edition also became quite popular in its specific market.

Even if most of the algorithms presented are "classics," and some many decades old, an understanding of their fundamental character is still indispensable for today's highly complex design systems. This algorithmic knowledge is useful not only for electronic design automation (EDA), but also in other application areas. Anyone who has ever programmed a Dijkstra's algorithm for intelligent, effective pathfinding will confirm that it can be used to optimize much more, including traffic and infrastructure projects. In addition, the knowledge of EDA algorithms leads to an enormous increase in competence when using commercially available EDA tools. Just as it is hard to imagine driving a car with expertise without knowing what is going on under the hood, knowing basic algorithmic principles makes it easier to grasp, master, and fully utilize modern EDA systems.

We want to thank all those involved in the preparation of this second edition. We would like to mention Andreas Krinke, who used countless exercises in design automation to detect even the smallest incorrectness in the explanations. We also thank Robert Fischbach and Mike Alexander for their editing support. Finally, we would like to thank Springer, and in particular Charles Glaser, for their kind cooperation and support in the publication of this book.

Most importantly, we thank the many students who, year after year, ask probing questions after the lectures with the open book in their hands. May they keep their curiosity and thirst for knowledge alive, and may the book be a faithful companion in their further professional life.

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Preface to the 1st Edition

VLSI physical design of integrated circuits underwent explosive development in the 1980s and 1990s. Many basic techniques were suggested by researchers and implemented in commercial tools, but only described in brief conference publications geared for experts in the field. In the 2000s, academic and industry researchers focused on comparative evaluation of basic techniques, their extension to large-scale optimization, and the assembly of point optimizations into multi-objective design flows. Our book covers these aspects of physical design in a consistent way, starting with basic concepts in Chapter 1 and gradually increasing the depth to reach advanced concepts, such as physical synthesis. Readers seeking additional details will find a number of references discussed in each chapter, including specialized monographs and recent conference publications.

Chapter 2 covers netlist partitioning. It first discusses typical problem formulations and proceeds to classic algorithms for balanced graph and hypergraph partitioning. The last section covers an important application, system partitioning among multiple FPGAs, used in the context of high-speed emulation in functional validation.

Chapter 3 is dedicated to chip planning, which includes floorplanning, power-ground planning, and I/O assignment. A broad range of topics and techniques are covered, ranging from graph theoretical aspects of block packing to optimization by simulated annealing and package-aware I/O planning.

Chapter 4 addresses VLSI placement and covers a number of practical problem formulations. It distinguishes between global and detailed placement and first covers several algorithmic frameworks traditionally used for global placement. Detailed placement algorithms are covered in a separate section. Current state of the art in placement is reviewed, with suggestions to readers who might want to implement their own software tools for large-scale placement.

Chapters 5 and 6 discuss global and detailed routing, which have received significant attention in research literature due to their interaction with manufacturability and chip yield optimizations. Topics covered include representing layout with graph models and performing routing, for single and multiple nets, in these models. State-of-the-art global routers are discussed, as well as yield optimizations performed in detailed routing to address specific types of manufacturing faults.

Chapter 7 deals with several specialized types of routing, which do not conform with the global detailed paradigm followed by Chapters 5 and 6. These include non-Manhattan area routing, commonly used in PCBs, and clock tree routing required for every synchronous digital circuit. In addition to algorithmic aspects, we explore the impact of process variability on clock tree routing and means of decreasing this impact.

Chapter 8 focuses on timing closure, and its perspective is particularly unique. It offers a comprehensive coverage of timing analysis and relevant optimizations in placement, routing, and netlist restructuring. Section 8.6 assembles all these techniques, along with those covered in earlier chapters, into an extensive design flow, illustrated in detail with a flowchart and discussed step-by-step with several figures and many references.

This book does not assume prior exposure to physical design or other areas of EDA. It introduces the reader to the EDA industry and basic EDA concepts, covers key graph concepts and algorithm analysis, carefully defines terms, and specifies basic algorithms with pseudocode. Many illustrations are given throughout the book, and every chapter includes a set of exercises, solutions to which are given in one of the appendices. Unlike most other sources on physical design, we made an effort to avoid impractical and unnecessarily complicated algorithms. In many cases, we offer comparisons between several leading algorithmic techniques and refer the reader to publications with additional empirical results.

Some chapters are based on the material in the book *Layoutsynthese elektronischer Schaltungen – Grundlegende Algorithmen für die Entwurfsautomatisierung*, which was published by Springer in 2006 and 2016, respectively.

We are grateful to our colleagues and students who proofread earlier versions of this book and suggested a number of improvements (in alphabetical order): Matthew Guthaus, Kwangok Jeong, Seokhyeong Kang, Johann Knechtel, Andreas Krinke, Jingwei Lu, Nancy MacDonald, Jarrod Roy, Kambiz Samadi, Yen-Kuan Wu, and Hailong Yao.

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We hope that you will find the book interesting to read and useful in your professional endeavors.

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