well, which in turn leads to EM-induced malfunctions. Interconnect properties are increasingly subjected to side effects: while on the one hand the barrier component of the overall cross-section is rising, the specific resistance of the interconnect track is increasing due to the scattering effects of electron conduction. Both side effects accelerate the characteristic heat increase (*Joule heating*) of the interconnect. Hence, the reduction in cross-sectional area causes a reduction in allowed current densities (see (3) in Fig. 1.5) for constant durability. There is a 50% decrease in the permissible current density every three years, according to [ITR14, ITR16].

The following conclusion can also be drawn from (1) and (2) in Fig. 1.5: The current densities required to operate an integrated circuit with decreasing structure sizes double approximately every eight years (see (4) in Fig. 1.5). This is directly opposed to falling current-density boundaries (3), as these opposing trends exacerbate the problem of rising current densities. This development (4) will cause a technological hurdle even if current-density boundaries are maintained at their present levels.

If required current densities exceed approved boundaries, this will spell the death knell for technological progress as we know it in this area. And, according to the ITRS [ITR14, ITR16], approved current densities are increasingly exceeded, which makes this topic of immediate concern for IC design.

1.4 Motivation and Structure of This Book

Integrated circuits have far greater reliability than circuits consisting of discrete components; this advantage is driving semiconductor scale reductions and associated investments in advanced technologies.

Unfortunately, increasingly small IC structures begin to have a significant negative impact on reliability, as the cross-sectional areas of the metallic interconnects in the ICs are diminished in size. The problem arises because the required currents cannot be reduced to the same extent—even by reducing the supply voltages and gate capacitances. This is illustrated in Fig. 1.6, where the required current densities to drive four inverter gates, for example, increase over time as a consequence of decreased structure size.

To make matters worse, the maximum tolerable current densities are shrinking at the same time due to smaller structure sizes (see Fig. 1.5). As already mentioned, the reason for this is that small voids and other material defects, which could have been tolerated in earlier technology nodes, cause increasingly dramatic damage and side effects to the wires with shrinking metal structures. Thus, maximum tolerable current densities will have to decrease to maintain the required interconnect reliability. As a result, the ITRS indicates that all minimum-sized interconnects will be

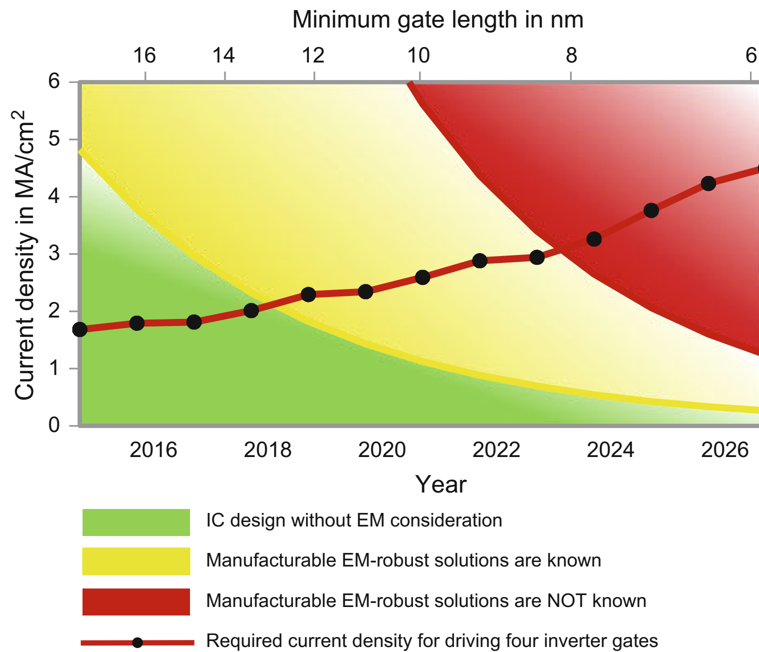

Fig. 1.6 Evolution of required and maximum current densities in IC interconnect [ITR14, ITR16]. While the required current density scales with frequency and reducing cross-section, the maximum tolerable current density is shrinking due to smaller structure sizes (cf. Fig. 1.5). EM degradation needs to be considered inside the yellow area. As of now, manufacturable solutions are not known in the red area

increasingly EM-affected, potentially limiting any further downscaling of wire sizes (Fig. 1.6, yellow barrier).

Furthermore, the total length of interconnect per IC will continue to increase. As a consequence, reliability requirements per length unit of the wires need to *increase* in order to *maintain* overall IC reliability. This accepted wisdom is contradicted by the future *decrease* in interconnect reliability due to electromigration—as noted above. The ITRS thus states that no known solutions are available for the EM-related reliability requirements that we will face in the near future (Fig. 1.6, red barrier).

Measures to handle electromigration, such as current-dependent routing or the adaptation of the track width in highly loaded interconnects, are *de rigueur* today for designing analog integrated circuits. As a result of structural miniaturization, digital integrated circuits are now also affected by the problem of increasing current densities and accompanying EM. Typical measures, such as increasing the interconnect width, common in analog circuit design, cannot be deployed in these much more complex digital circuits. Such measures would work against the reduction in structure size and prevent further scaling. New approaches are therefore required to avoid EM damage in digital circuits, as a result of falling semiconductor scale.

This book presents measures for layout design for avoiding damage caused by EM in both digital and analog ICs. We determine parameters for every measure so that the usability and suitability of a specific measure can be determined as a function of the technology used. Approved current densities can thus be increased at the critical places by means of local layout modifications. This ensures that current densities in the yellow section in Fig. 1.6 are tolerated as well. The aim essentially is to avoid exceeding approved current densities by enlarging reliability limits. This book provides the reader with the necessary knowledge to overcome such design challenges.

It is particularly important that the proposed measures be applied at the physical-design stage and especially for the routing step. The reason for this is that good interconnect routing allows the optimal utilization of measures for promoting EM robustness. Interventions at a later stage in the design process, typically involving layout modifications, are much less effective, because fewer modification options are available at this later stage. On the other hand, currents cannot be precisely specified before the layout is generated, as a physical network topology is needed to provide detailed current knowledge.

The fundamental physical problem of EM will be examined to the core in Chap. 2, as this knowledge is a requisite for adopting appropriate countermeasures. After first explaining the physical causes of EM, we introduce influencing factors arising from the specific circuit technology, the environment, and the design. We then investigate detailed EM mechanisms with regard to circuit materials, frequencies, and mechanical stresses. IC designers must be especially aware of thermal and stress migration; both are introduced and described in their interaction with EM.

Chapter 2 also outlines the principles of a migration analysis through simulation. This honors the importance of finite element modeling (using the finite element method, FEM) in EM analysis and enables the reader to develop and apply similar modeling and simulation techniques.

Chapter 3 presents options for modifying the present design methodology to encompass EM prevention. Analog and digital designs are considered separately in this context as the respective measures differ for both. Understanding that knowledge of the currents flowing in interconnects is a fundamental requisite for an EM-aware design flow, we will discuss the different types of currents encountered and show how sensible current values can be determined.

The key parameter for EM prevention is the maximum permissible boundary value of the current density in the wires. This parameter is, however, dependent on the intended use of the IC, which is why so-called mission profiles are created to determine such values. Chapter 3 describes how robust current-density boundary values (limits) can be determined, using application and reliability specifications.

Fundamental procedures for current-density verification are examined as well. Methods for eliminating problems, identified during current-density verification, by

means of layout adjustment are presented. Finally, we put forward a number of approaches for increasing current-density boundary values, based on our assessment of current technological trends.

While Chap. 3 outlined options to address EM in today's physical design of electronic circuits, Chap. 4 describes in detail the EM-inhibiting effects that these options are based on. The goal of this chapter is to summarize the state of the art in EM-mitigating effects. This knowledge is presented such that a circuit designer can use it to increase current-density limits with the overall goal of reducing the negative impact of EM on the circuit's reliability. We will show how approved current densities can be increased by means of local layout modifications. Detailed application advice concludes each presented measure.

We also consider material-related options to reduce EM, such as surface passivation, and the use of EM-robust materials, such as carbon nanotubes.

In Chap. 5, we summarize our findings, make proposals for further EM-aware integrated circuit design, and present the future outlook in this field, along with expected developments in micro- and nanoelectronics.

References

[Int17] 8th Gen (S-platform) Intel® processor family datasheet, vol. 1, 2017, https://www.intel.com/content/dam/www/public/us/en/documents/datasheets/8th-gen-processor-family-s-platform-datasheet-vol-1.pdf. Last retrieved on 1 Jan 2018

[ITR14] International Technology Roadmap for Semiconductors (ITRS), 2013 edn. (2014), http://www.itrs2.net/itrs-reports.html. Last retrieved on 1 Jan 2018

[ITR16] International Technology Roadmap for Semiconductors (ITRS 2.0), 2015 edn. (2016), http://www.itrs2.net/itrs-reports.html. Last retrieved on 1 Jan 2018

[KML+12] J. Knechtel, I.L. Markov, J. Lienig, et al., Multiobjective optimization of deadspace, a critical resource for 3D-IC integration, in *Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD)* (2012), pp. 705–712. https://doi.org/10.1145/2429384.2429538

[KYL12] J. Knechtel, E.F.Y. Young, J. Lienig, Planning massive interconnects in 3D chips. IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. 34(11), 1808–1821 (2015), ISSN 02780070. https://doi.org/10.1109/tcad.2015.2432141

[KSE+17] J. Knechtel, O. Sinanoglu, I. M. Elfadel, et al., Large-scale 3D chips: challenges and solutions for design automation, testing, and trustworthy integration, IPSJ Trans. on System LSI Design Methodology, **10**, 45–62 (2017). https://doi.org/10.2197/ipsjtsldm.10.45

[Moo65] G.E. Moore, Cramming more components onto integrated circuits. Electronics **38** (8), 114–117 (1965). https://doi.org/10.1109/N-SSC.2006.4785860

[PPL+11] J. Pak, M. Pathak, S.K. Lim, et al., Modeling of electromigration in through-silicon-via based 3D IC, in *61st IEEE Electronic Components and Technology Conference (ECTC)* (2011), pp. 1420–1427. https://doi.org/10.1109/ectc.2011.5898698

[PPP+11] M. Pathak, J. Pak, D.Z. Pan, et al., Electromigration modeling and full-chip reliability analysis for BEOL interconnect in TSV-based 3D ICs, in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)* (2011), pp. 555–562. https://doi.org/10.1109/iccad.2011.6105385