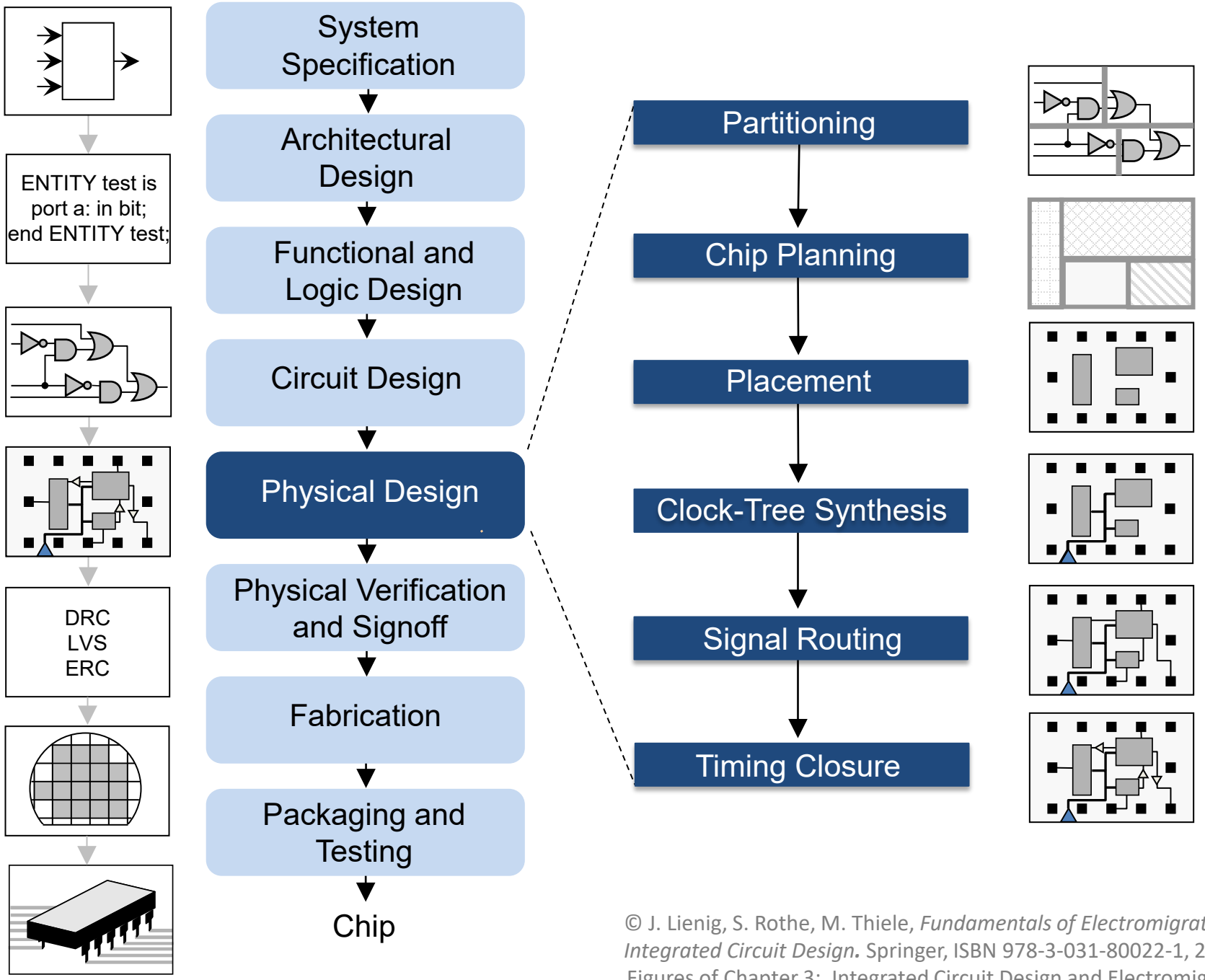
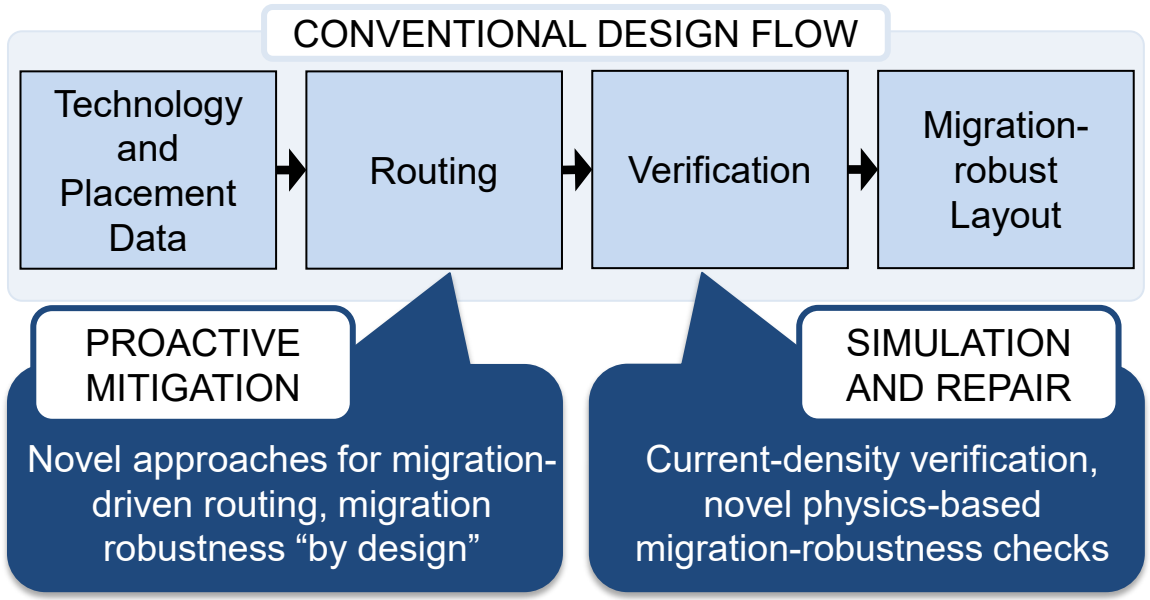
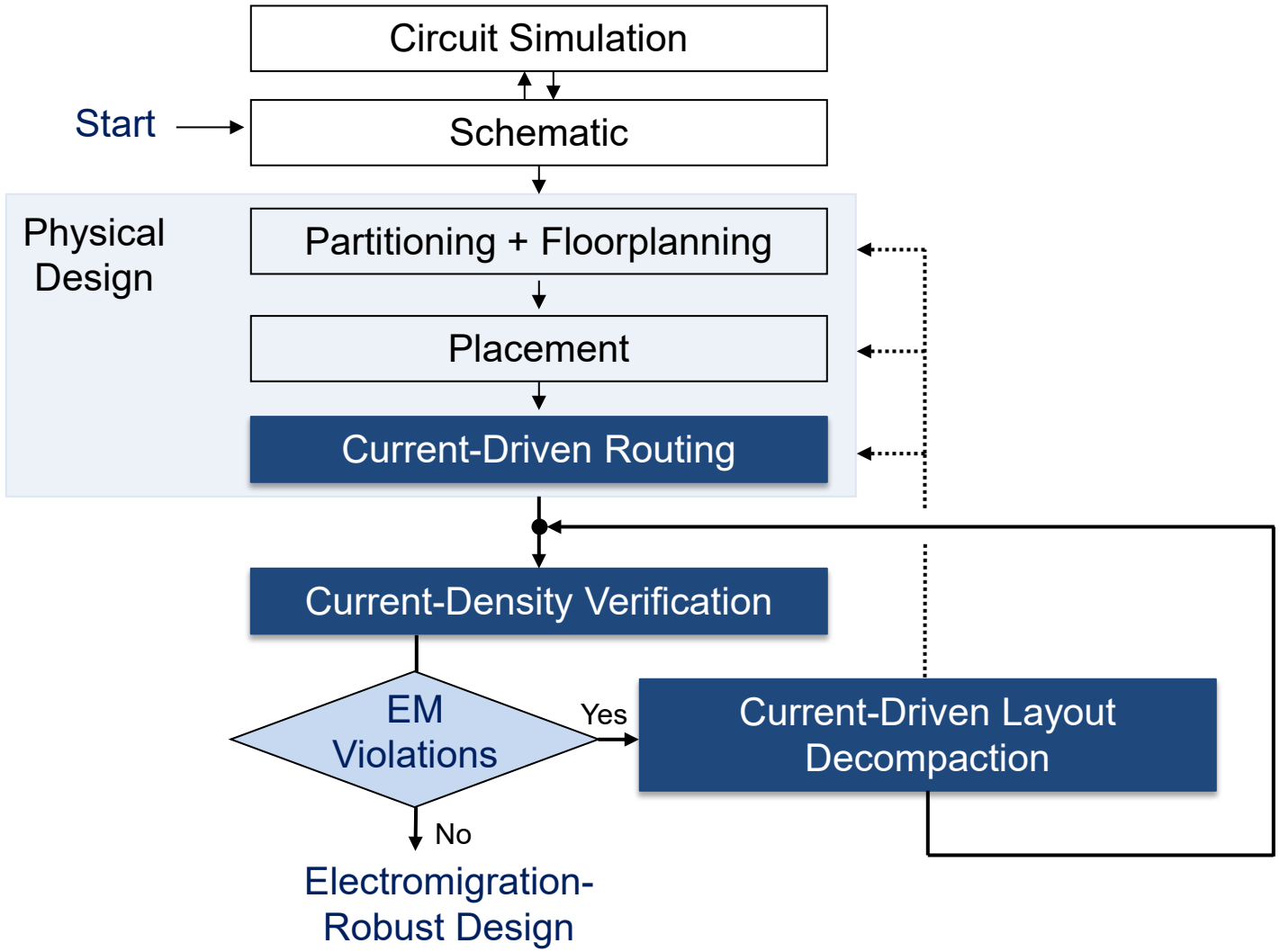
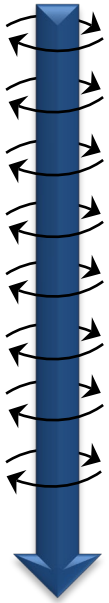



CONVENTIONAL DESIGN FLOW
Technology and Placement Data
Routing
Verification
Migration-robust Layout
PROACTIVE MITIGATION
Novel approaches for migration-driven routing, migration robustness “by design”
SIMULATION AND REPAIR
Current-density verification, novel physics-based migration-robustness checks


Circuit Simulation
Start
Schematic
Physical Design
Partitioning + Floorplanning
Placement
Current-Driven Routing
Current-Density Verification
EM Violations
Yes
Current-Driven Layout Decompaction
No
Electromigration-Robust Design

Synthesis

Logic Synthesis
Partitioning
Floorplanning
Power Routing
Global Placement
Detailed Placement
Clock Tree Synthesis
Global Routing
Detailed Routing
Timing Closure



Analysis / Verification

Formal Verification

Global Timing

Routability Prediction

Timing

Parasitic Extraction
Sign-off DRC
Sign-off Timing
Sign-off Spice Simulation

EM-Specific Analysis and Verification

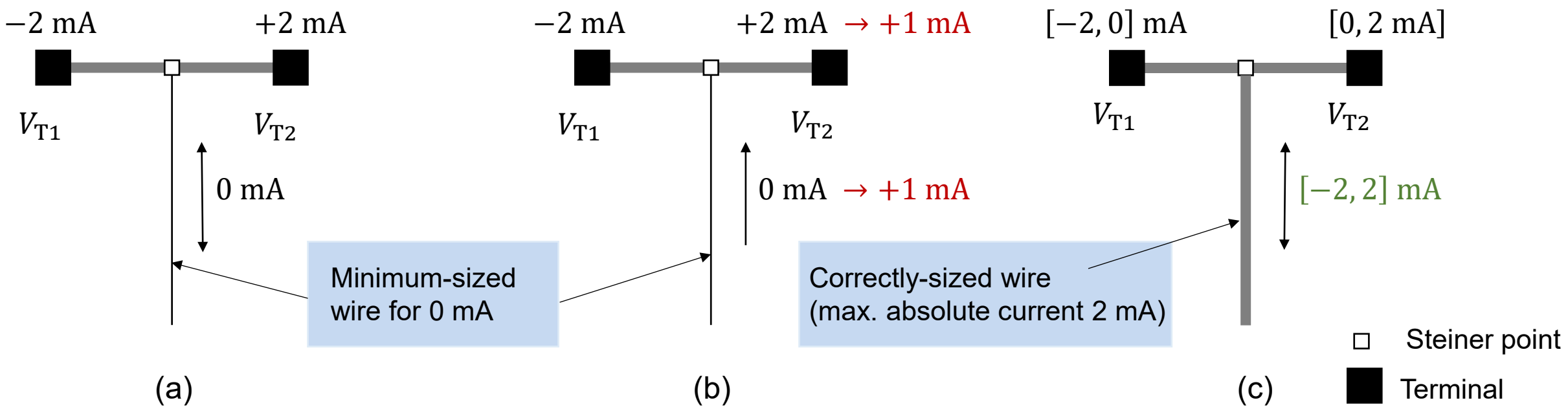
Estimation of EM-Critical Nets Based on Netlist

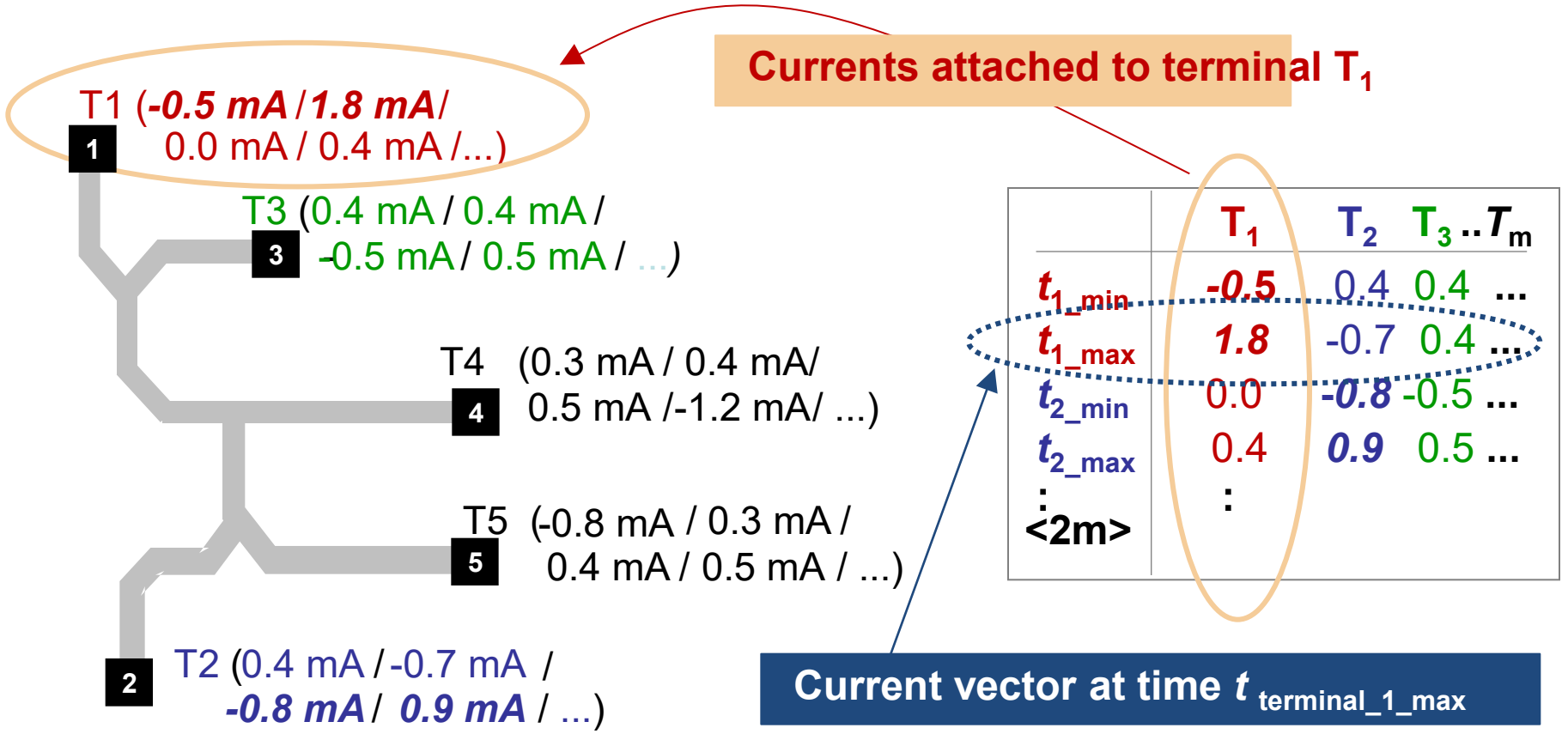
Current Density Distribution in Power Nets

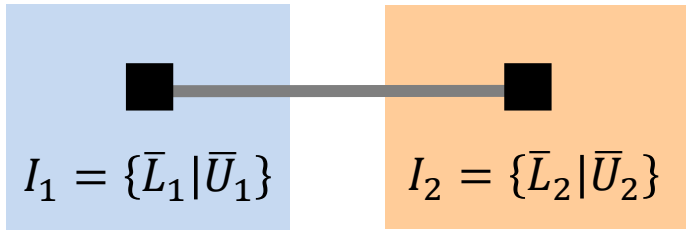
Current Density and Temperature Estimation

Sign-off DRC w/ EM Rules

Sign-off Spice Simulation of Currents in Segments


−2 mA
+2 mA
V_{T1}
V_{T2}
0 mA
Minimum-sized wire for 0 mA
(a)
−2 mA
+2 mA → +1 mA
V_{T1}
V_{T2}
0 mA → +1 mA
(b)
[−2, 0] mA
[0, 2 mA]
V_{T1}
V_{T2}
[−2, 2] mA
Correctly-sized wire (max. absolute current 2 mA)
(c)
Steiner point
Terminal


Currents attached to terminal T_1
T1 (-0.5 mA / 1.8 mA / 0.0 mA / 0.4 mA /...)
1
T3 (0.4 mA / 0.4 mA / -0.5 mA / 0.5 mA / ...)
3
T4 (0.3 mA / 0.4 mA/ 0.5 mA /-1.2 mA/ ...)
4
T5 (-0.8 mA / 0.3 mA / 0.4 mA / 0.5 mA / ...)
5
T2 (0.4 mA / -0.7 mA / -0.8 mA / 0.9 mA / ...)
2
T_1 T_2 T_3 .. T_m
t_{1_min} -0.5 0.4 0.4 ...
t_{1_max} 1.8 -0.7 0.4 ...
t_{2_min} 0.0 -0.8 -0.5 ...
t_{2_max} 0.4 0.9 0.5 ...
<2m>
Current vector at time t terminal_1_max



$I_1 = \{\overline{L}_1 | \overline{U}_1\}$

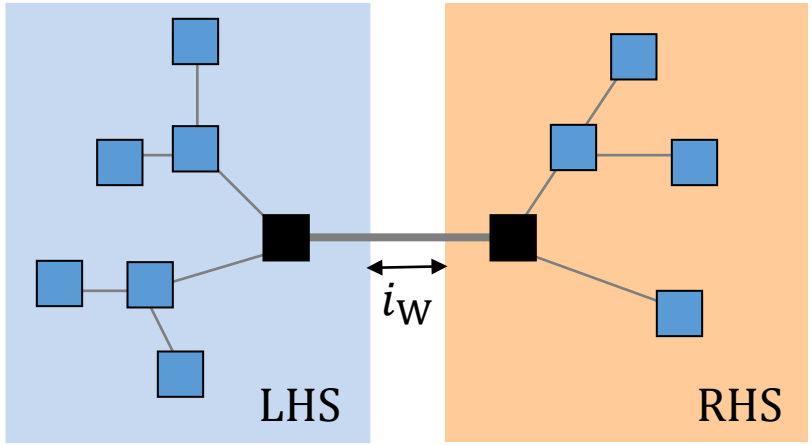
$I_2 = \{\overline{L}_2 | \overline{U}_2\}$

$$\overline{L}_n = \begin{pmatrix} i_{Ln,11} & i_{Ln,12} & \cdots & i_{Ln,1P} \\ i_{Ln,21} & i_{Ln,22} & \cdots & i_{Ln,2P} \\ \vdots & \vdots & \ddots & \vdots \\ i_{Ln,O1} & i_{Ln,O2} & \cdots & i_{Ln,OP} \end{pmatrix}$$

$$\overline{U}_n = \begin{pmatrix} i_{Un,11} & i_{Un,12} & \cdots & i_{Un,1P} \\ i_{Un,21} & i_{Un,22} & \cdots & i_{Un,2P} \\ \vdots & \vdots & \ddots & \vdots \\ i_{Un,O1} & i_{Un,O2} & \cdots & i_{Un,OP} \end{pmatrix}$$

Current type 1...*O*

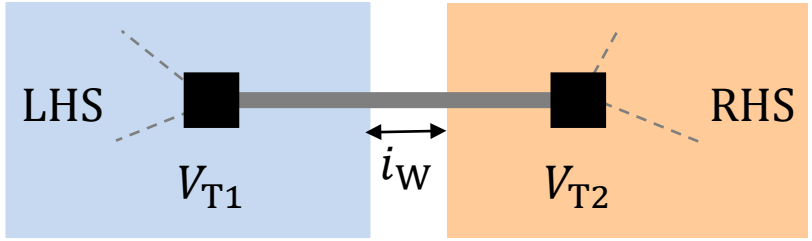
Operating phase 1...*P*



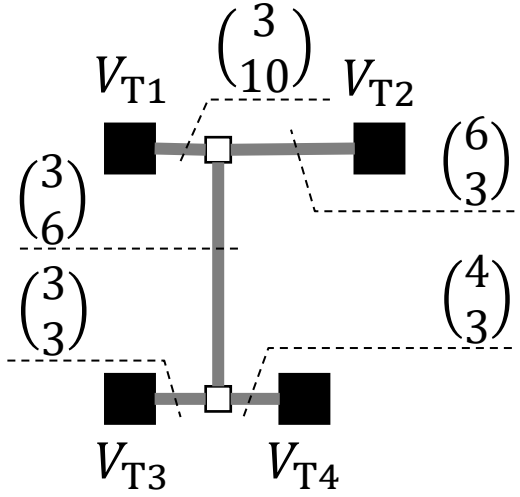
$\bar{L}_1 = (-1\ \text{mA})$ $\quad$ $\bar{L}_2 = (-3\ \text{mA})$

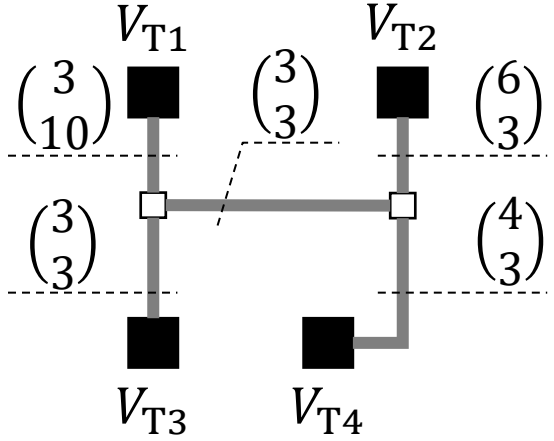
$\bar{U}_1 = (2\ \text{mA})$ $\quad$ $\bar{U}_2 = (0\ \text{mA})$

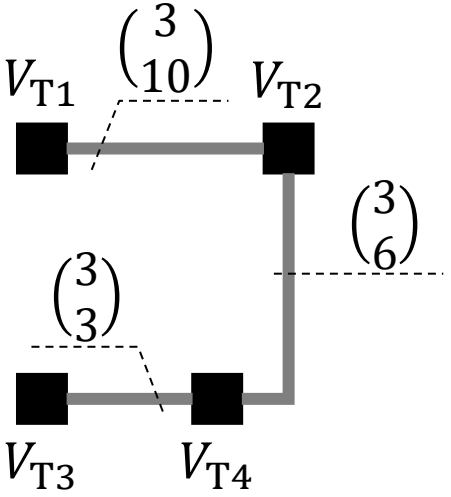
$$\vec{\imath}_W = \left(max \begin{cases} min(|-1\ \text{mA}|, |0\ \text{mA}|) \\ min(|-3\ \text{mA}|, |2\ \text{mA}|) \end{cases} \right)$$



$$\vec{\imath}_W = (2\ \text{mA})$$





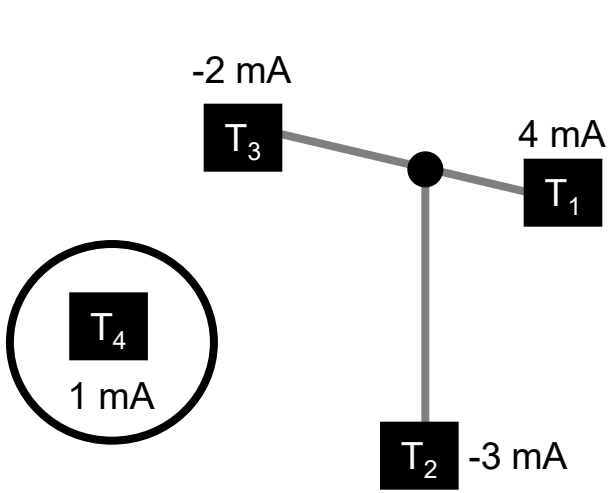


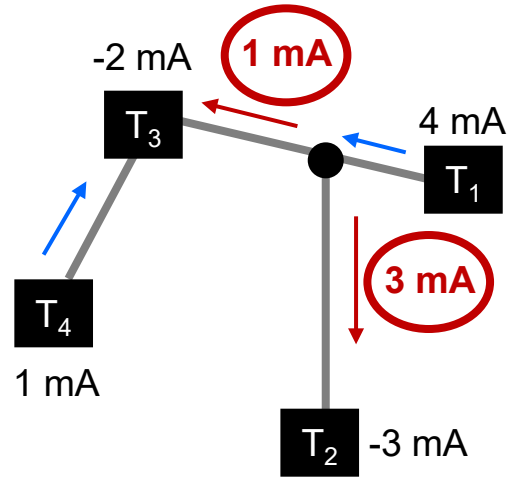
V_{T1}: $\bar{L}_1 = \begin{pmatrix}-1 & -2\\ -10 & -8\end{pmatrix}$ $\bar{U}_1 = \begin{pmatrix}3 & 2\\ 0 & 4\end{pmatrix}$

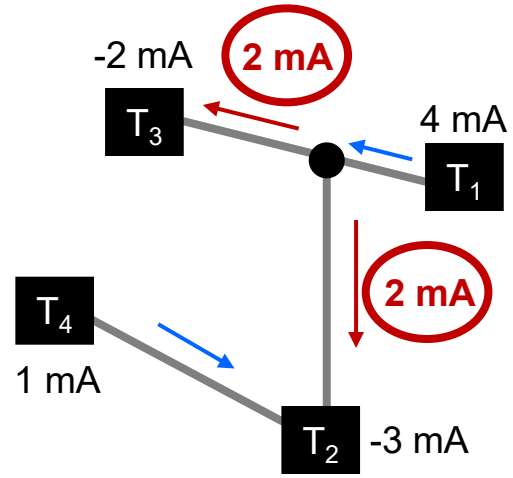
V_{T2}: $\bar{L}_2 = \begin{pmatrix}0 & -1\\ -3 & 0\end{pmatrix}$ $\bar{U}_2 = \begin{pmatrix}0 & 6\\ 0 & 2\end{pmatrix}$

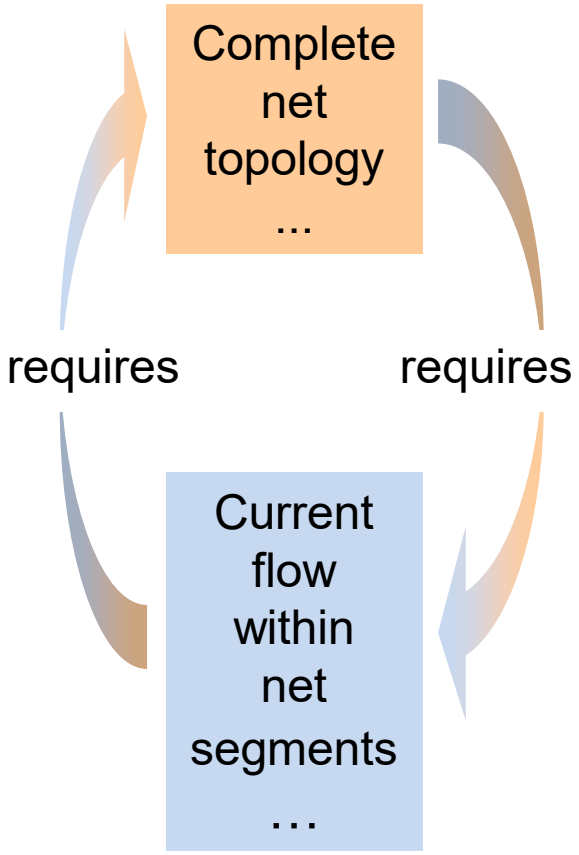
V_{T3}: $\bar{L}_3 = \begin{pmatrix}2 & -1\\ 0 & -3\end{pmatrix}$ $\bar{U}_3 = \begin{pmatrix}3 & 0\\ 2 & 3\end{pmatrix}$

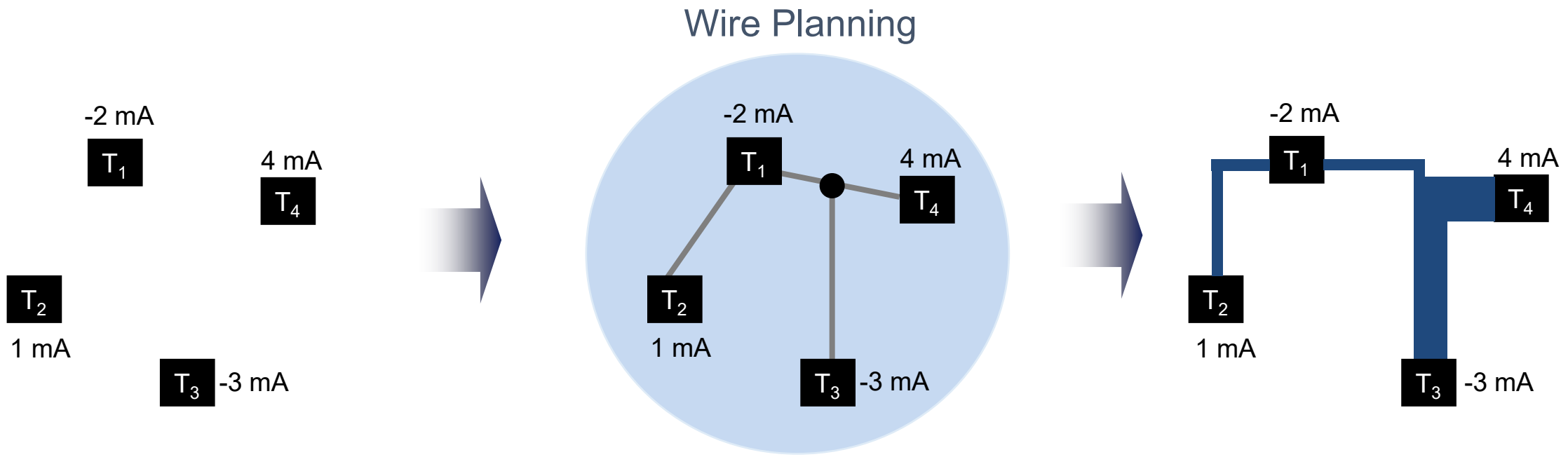
V_{T4}: $\bar{L}_4 = \begin{pmatrix}-2 & 1\\ -1 & -3\end{pmatrix}$ $\bar{U}_4 = \begin{pmatrix}-2 & 4\\ 1 & 0\end{pmatrix}$


-2 mA
T3
4 mA
T1
T4
1 mA
T2
-3 mA


-2 mA
1 mA
T3
4 mA
T1
3 mA
T4
1 mA
T2
-3 mA


-2 mA
2 mA
T3
4 mA
T1
2 mA
T4
1 mA
T2
-3 mA

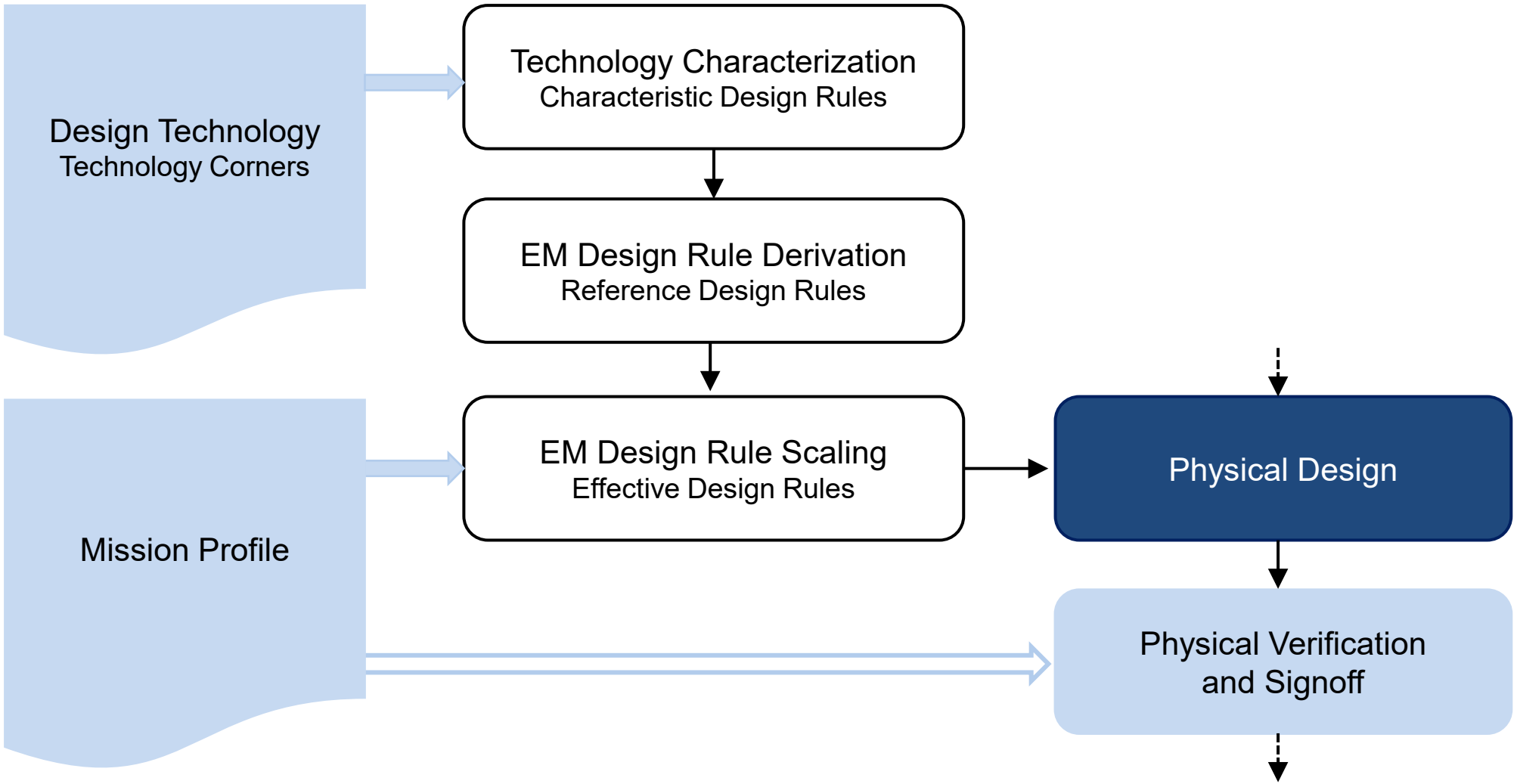

Complete net topology ...
requires
requires
Current flow within net segments ...

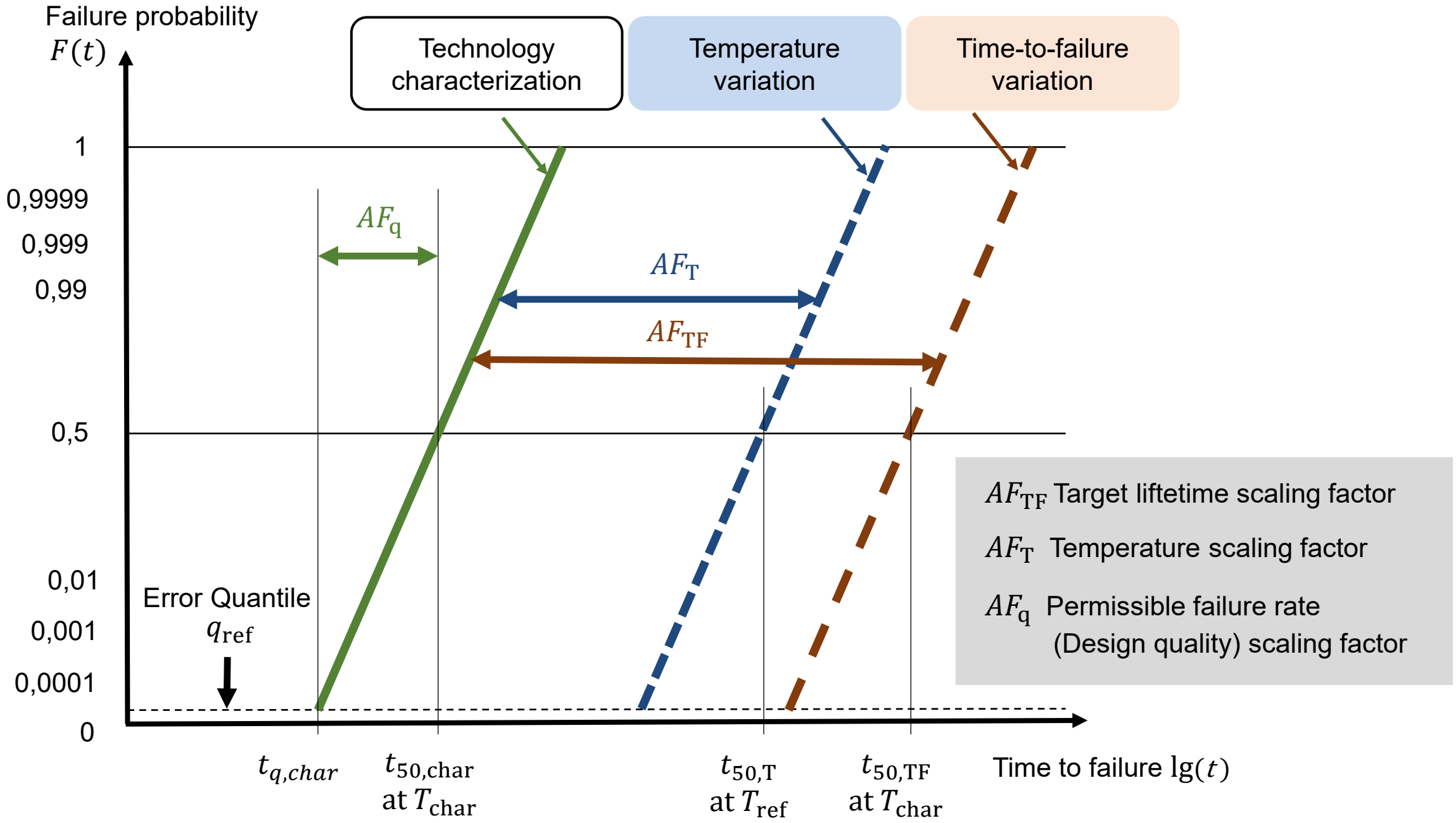


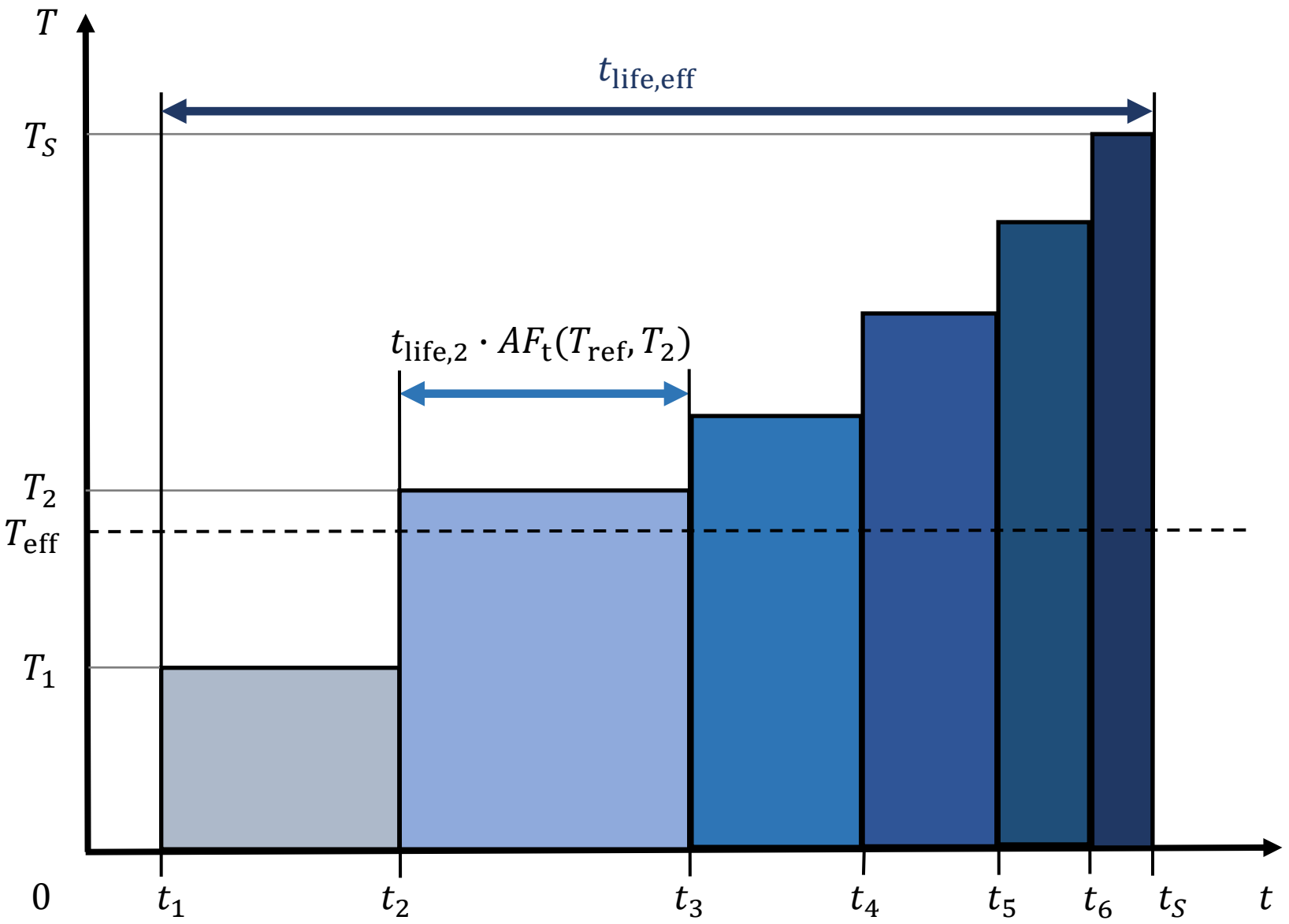
Given:
Net terminals with currents

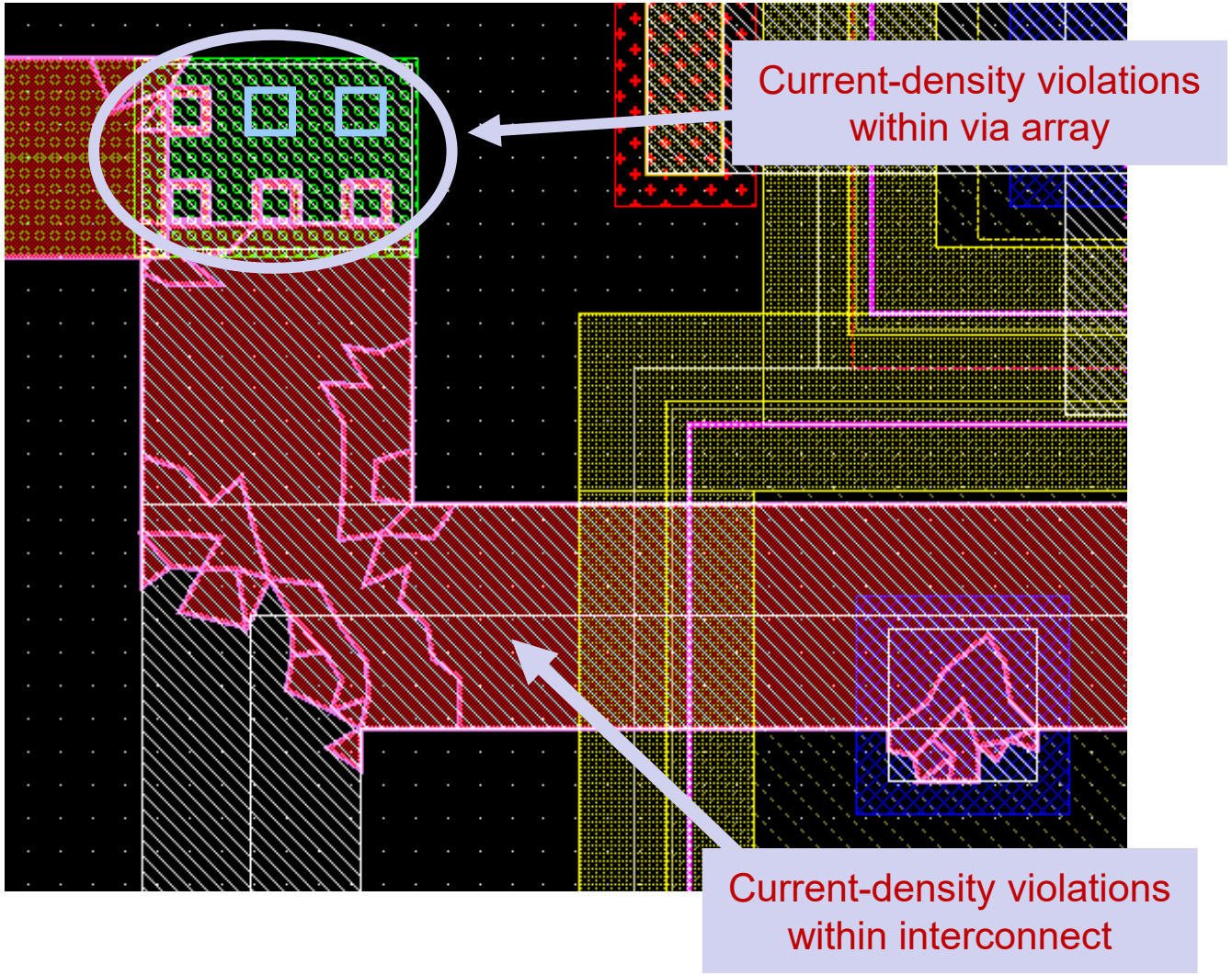
Wire planning objective:
Obtain a net topology with optimized current flow

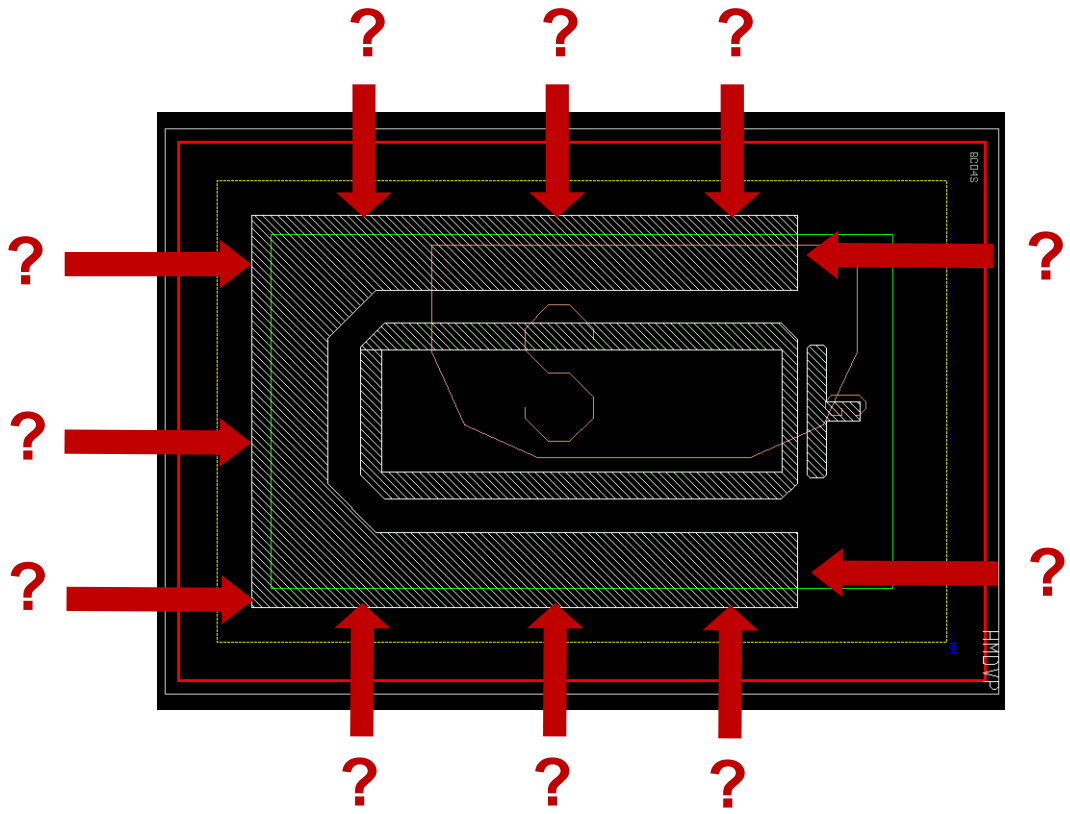
After routing:
Minimized interconnect area


Design Technology
Technology Corners
Technology Characterization
Characteristic Design Rules
EM Design Rule Derivation
Reference Design Rules
Mission Profile
EM Design Rule Scaling
Effective Design Rules
Physical Design
Physical Verification
and Signoff


Failure probability
$F(t)$
Technology characterization
Temperature variation
Time-to-failure variation
1
0,9999
0,999
0,99
0,5
0,01
0,001
0,0001
0
AF_q
AF_T
AF_{TF}
Error Quantile
q_{ref}
$t_{q,char}$
$t_{50,char}$ at T_{char}
$t_{50,T}$ at T_{ref}
$t_{50,TF}$ at T_{char}
Time to failure $\lg(t)$
AF_{TF} Target liftetime scaling factor
AF_T Temperature scaling factor
AF_q Permissible failure rate (Design quality) scaling factor


T
$t_{\text{life,eff}}$
T_S
$t_{\text{life,2}} \cdot AF_{\text{t}}(T_{\text{ref}}, T_2)$
T_2
T_{eff}
T_1
0
t_1
t_2
t_3
t_4
t_5
t_6
t_S
t


Current-density violations within via array
Current-density violations within interconnect


?
?
?
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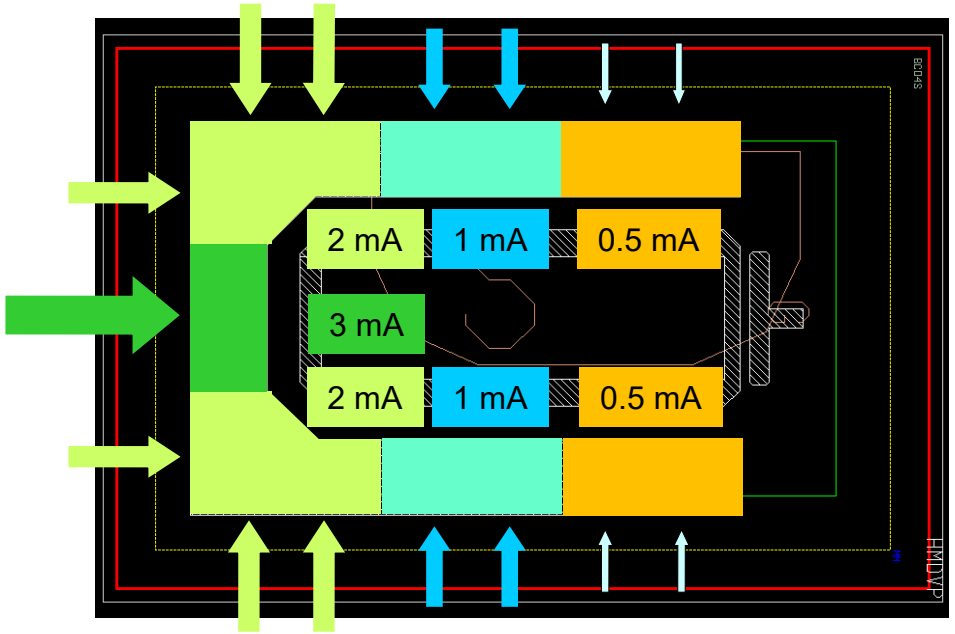
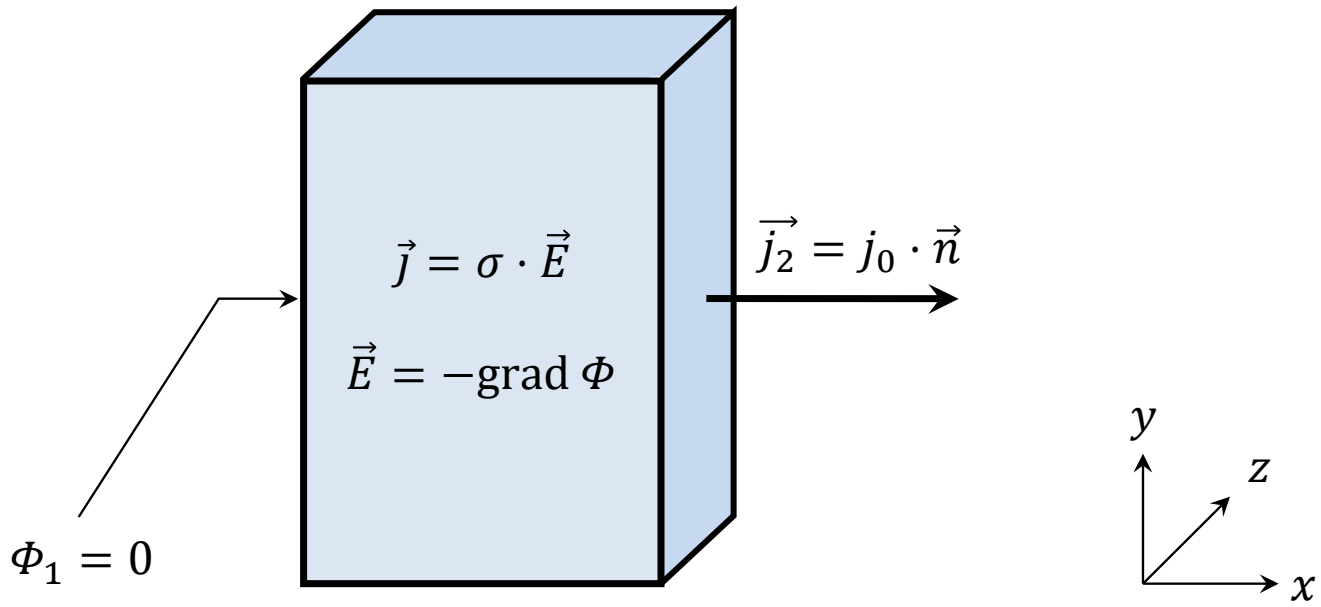
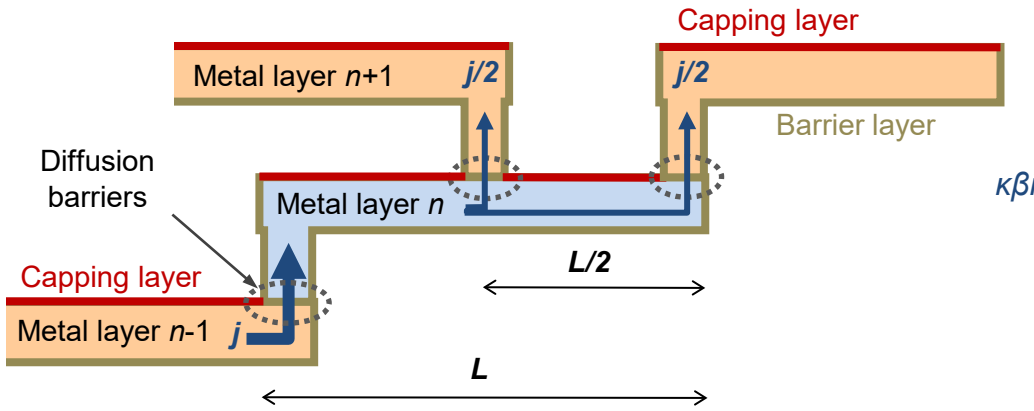
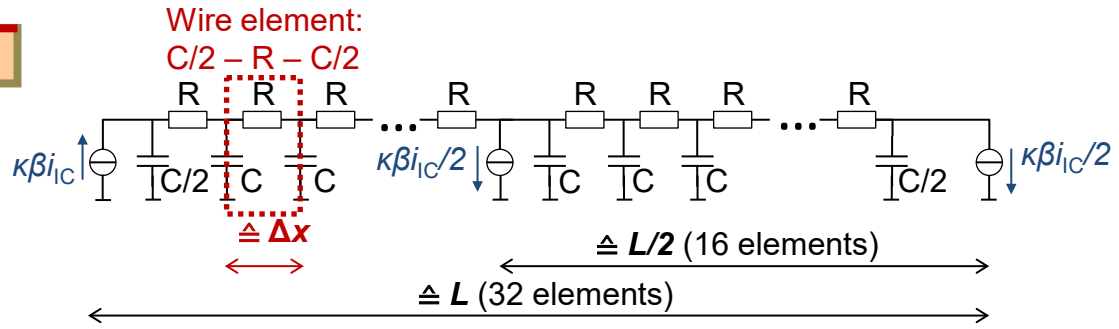
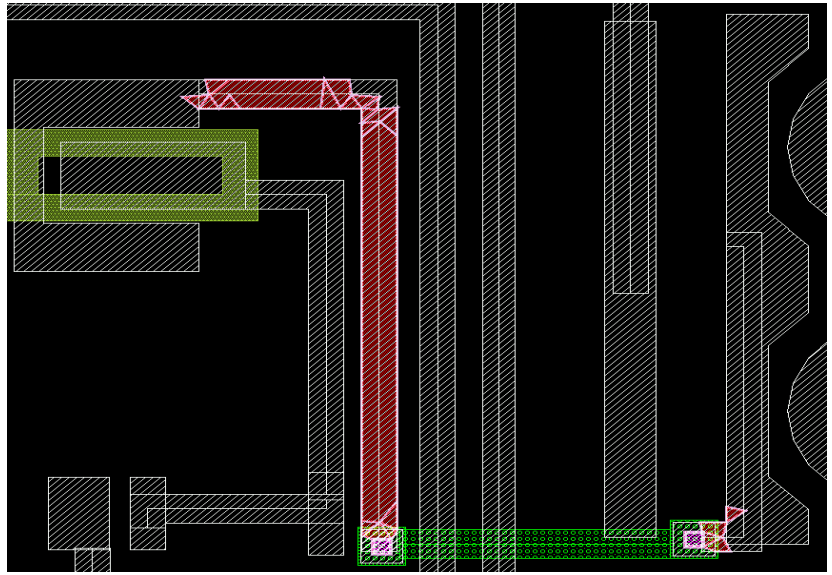
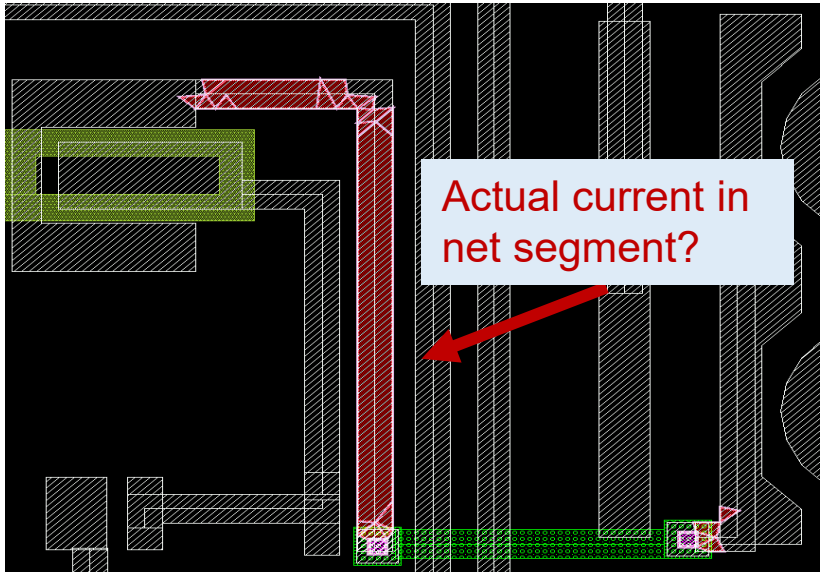

2 mA
1 mA
0.5 mA
3 mA
2 mA
1 mA
0.5 mA

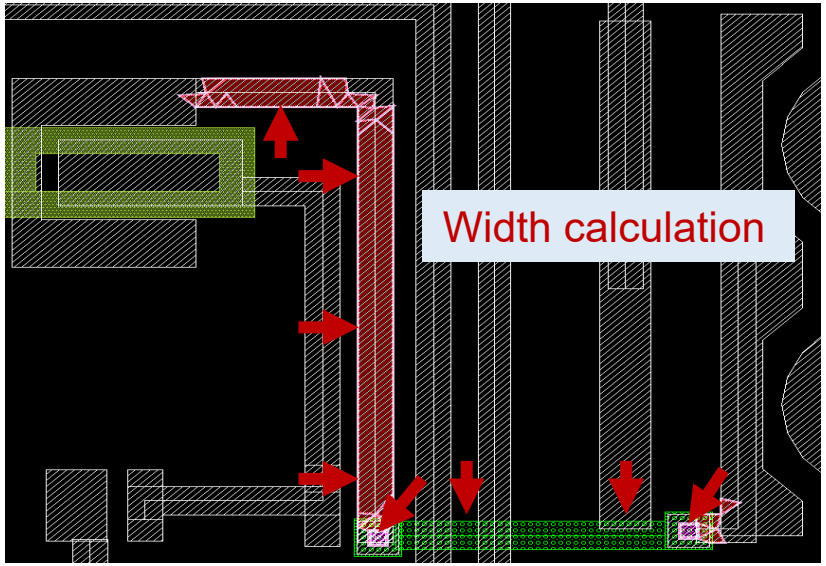

$\vec{j} = \sigma \cdot \vec{E}$
$\vec{E} = -\text{grad}\,\Phi$
$\overrightarrow{j_2} = j_0 \cdot \vec{n}$
$\Phi_1 = 0$
y
z
x

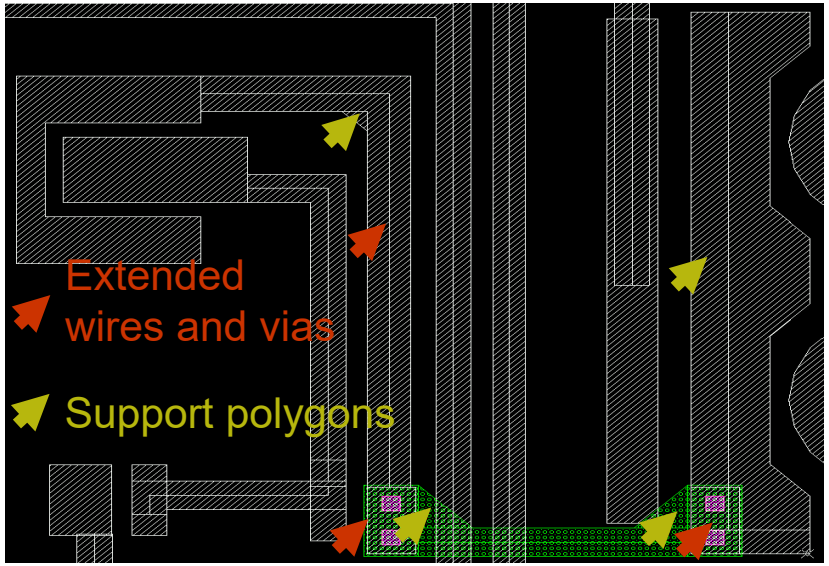

Capping layer
Metal layer n+1
j/2
j/2
Barrier layer
Diffusion
barriers
Metal layer n
L/2
Capping layer
Metal layer n-1
j
L


Wire element:
C/2 – R – C/2
R
R
R
R
R
R
R
R
κβi_IC
C/2
C
C
κβi_IC/2
C
C
C
C/2
κβi_IC/2
≙ Δx
≙ L/2 (16 elements)
≙ L (32 elements)




Actual current in
net segment?


Width calculation


Extended
wires and vias
Support polygons