5.5 Electromigration-Aware Design: Driven by Constraints

New challenges for IC design are appearing on the back of the ongoing trend in IC downscaling, i.e., structural miniaturization. Physical designs with ever-smaller feature sizes are subjected to an increasing number of more complex constraints due to these challenges. They are increasingly curtailing freedom in the design flow and are setting the boundaries of the ever-decreasing solution space. Hence, we are witnessing a slow, but steady evolution from a *constraint-correct* design flow to a *constraint-driven* one. With the latter, design algorithms and methodologies not only verify the correct implementation of constraints, but rather are governed by them.

One such challenge is EM. EM considerations are thus producing additional constraints in the design flow that are becoming the principal obstacles arising from progressive reductions in structure size. The resultant reduction in the available solution space for IC and routing design is illustrated in Fig. 5.2. Hence, a future distinction must be made between EM-robust and non-viable routing elements, ensuring that only EM-robust elements are used for routing. Consequently, constraint-driven routing is anticipated to dominate in the future.

This book has examined the underlying EM-inhibiting effects and proposed guidelines for creating routing elements that are more EM robust. The prospective rules for the constraint-driven design in general and, in particular, constraint-driven routing techniques can be derived from the presented guidelines. A feasible option to incorporate these constraints into any routing procedure is using current- and/or stress-dependent design rules.

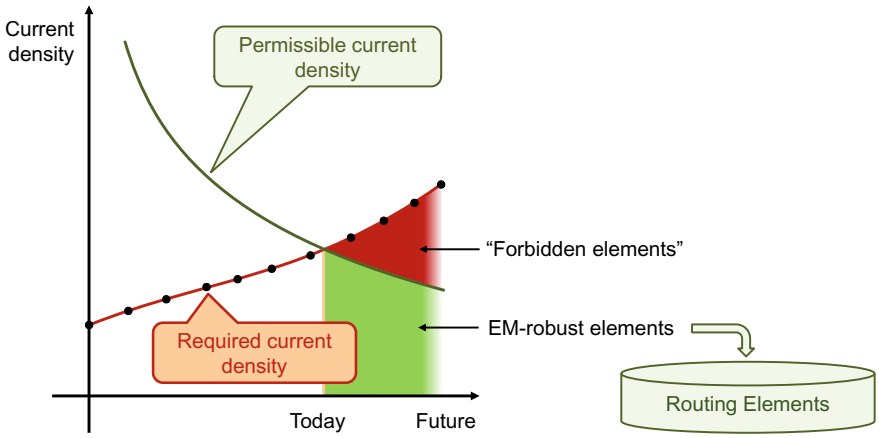

Fig. 5.2 Projected evolution of the routing solution space with falling current-density boundaries (green curve) and required current densities which are on the rise (red curve). The solution space for the allowed routing elements will be increasingly curtailed; hence, today's constraint-correct routing evolves into constraint-*driven* routing where only EM-robust elements (interconnect patterns) may be implemented in the chip's layout (see Fig. 5.1 for the generation of the routing elements)

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We expect that future, nanoscale design of *reliable* integrated circuits can only be achieved by applying the methodologies summarized in this final chapter and described in detail throughout this book.

Reference

[IRD] International Roadmap for Devices and Systems (IRDS), 2022. https://irds.ieee.org/editions/2022. Last retrieved on 1 Jan 2025