Chapter 3: Bridges to Technology: Interfaces, Design Rules, and Libraries

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- Specification
  - Design data
- Circuit Design
  - Circuit data (Sect. 3.1)
- Physical Design and Verification
  - Layout data (Sect. 3.2)
- Layout Post Processing (Sect. 3.3)
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- Fabrication

Technology data

Design data

Geometrical design rules (Sect. 3.4)

Libraries (Sect. 3.5)
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Pin-oriented netlist

(A: \textbf{Net1})
(B: Net2)
(C: Net5)
(NAND[1]: IN1 \textbf{Net1}, IN2 Net2, OUT Net3)
(NAND[2]: IN1 \textbf{Net1}, IN2 Net2, OUT Net4)
(NOR[1]: IN1 Net3, IN2 Net4, OUT Net5)

Net-oriented netlist

(\textbf{Net1}: A, NAND[1].IN1, NAND[2].IN1)
(\textbf{Net2}: B, NAND[1].IN2, NAND[2].IN2)
(\textbf{Net3}: NAND[1].OUT, NOR[1].IN1)
(\textbf{Net4}: NAND[2].OUT, NOR[1].IN2)
(\textbf{Net5}: NOR[1].OUT, C)
.SUBCKT bgap Ibias VDD VSS bg
QQ1 VSS VSS net05 vpnp M=1 EA=1.69
QQ0 VSS VSS net04 vpnp M=8 EA=1.69
XI0 Ibias VDD VSS net05 net01 net02 / moa
MPM1 bg net02 VDD VDD pmos W=8u L=4u M=2
MPM0 net03 net02 VDD VDD pmos W=8u L=4u M=2
RR2 net03 net05 45.05k polyhres W=2u L=255u
RR1 bg net01 45.05k polyhres W=2u L=255u
RR0 net01 net04 5.3k polyhres W=2u L=30u
.ENDS
.SUBCKT moa ibias VDD VSS inn inp out
MPM4 ibias ibias VDD VDD pmos W=6u L=2u M=2
MPM3 out ibias VDD VDD pmos W=6u L=2u M=6
MPM0 net03 inp net02 VDD pmos W=50u L=4u M=2
MPM1 net01 inn net02 VDD pmos W=50u L=4u M=2
MPM2 net02 ibias VDD VDD pmos W=6u L=2u M=2
MNM2 out net03 VSS VSS nmos W=12u L=2u M=6
MNM1 net01 net01 VSS VSS nmos W=12u L=2u M=2
MNN0 net03 net01 VSS VSS nmos W=12u L=2u M=2
CC0 net03 out 635f mimcap M=2
.ENDS
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Layout

Sectional view

Circuit diagram
\[ x = \text{blue OR red} \]
\[ x = \text{blue AND red} \]
\[ x = \text{blue XOR red} \]
\[ x = \text{red ANDNOT blue} \]
\[ x = \text{blue ANDNOT red} \]
Sizing without beveling

Sizing with beveling
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(a) Original \[\rightarrow\] (1) Undersize \[\rightarrow\] (2) Oversize

(b) Original \[\rightarrow\] (1) Oversize \[\rightarrow\] (2) Undersize

(c) Original \[\rightarrow\] Oversize \[\rightarrow\] Undersize

Deviation from original
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(a) Dishing  (b) Too much erosion  (c) Desired erosion  (d) Too little erosion

Pre-CMP level

(a) Dishing  (b) Too much erosion  (c) Desired erosion  (d) Too little erosion

Pre-CMP level

Slotting  Metal lines homogenously spread  Dummy fill structures

Pre-CMP level
Scribe lines with test patterns for process monitoring

Die

Die

Die

Die

Die

Die

Alignment marks

Logo

Layer revisions

Scribe monitor structure

Scribe lines with test patterns of electrical components
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Layout data

NSD
Active
Poly
n-Active

PSD
Active
Nwell
p-Active

Mask data

Layout Post Process A

Layout Post Process B
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(a) Res Poly

(b) Text Poly

(c) Polyres
<table>
<thead>
<tr>
<th>Design Rule</th>
<th>Relationship between edges</th>
<th>Number of shapes</th>
<th>Number of layers</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Width</strong></td>
<td>Inside / inside</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td><strong>Spacing</strong></td>
<td>Outside / outside</td>
<td>(a) 1 or 2</td>
<td>(a) 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(b) 2</td>
<td>(b) 2</td>
</tr>
<tr>
<td><strong>Extension</strong></td>
<td>Inside / outside</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td><strong>Intrusion</strong></td>
<td>Inside / inside</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td><strong>Enclosure</strong></td>
<td>Outside / inside</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Width</td>
<td>Spacing</td>
<td>Extension</td>
<td>Intrusion</td>
</tr>
<tr>
<td>---------------</td>
<td>------------------------------</td>
<td>-----------</td>
<td>-----------</td>
</tr>
<tr>
<td>Design rule checked</td>
<td><img src="image1" alt="Width Design Rule Checked Diagrams" /></td>
<td><img src="image2" alt="Spacing Extension Diagrams" /></td>
<td><img src="image3" alt="Intrusion Diagrams" /></td>
</tr>
</tbody>
</table>

| Design rule not checked | ![Width Design Rule Not Checked Diagrams](image5) | ![Spacing Intrusion Diagrams](image6) | ![Enclosure Diagrams](image7) |

No errors can occur
Error-free layout with non-robust rules can cause **non-robust layout**
- Minimum width
- Minimum spacing

Error-free layout with robust rules guarantees **robust layout**
- Minimum width
- Minimum spacing

Manufacturing tolerance
- Break
  - No break

Manufacturing tolerance
- Short-circuit
  - No short-circuit

**Metal1**
Error-free layout with non-robust rules can cause **non-robust layout**

- Misaligned NSD mask
  - Short between S/D and p-substrate
- Misaligned Poly mask
  - Source to drain short
- Misaligned Metal1 mask
  - Bad/missing contacts

Error-free layout with robust rules guarantees **robust layout**

- Extension Poly Active
  - No short
- Enclosure Metal1 Cont
  - Good contacts
- Enclosure NSD Active

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[NSD Poly Cont Metal1 diagram]
X1 = Active ANDNOT Poly
X2 = X1 ANDNOT Cont
X3 = SIZE (X2, -clear)
Result = SIZE (X3, +clear)
Mold compound  
Die  
Lead frame  
Bonding wire  
Package leads
Lead frame
Forbidden area for bond pads
Contact points on the lead frame
Bonding wire
Bond pad
Bonding-wire angle
entity NOR2 is
  port(IN1: in std_logic;
       IN2: in std_logic;
       OUT: out std_logic);
end entity NOR2;

architecture RTL is
  begin
    OUT <= NOT(IN1 OR IN2);
  end architecture RTL;
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D-type flip flop w/ reset: D_FF_R
D-type flip flop w/ reset/set: D_FF_RS
D-type flip flop w/ reset and scan input: D_FF_R_SC
D-type latch w/ reset: LD_R
D-type latch w/ reset and scan input: LD_R_SC
Bus keeper flip flop: BK

NAND gate: NAND2, NAND3 ...
NOR gate: NOR2, NOR3 ...
AND gate: AND2
OR gate: OR2
Inverter: INV, INV_2X, INV_4X
Buffer: BUF_4X, BUF_16X ...
Tristate buffer: TRI_BUF_8X
XOR gate: XOR2
Multiplexer: MUX21, MUX41

Combinatorial (gates)

Memory (flip flops, latches)
Symbol library name
Symbols in this library
Selected symbol
Symbol editor
Pin names, pin assignment
Reference to footprint
Footprint Library

Example.fplib

Components
Name | Pads | Primitives
-----|------|--------
SOIC-8 (RN-8) | 8 | 15
SOT23-5 (RJ-5) | 5 | 12
SSOP16 (GN) | 16 | 24

Component Primitives
Type | Name | X-Size | Y-Size | Layer
------|------|--------|--------|------
ARC | 0.2mm | TopOverlay
Track | 0.2mm | TopOverlay
Track | 0.2mm | TopOverlay
Pad 1 | 1mm | 0.5mm | Top Layer
Pad 2 | 1mm | 0.5mm | Top Layer
Pad 3 | 1mm | 0.5mm | Top Layer
Pad 4 | 1mm | 0.5mm | Top Layer

Footprint library name
Footprints in this library
Footprint editor
Selected footprint
Constituting elements of the footprint
Model Library

.model 1N4001 D
+Is=14.11n N=1.984 Rs=33.89m Ikf=94.81
+xTi=3 Eg=1.11 CJo=25.89p M=.44
+VJ=.3245 Fc=.5 By=.75 IbV=.10u Tt=5.7u
+Iave=1 Vpk=50 mfg=GI type=silicon

Model name
Model category (diode)
Device specific parameter set