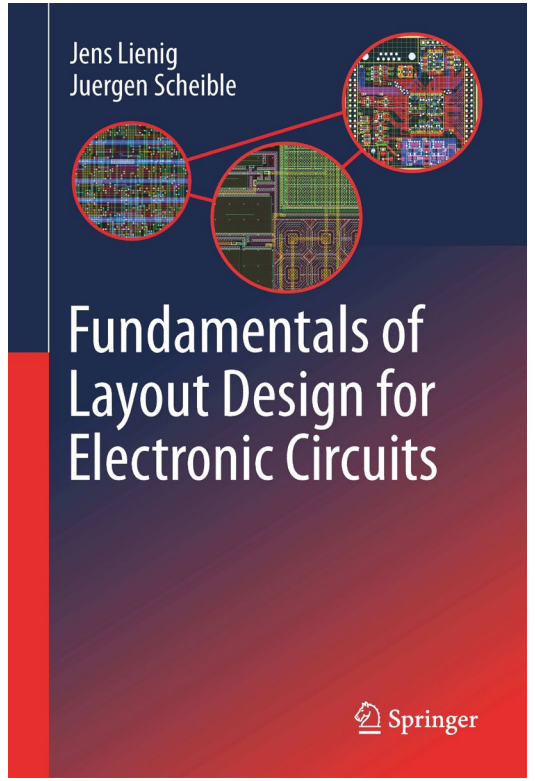
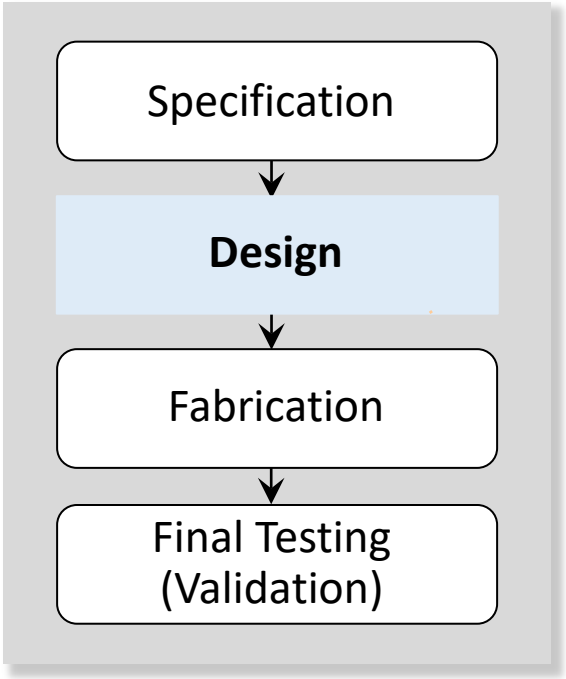
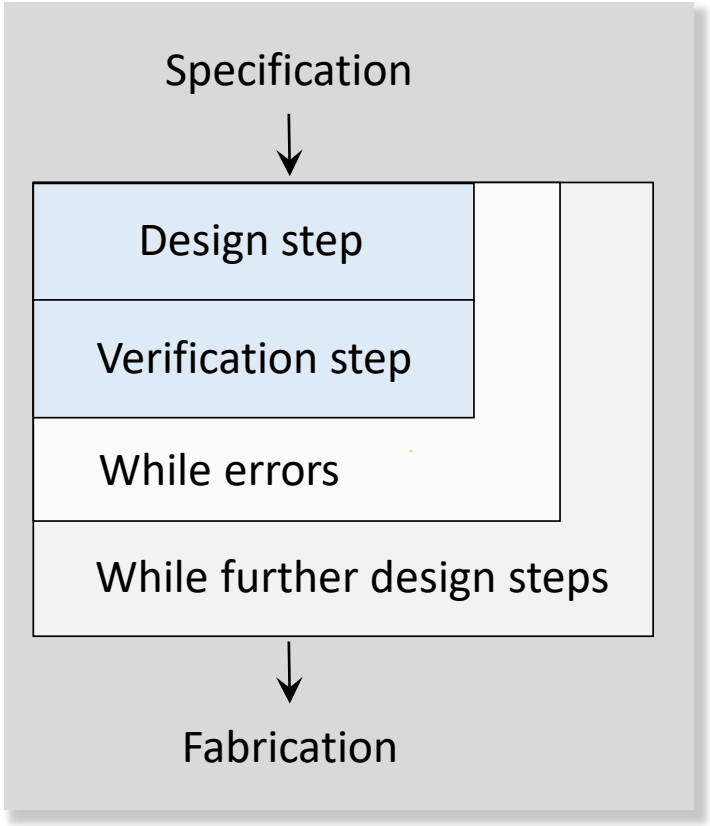
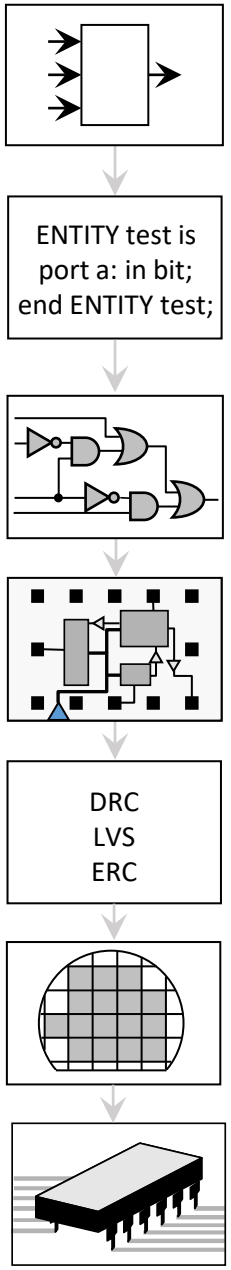
Chapter 4: Methods for Physical Design: Models, Styles, Tasks, and Flows



Chapter 4: Methods for Physical Design: Models, Styles, Tasks, and Flows







System Specification

Architectural Design

Functional Design and Logic Design

Circuit Design

Physical Design

Physical Verification

Layout Post Processing

Fabrication

Packaging and Testing

Partitioning

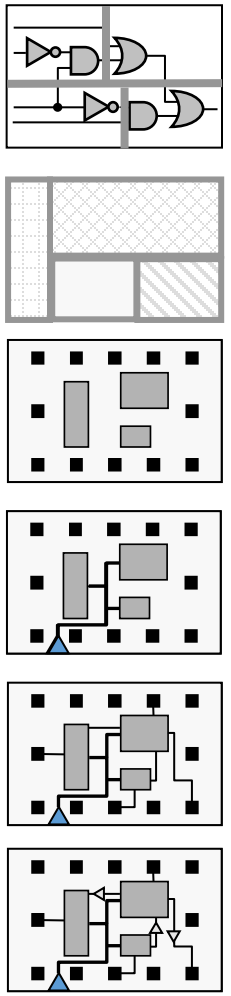
Floorplanning

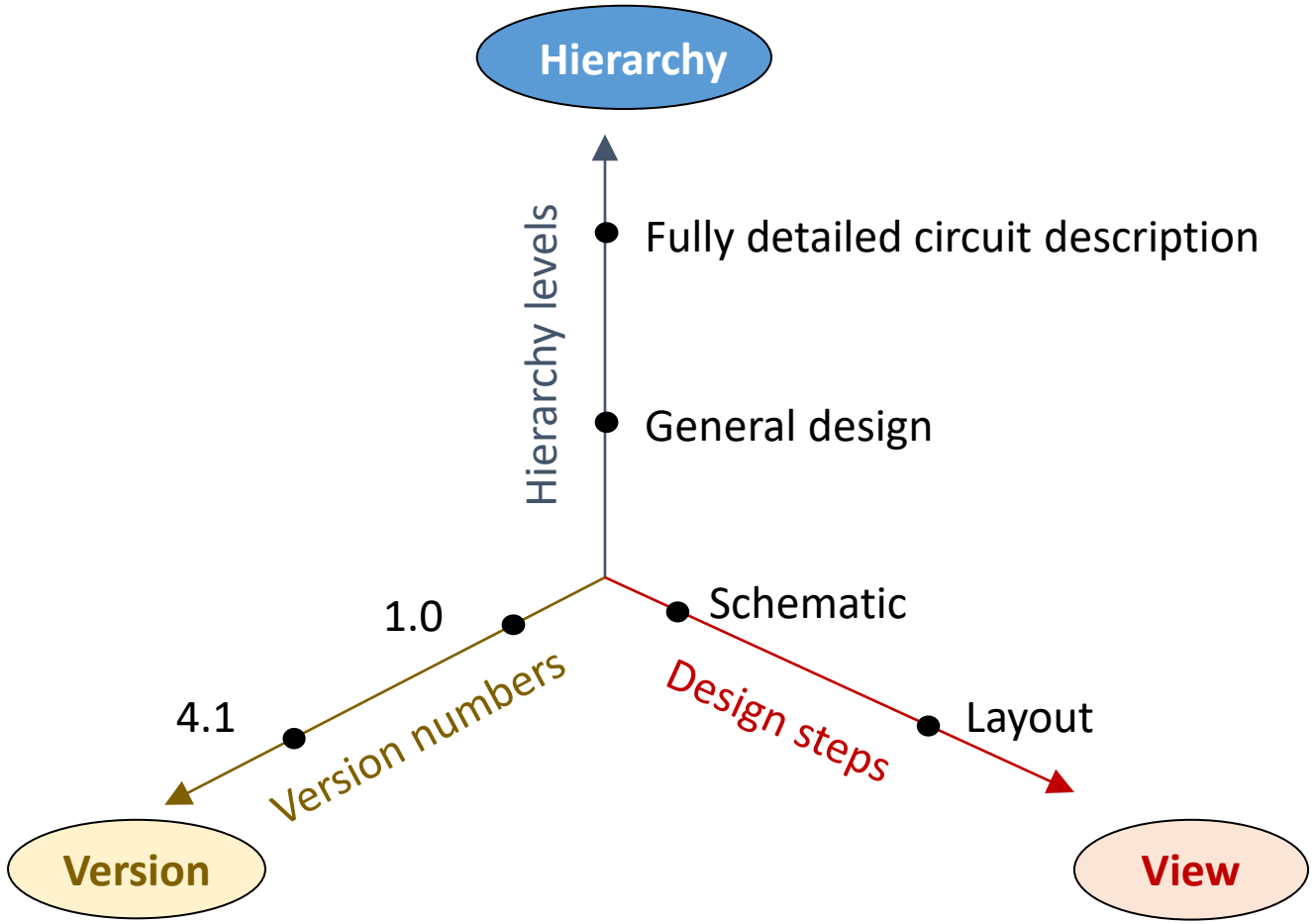
Placement

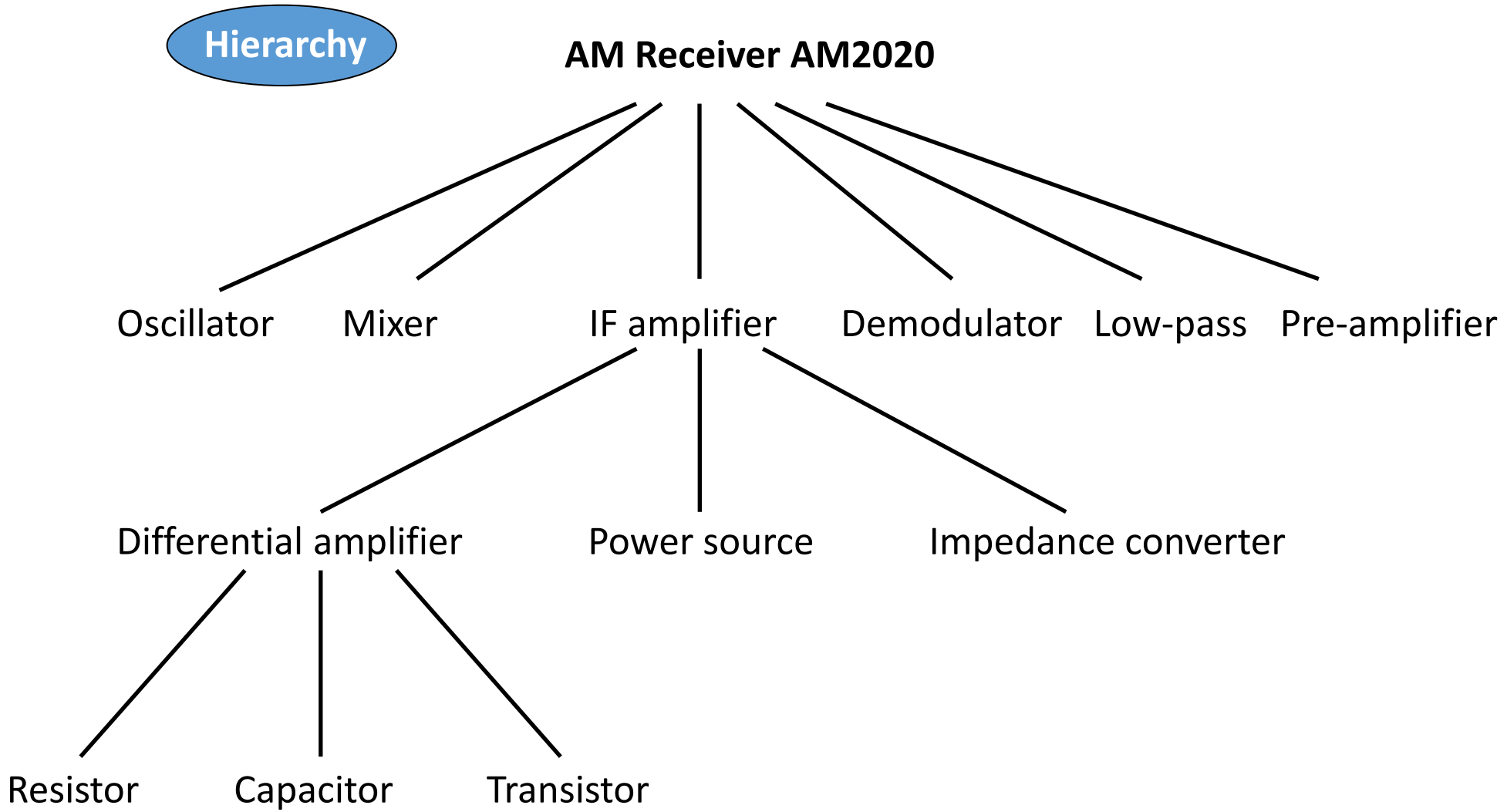
Clock Tree Synthesis

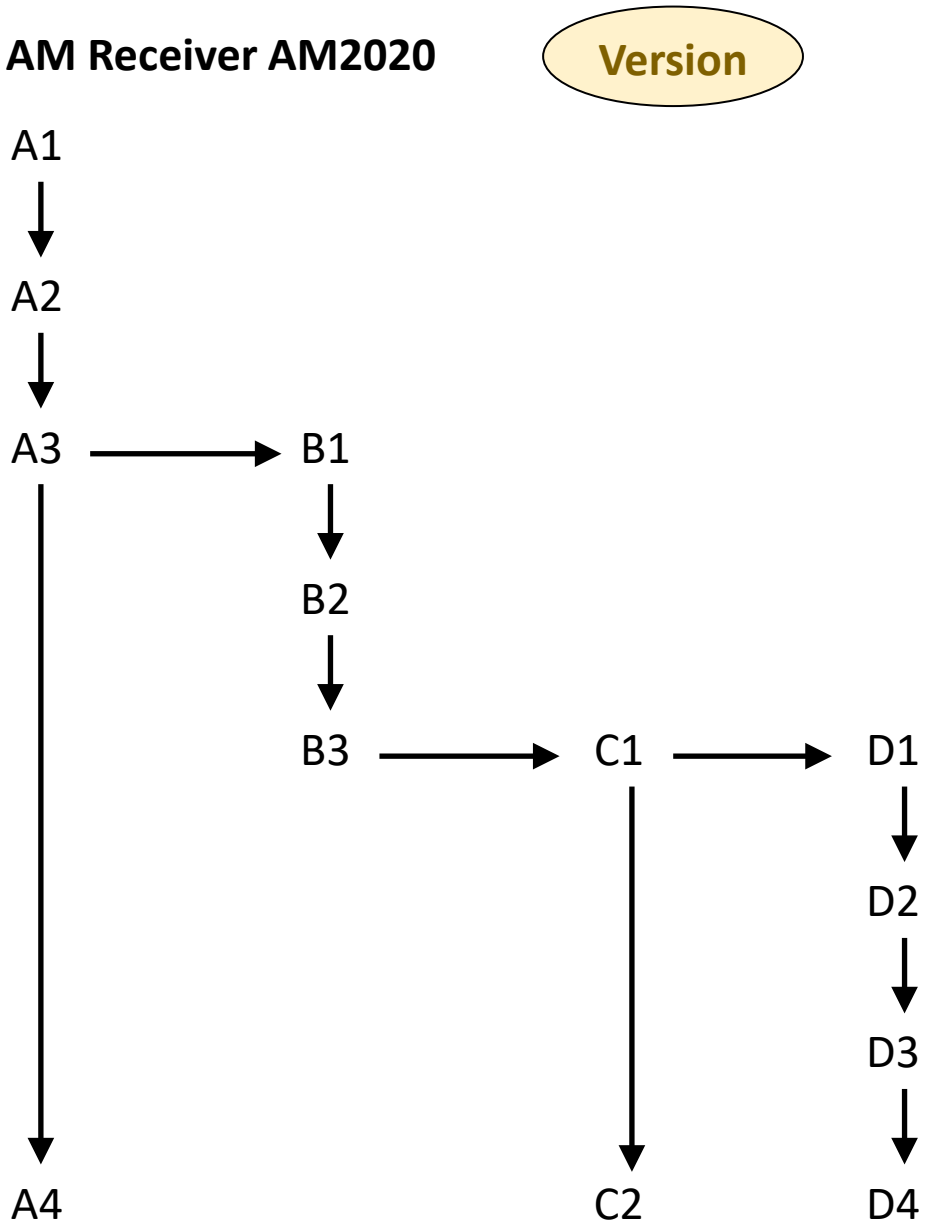
Signal Routing

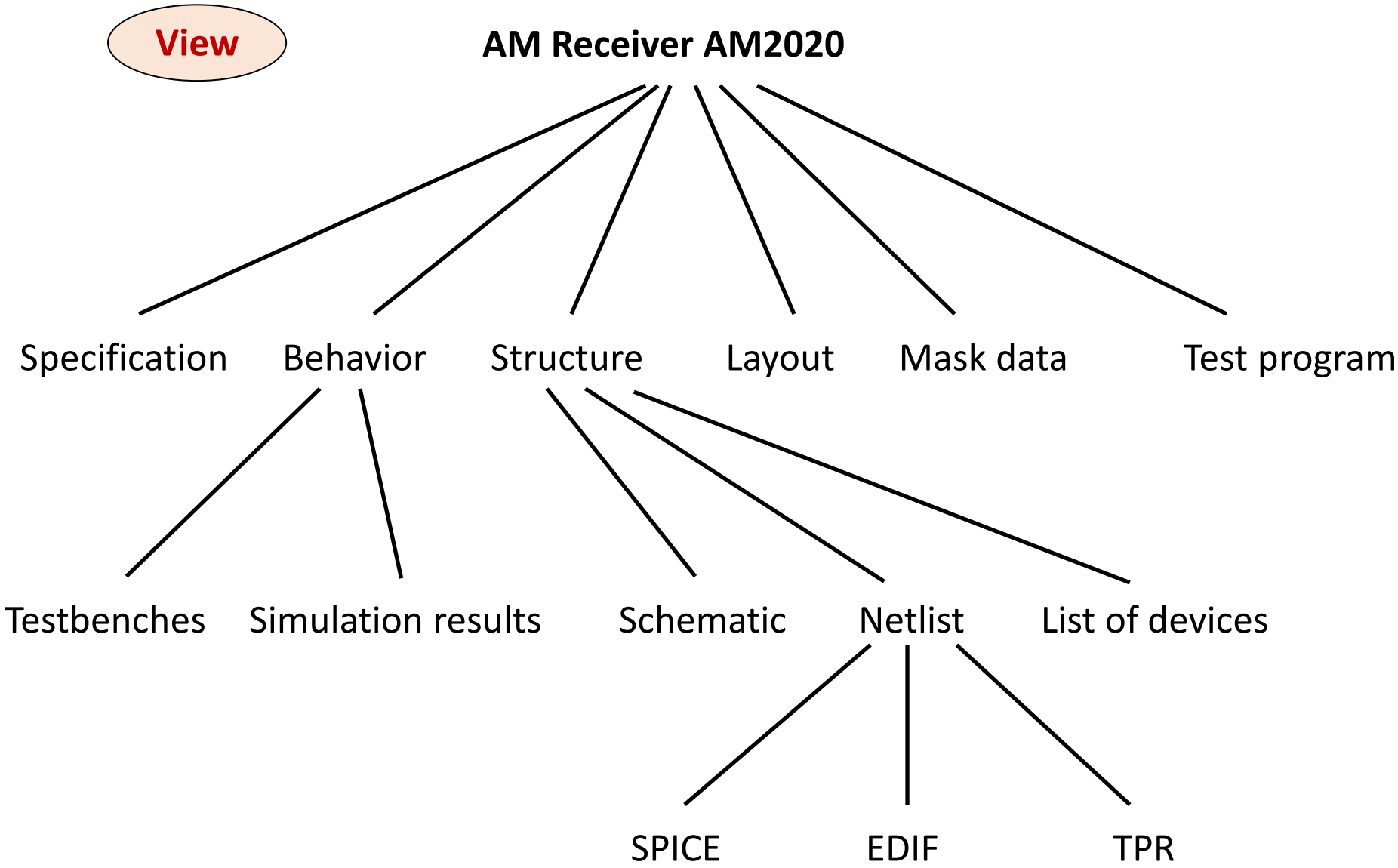
Timing Closure

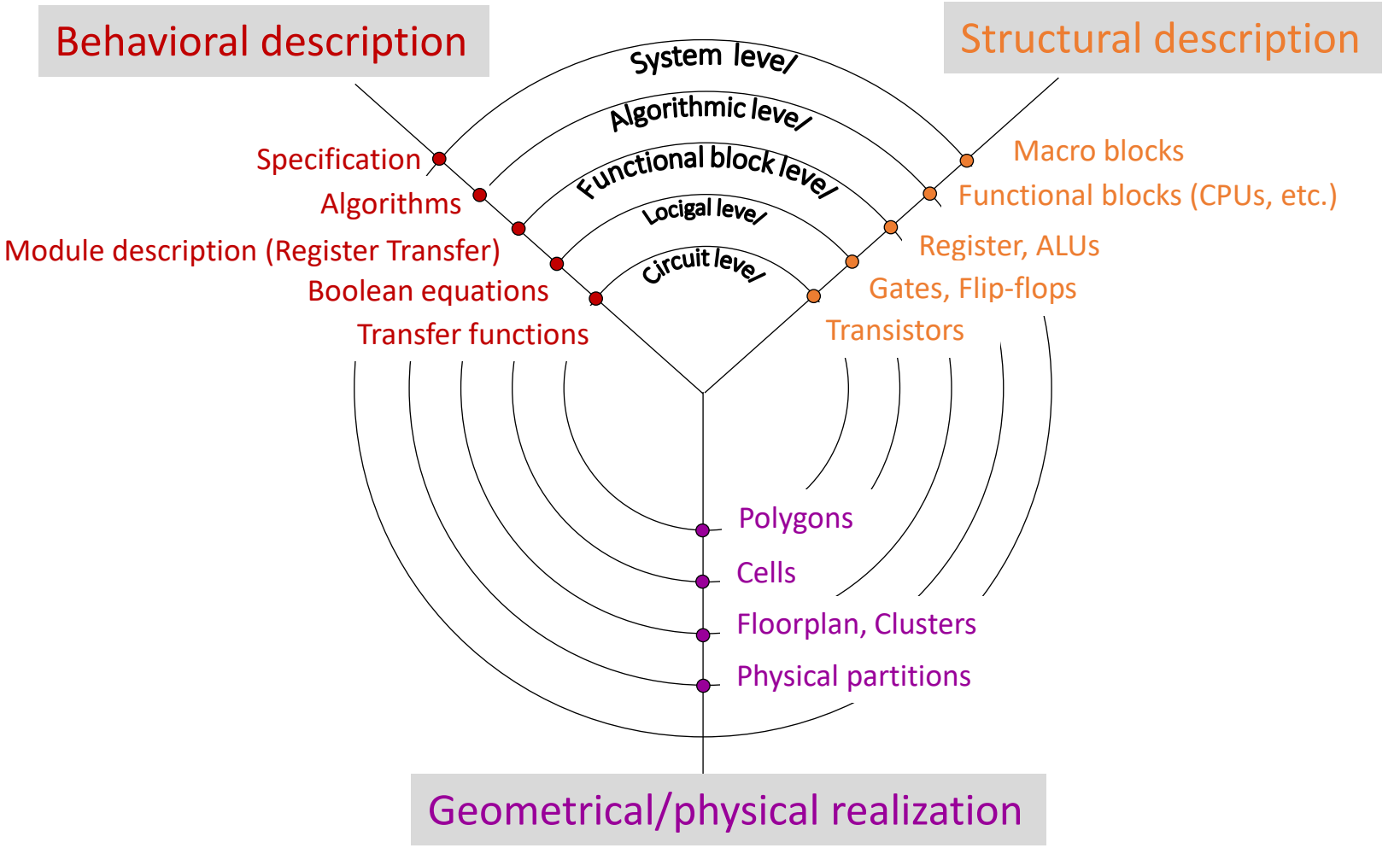








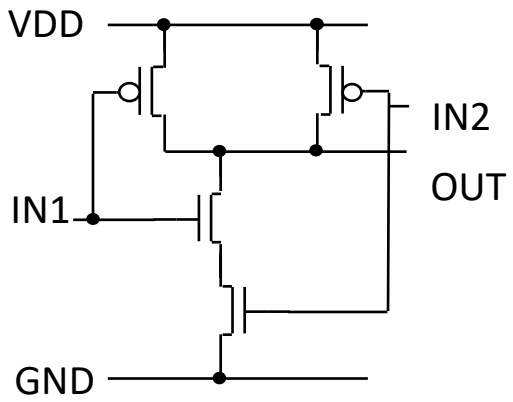




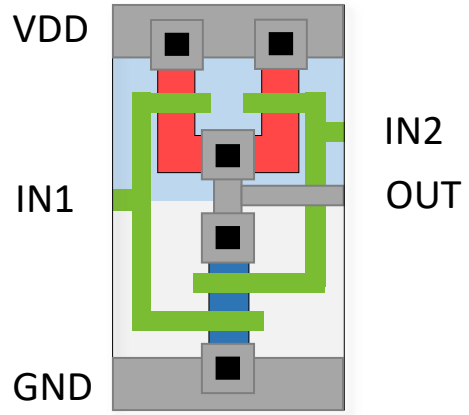
Behavioral description

IN1	IN2	OUT
0	0	1
0	1	1
1	0	1
1	1	0

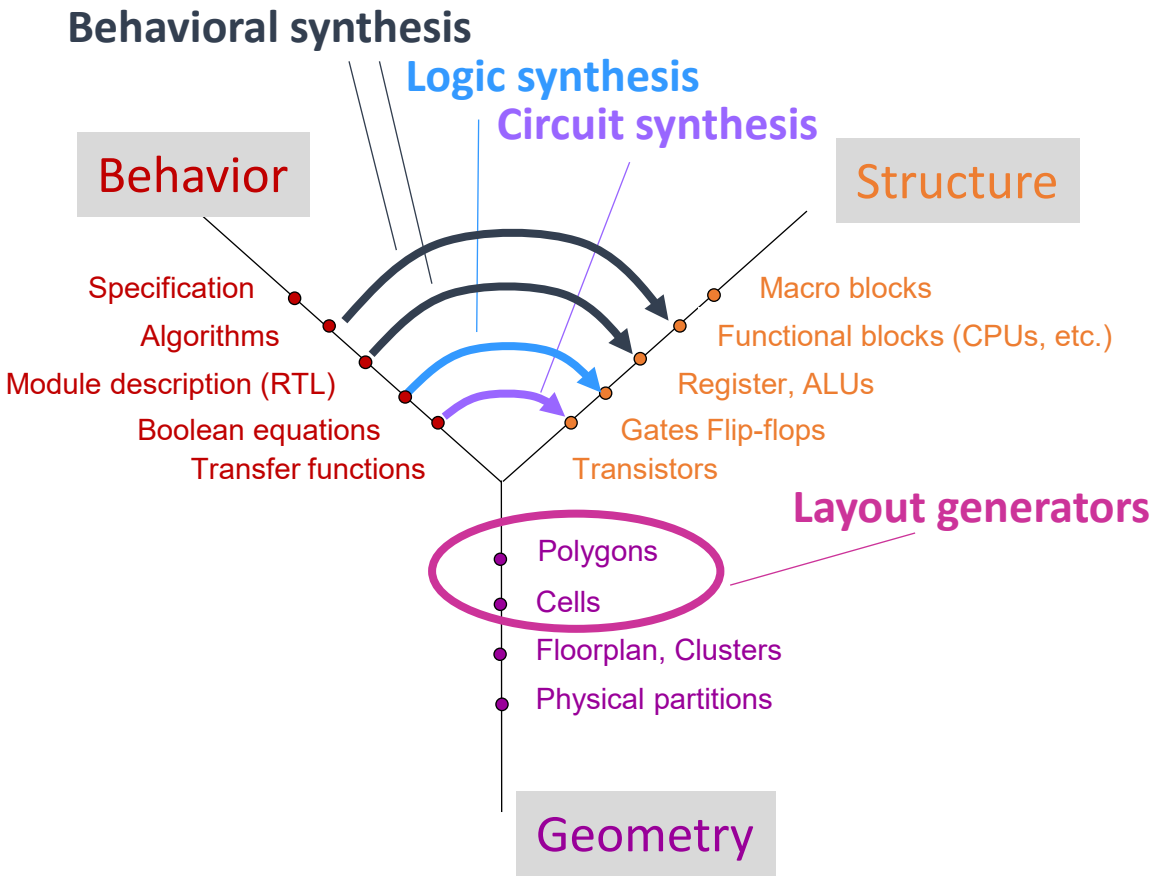
Structural description

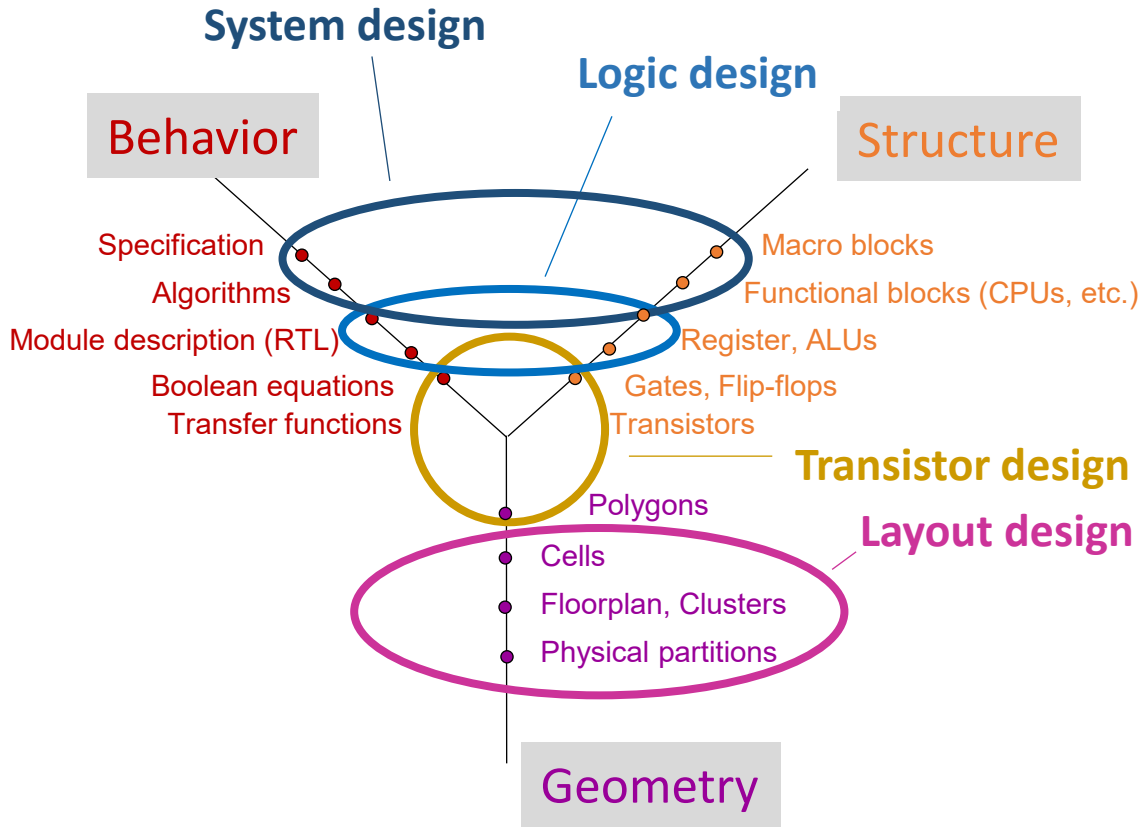


Geometrical/physical realization

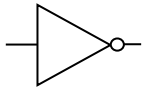


NAND gate 



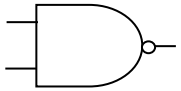


INV



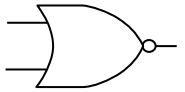
IN	OUT
0	1
1	0

NAND

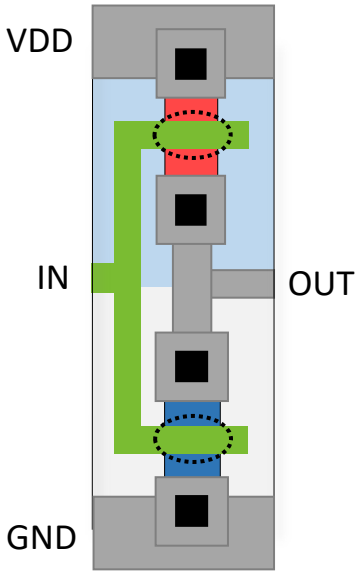


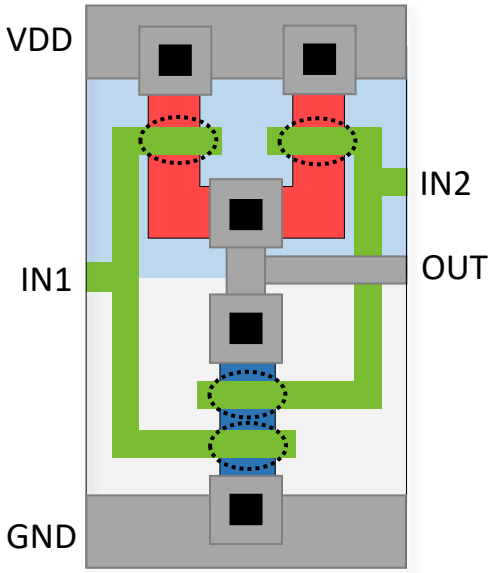
IN1	IN2	OUT
0	0	1
1	0	1
0	1	1
1	1	0

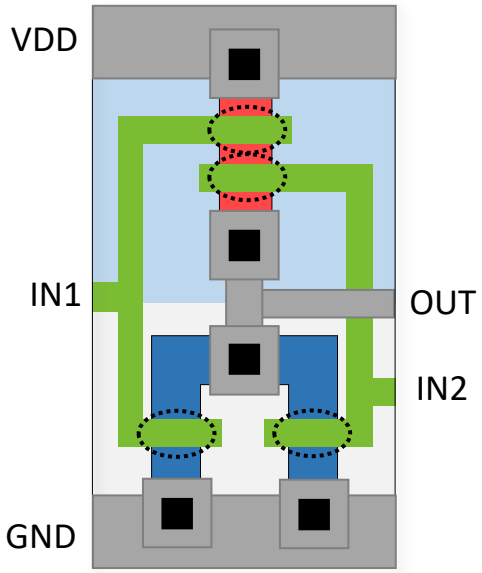
NOR

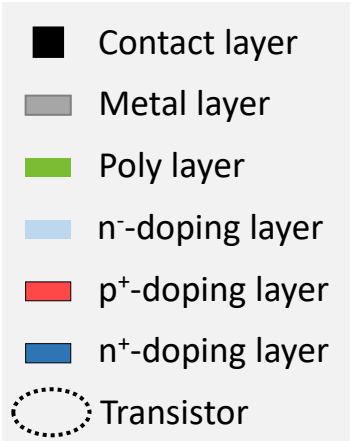


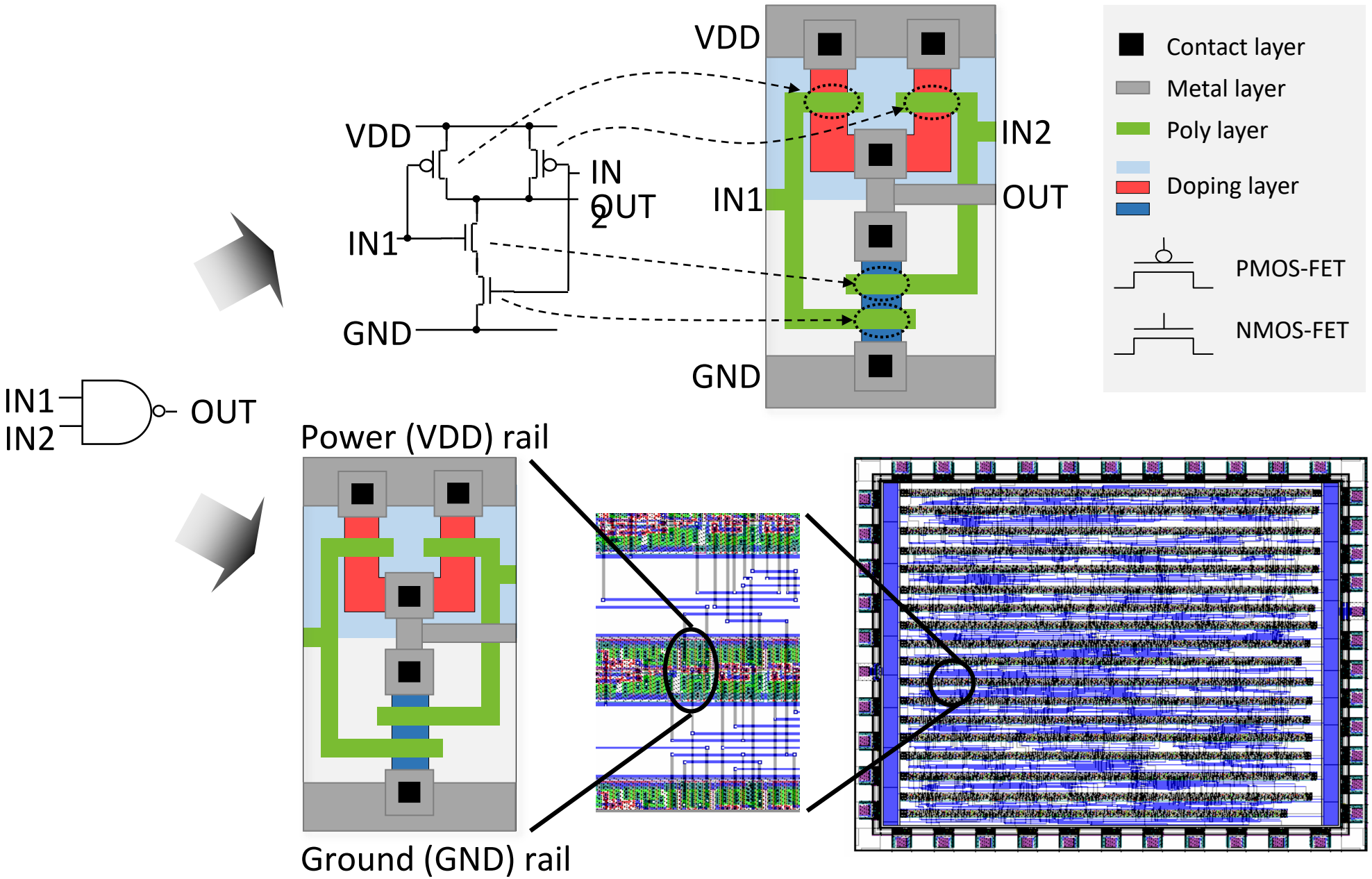
IN1	IN2	OUT
0	0	1
1	0	0
0	1	0
1	1	0

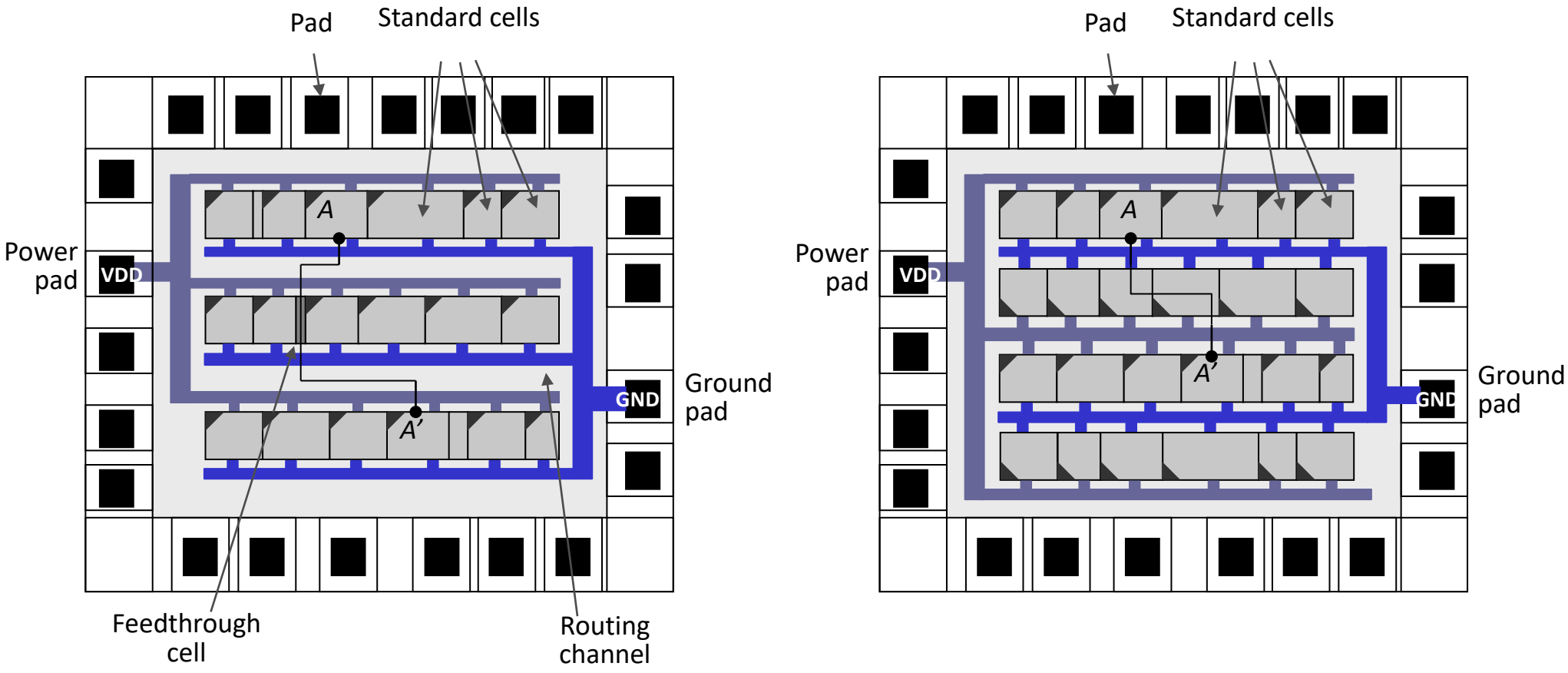


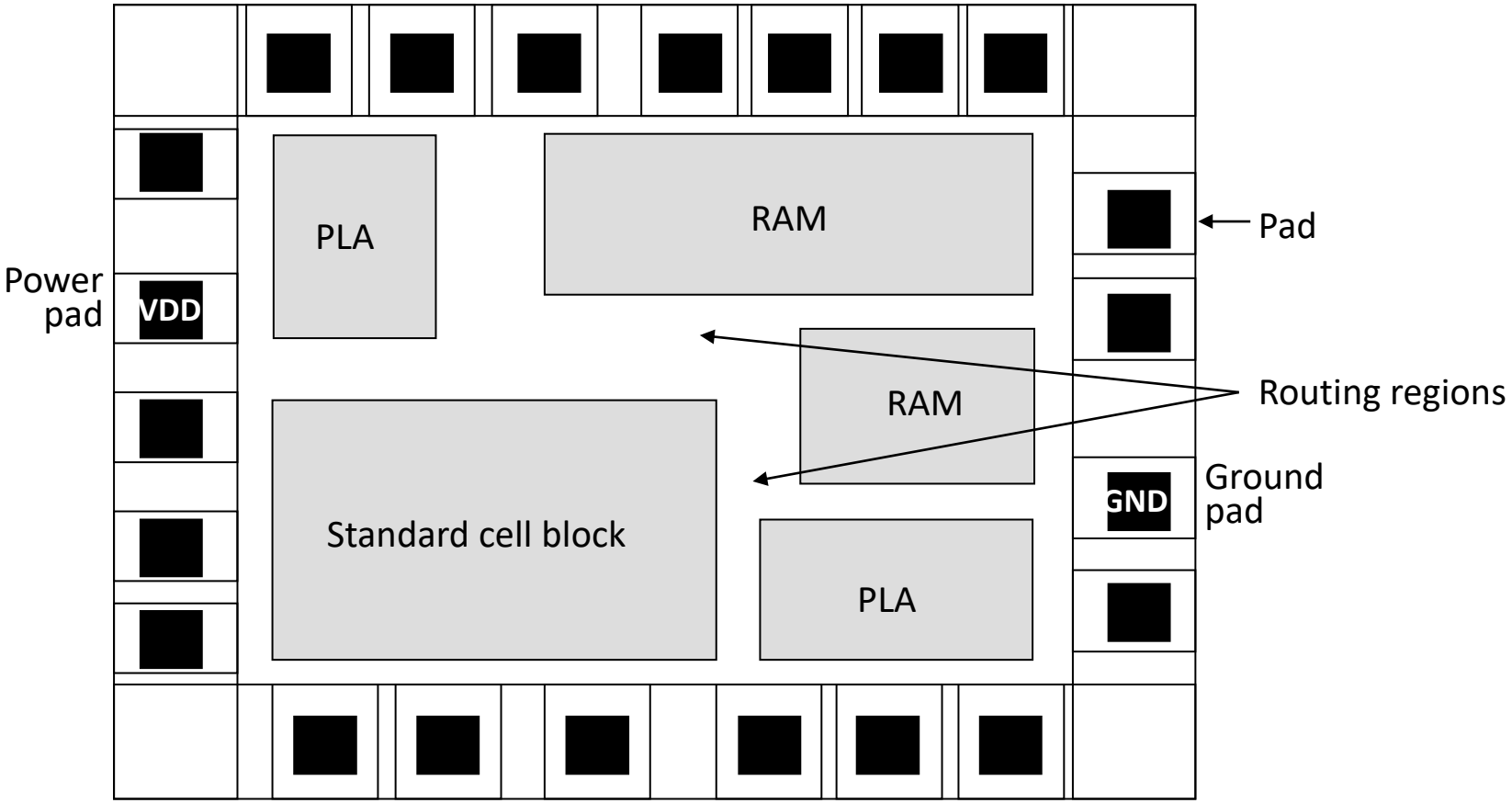


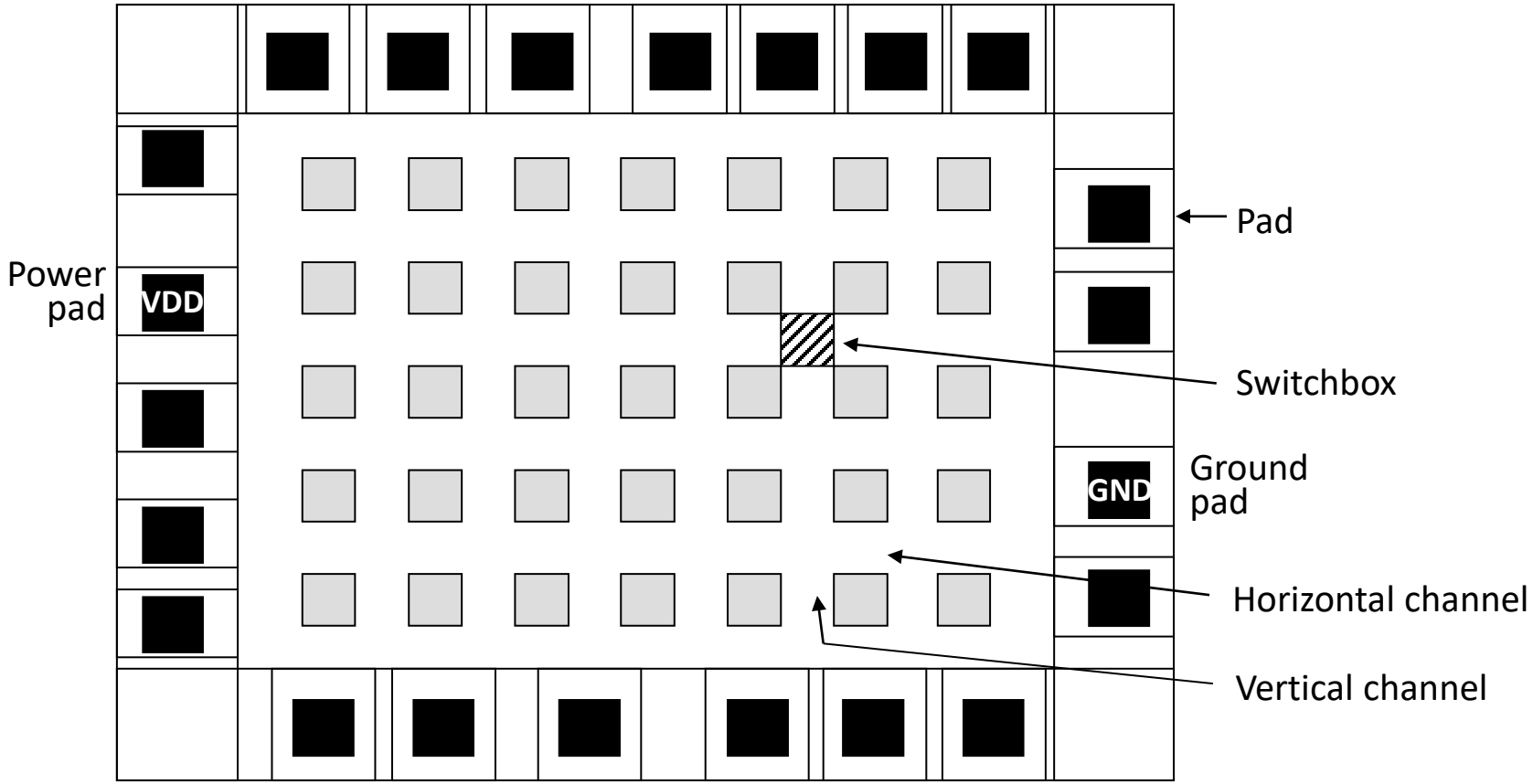


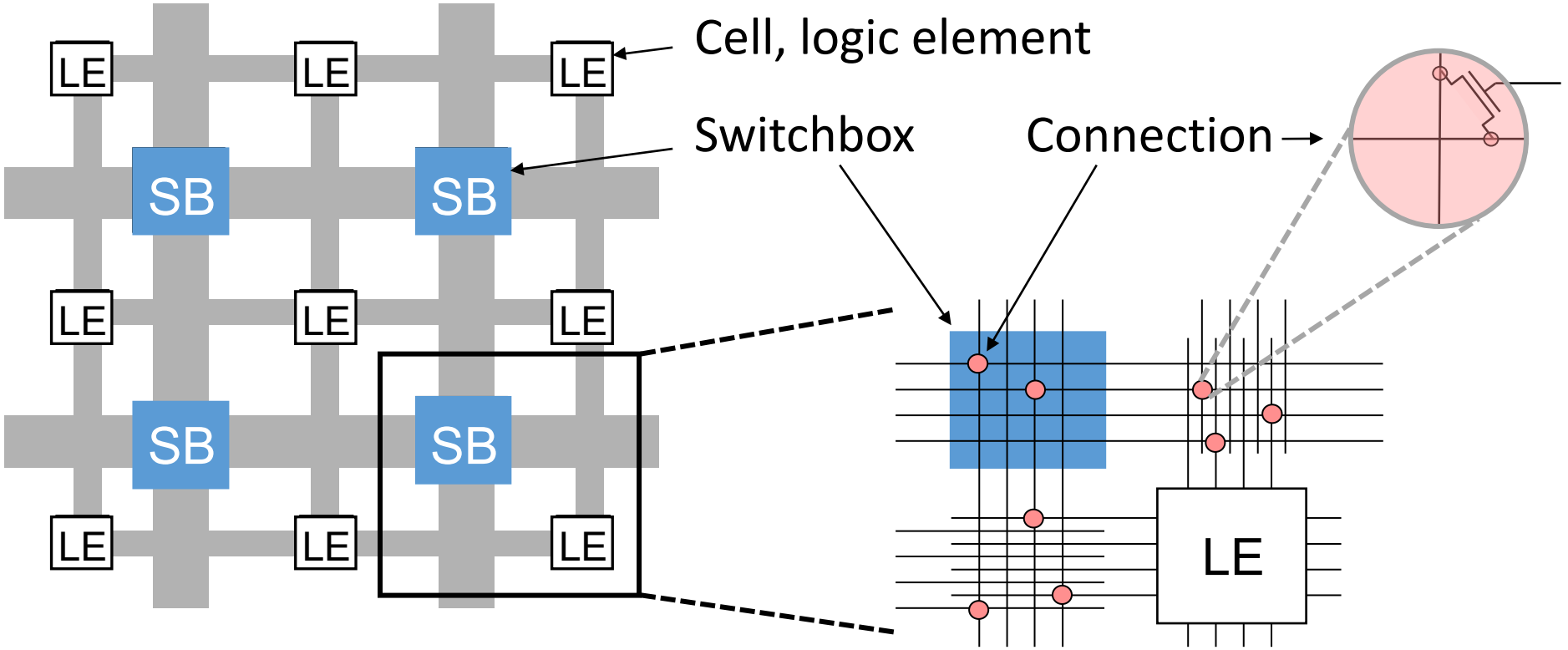




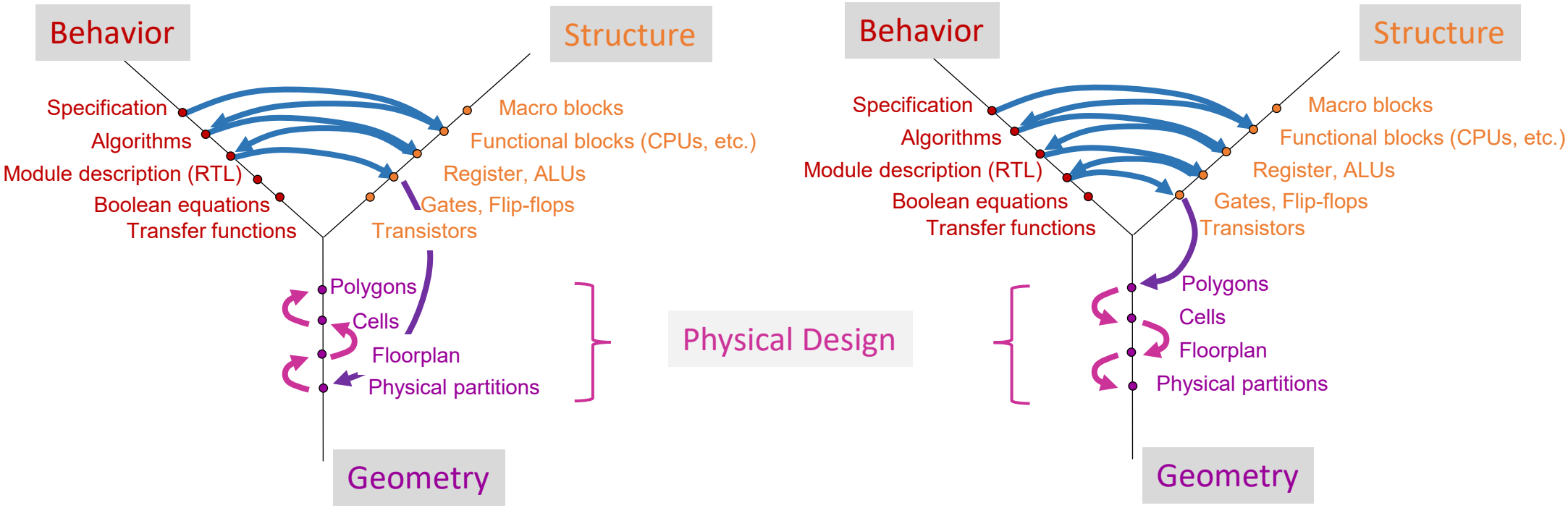


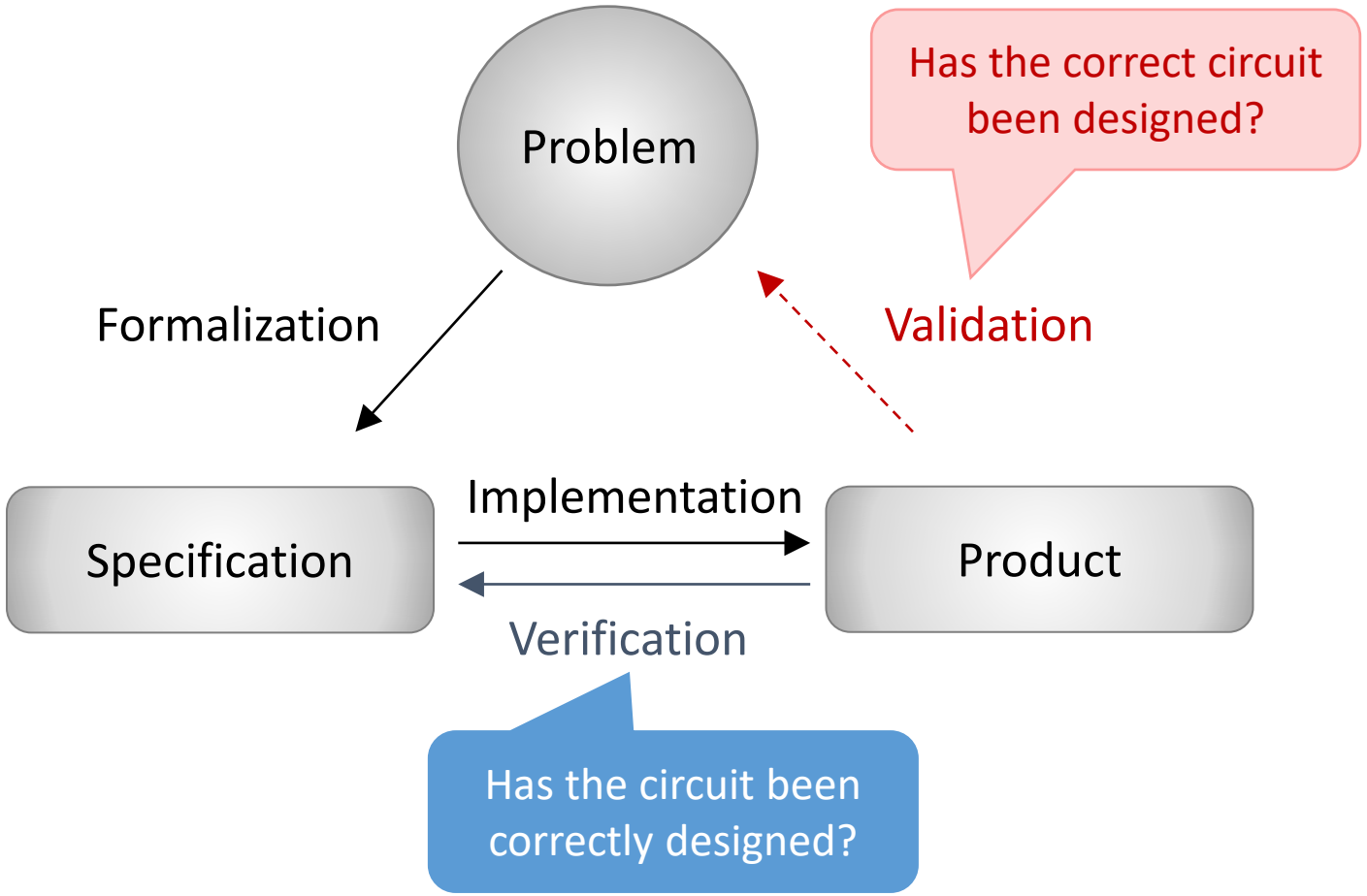


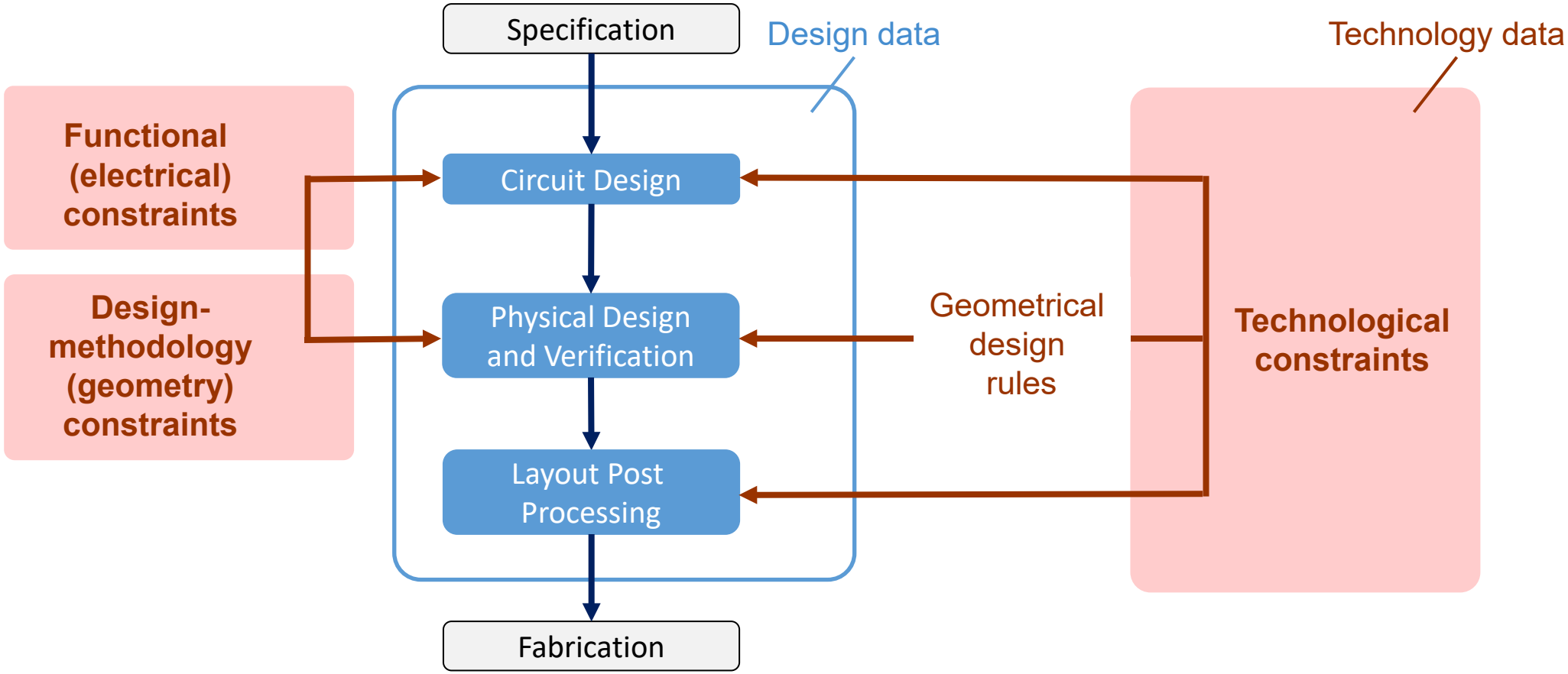


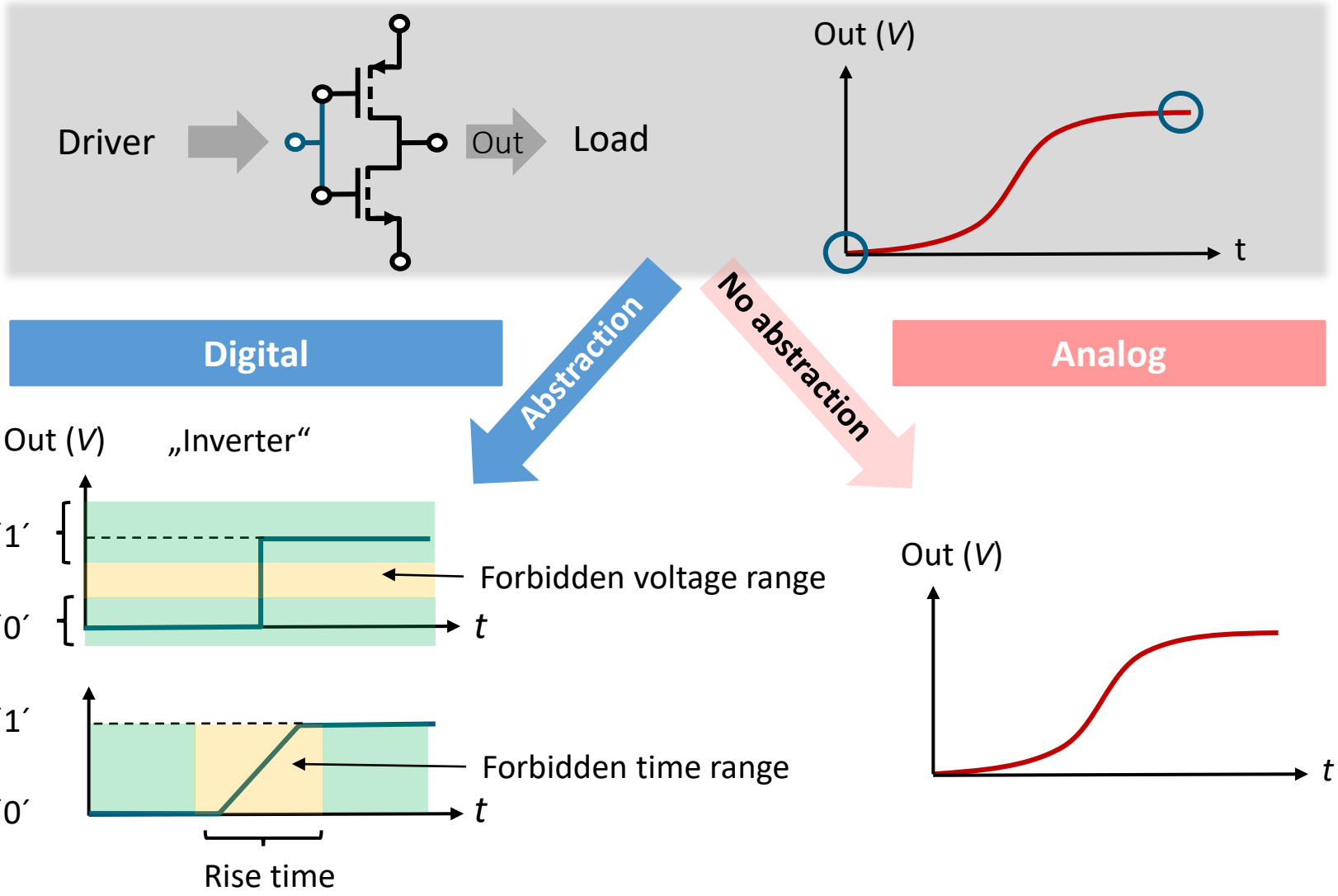


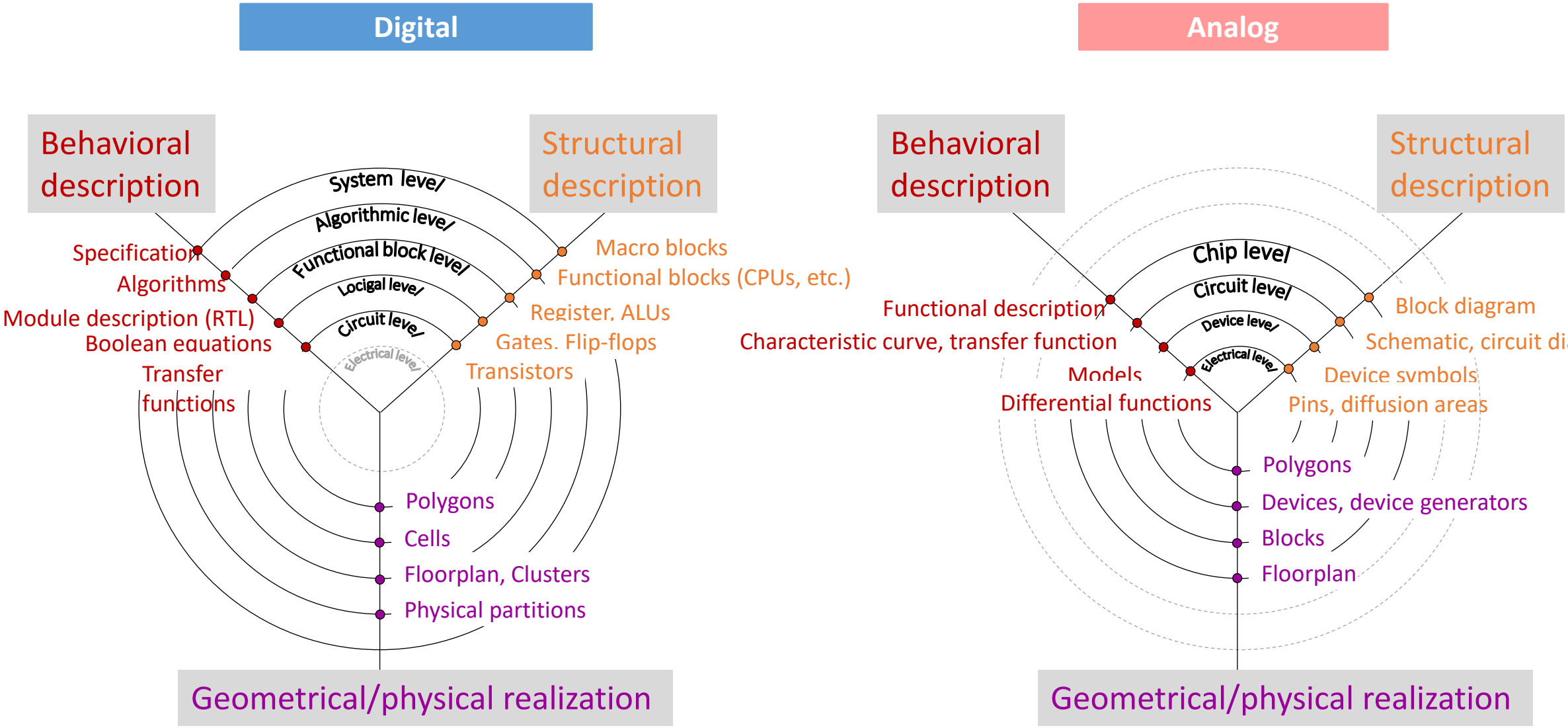
Design style	Design cost	Mask cost	Fab cost	Performance	Economic volume
Full custom	High	High	Low	High	High
Standard cell	Low	High	Medium	Medium	Wide range
Macro cell	High Low (reuse)	High	Low	High	Wide range
Gate array	Low	Medium	High	Low	Low
FPGA	Very low	None	High	Low	Low

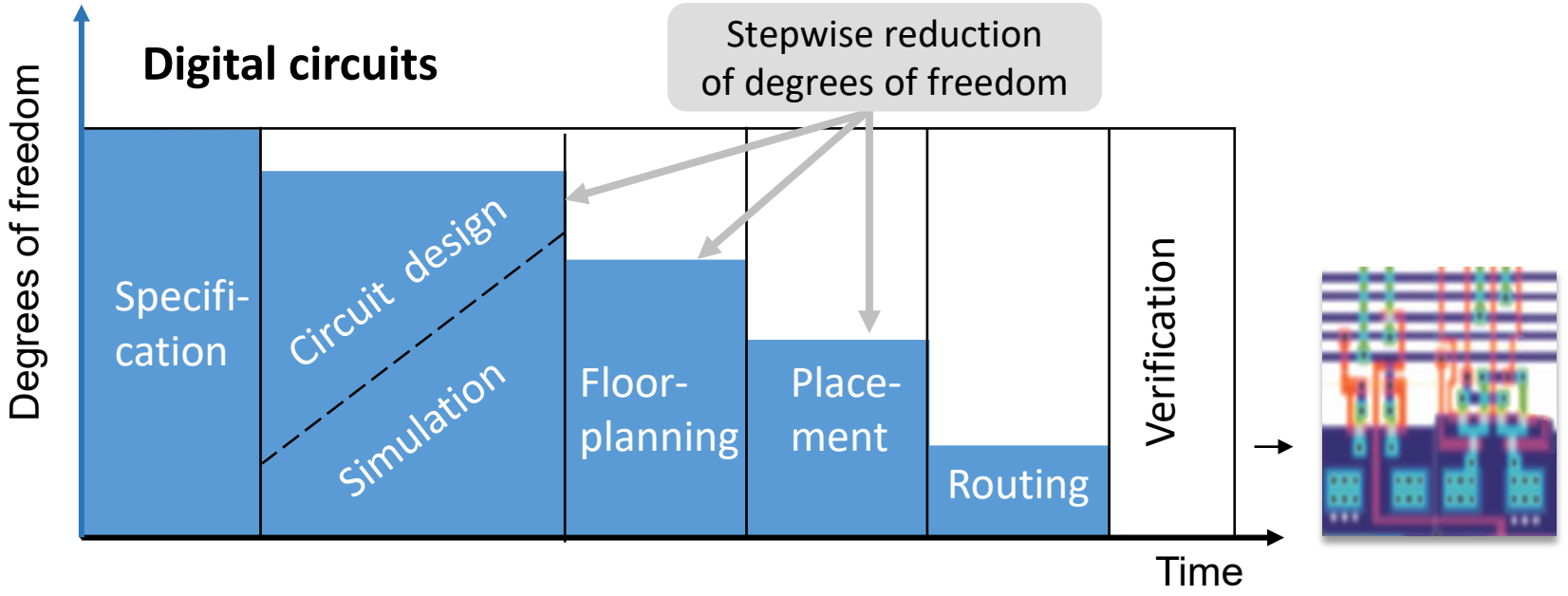


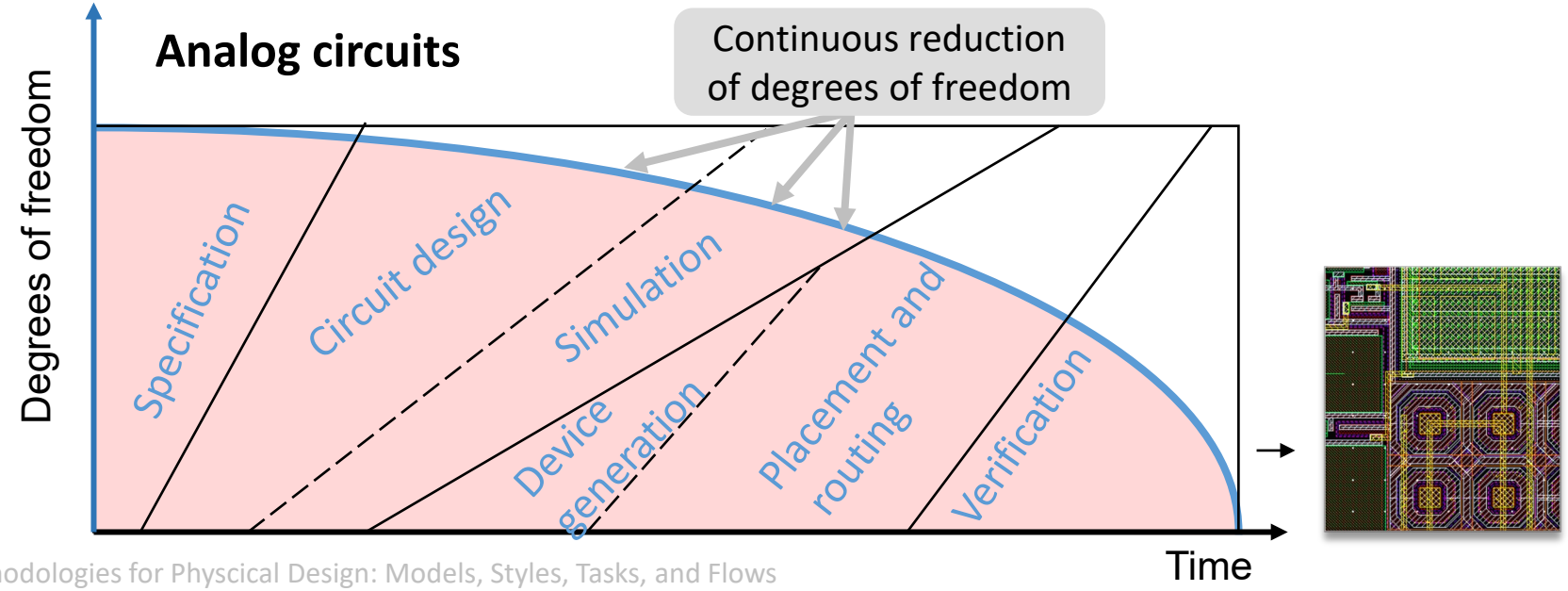


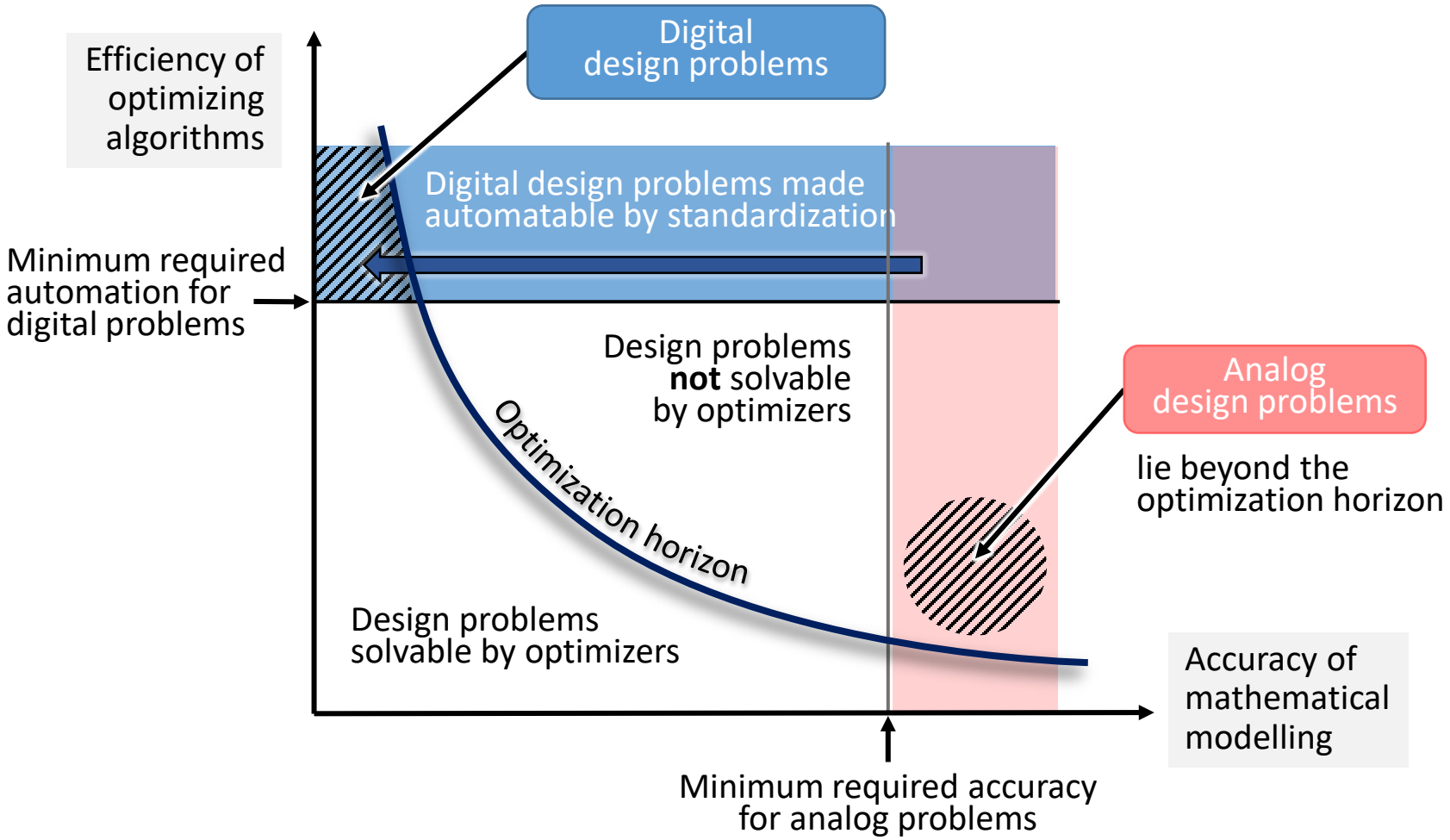




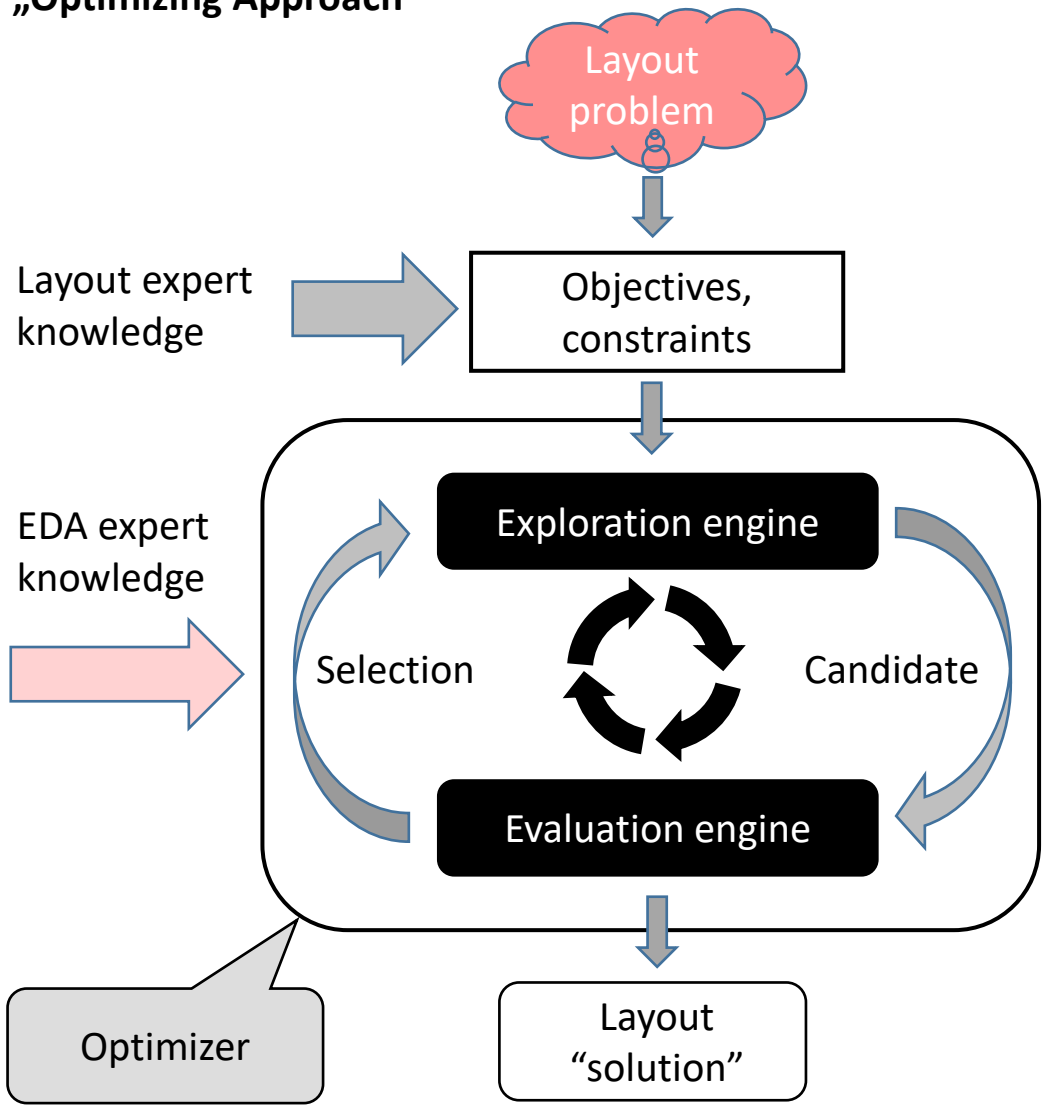




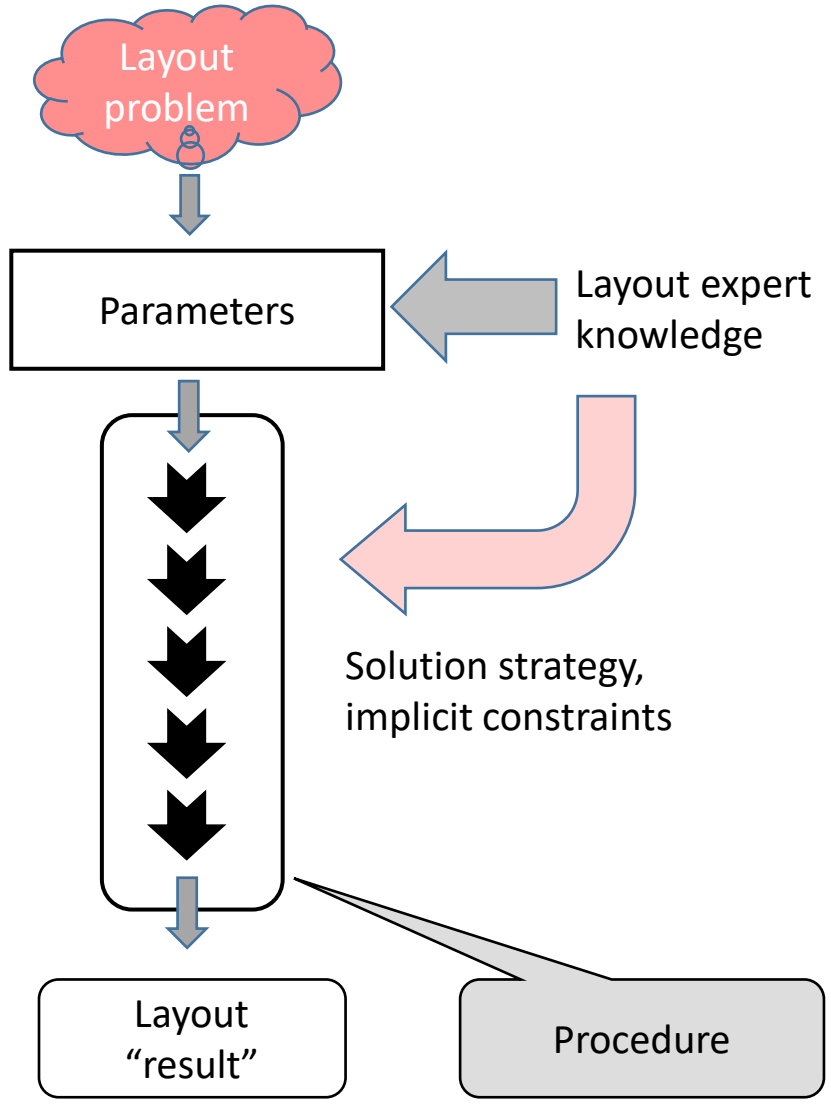




Top-Down Design
„Optimizing Approach“

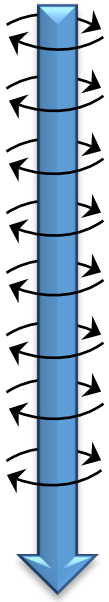


Bottom-Up Design „Procedural Approach“



Synthesis Steps

Logic Synthesis
Partitioning
Floorplanning
Power Routing
Global Placement
Detailed Placement
Clock Tree Synthesis
Global Routing
Detailed Routing
Timing Closure



Analysis / Verification Steps

Formal Verification

Global Timing

Routability Prediction

Timing

Parasitic Extraction
Sign-off DRC
Sign-off Timing
Sign-off Spice Simulation