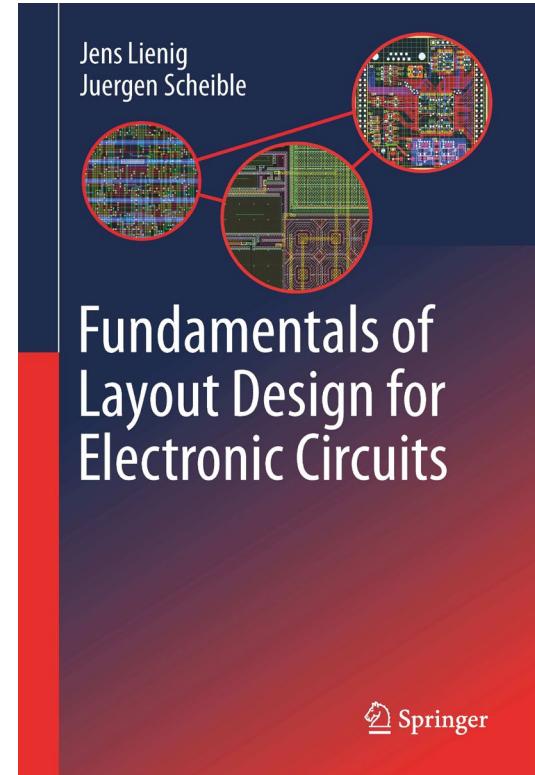


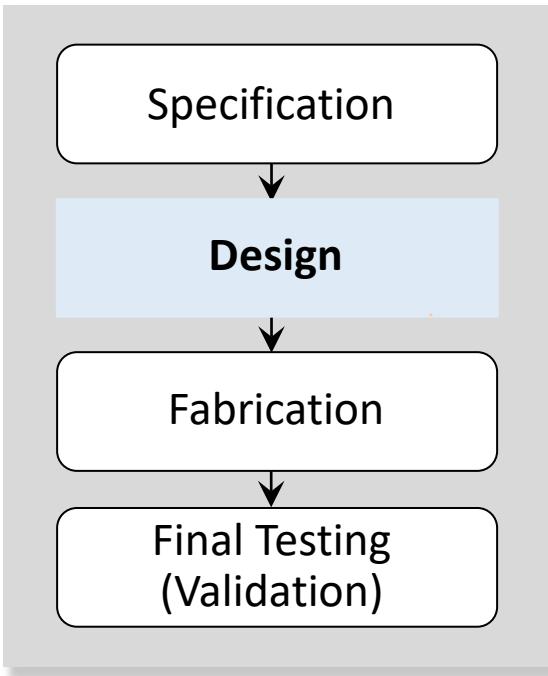
# Chapter 4: Methods for Physical Design: Models, Styles, Tasks, and Flows

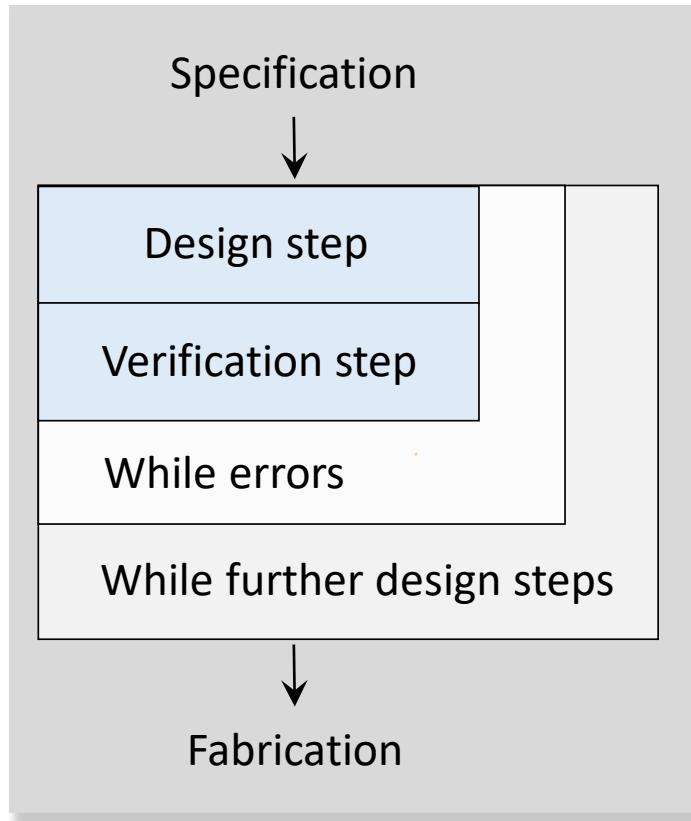
- 4.1 Design Flow
- 4.2 Design Models
- 4.3 Design Styles
- 4.4 Design Tasks and Tools
- 4.5 Physical Design Optimization and Constraints
- 4.6 Analog and Digital Design Flows
- 4.7 Visions for Analog Design

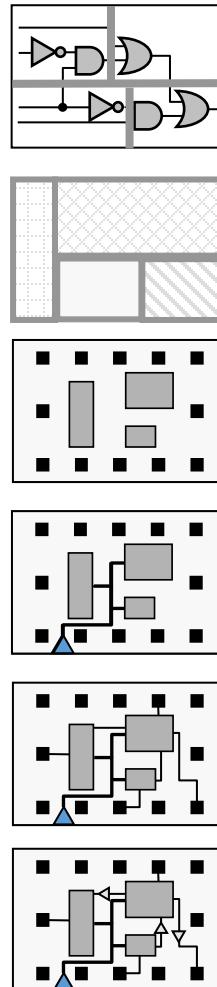
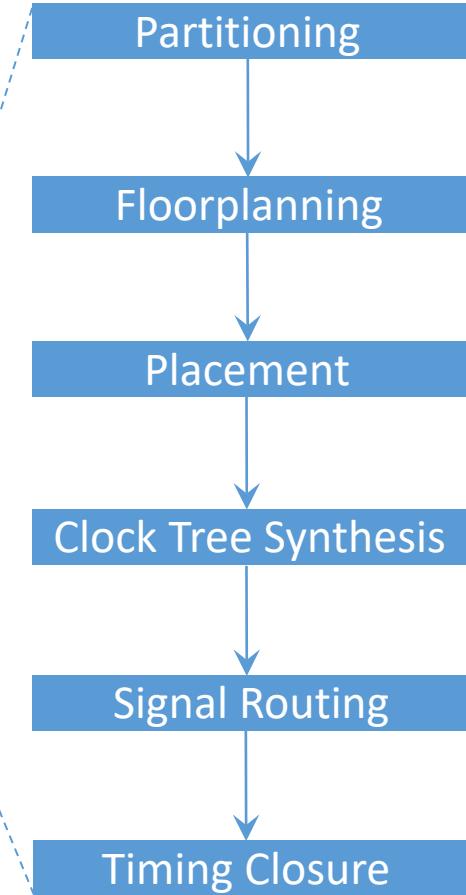
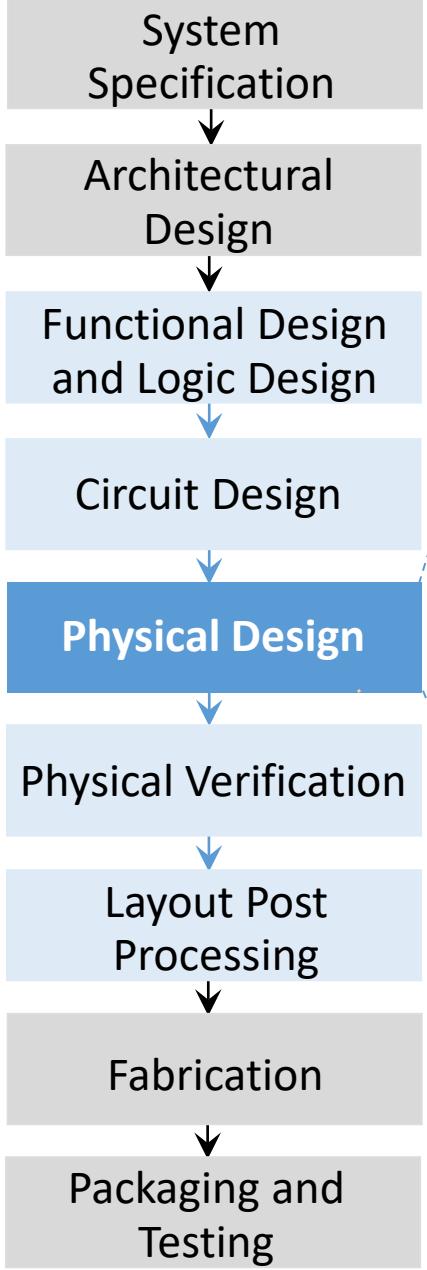
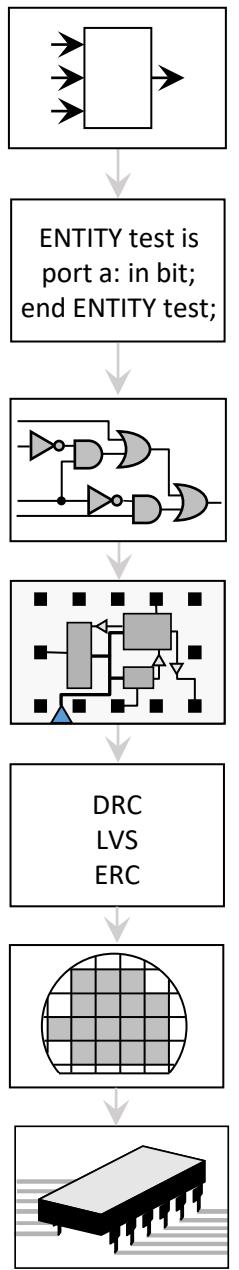


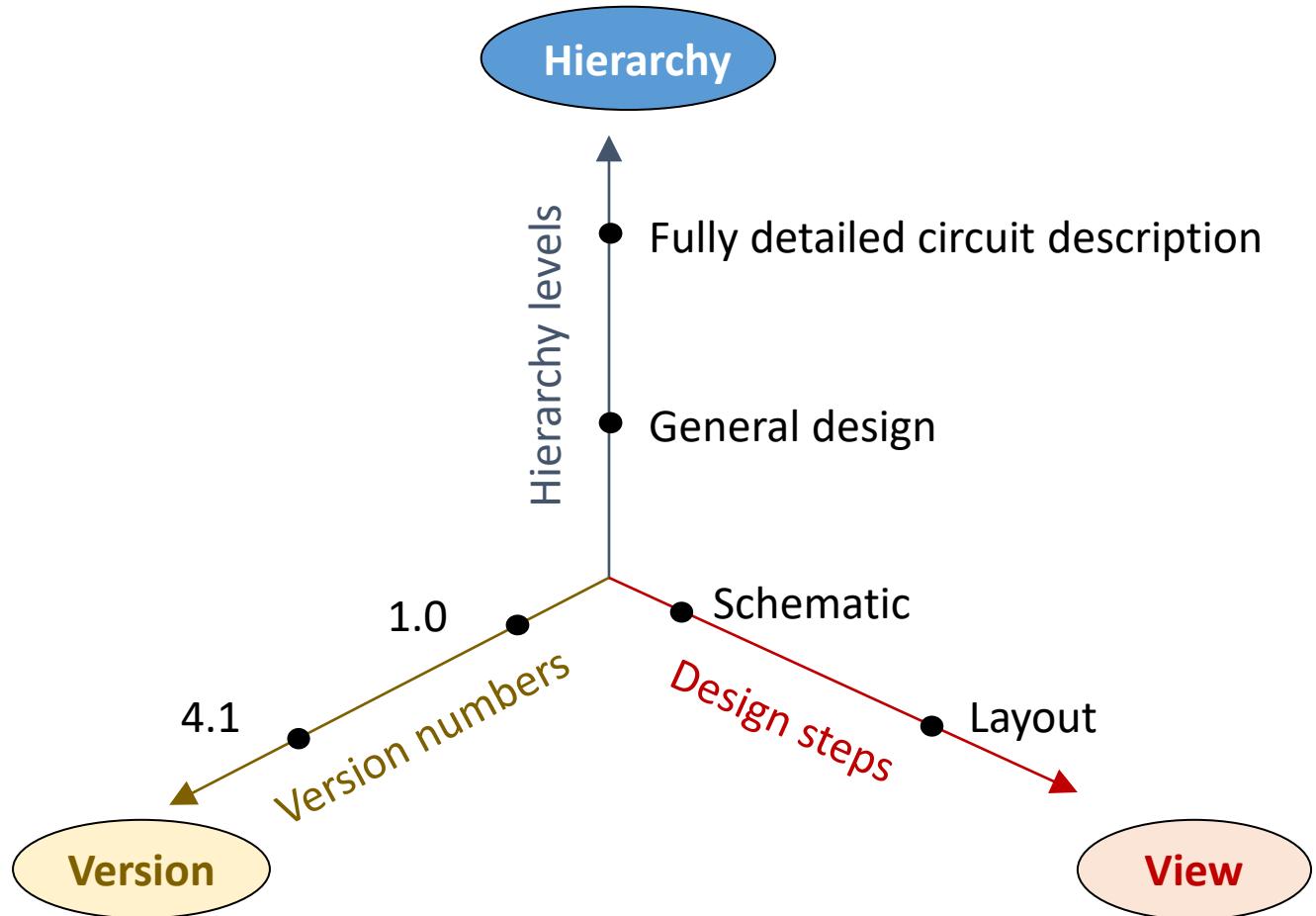
# Chapter 4: Methods for Physical Design: Models, Styles, Tasks, and Flows

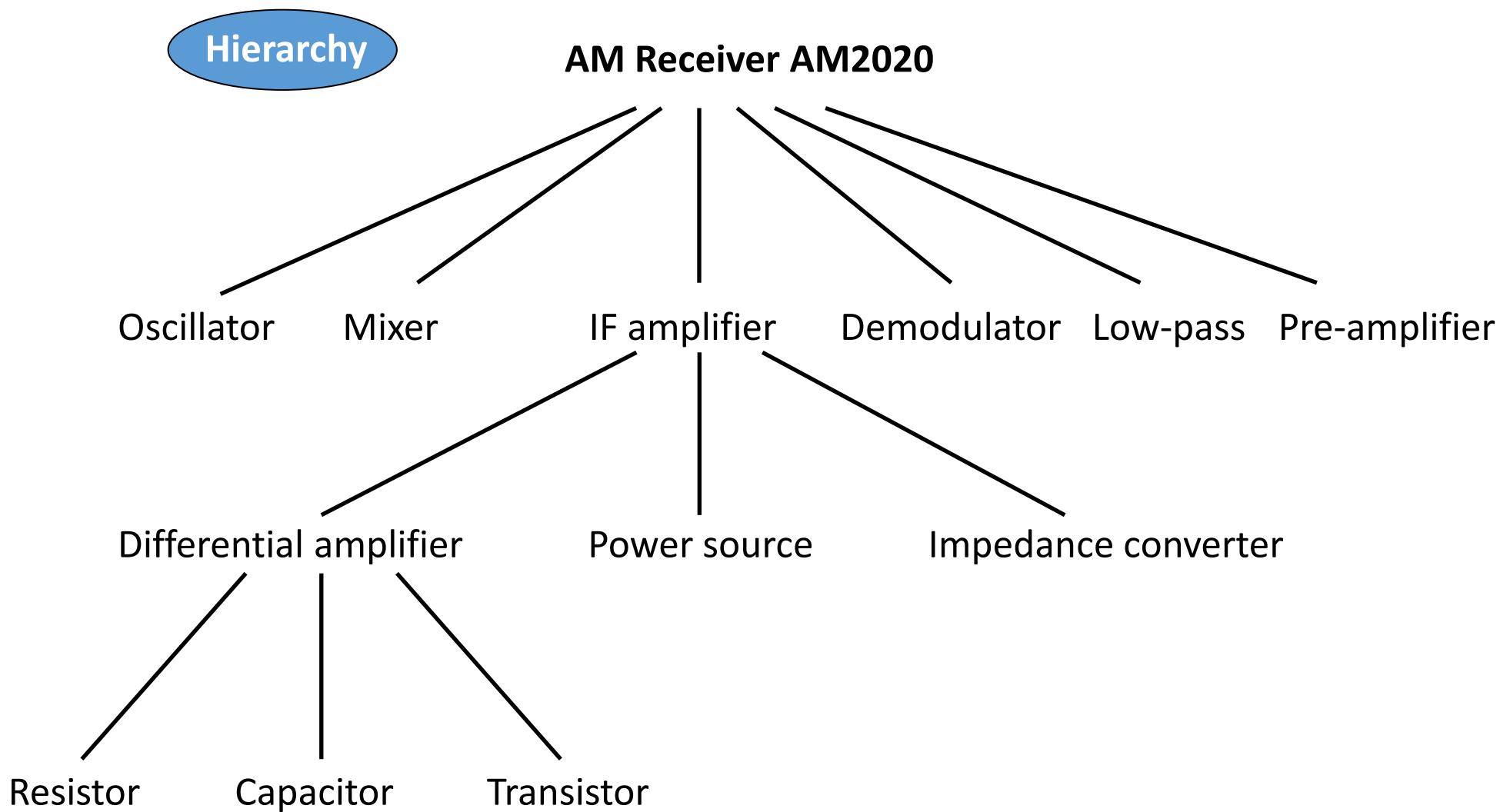
- 4.1      Design Flow**
- 4.2      Design Models**
  - 4.2.1     Three-Dimensional Design Space
  - 4.2.2     The Gajski-Kuhn Y-Chart
- 4.3      Design Styles**
  - 4.3.1    Full-Custom and Semi-Custom Design
  - 4.3.2    Top-Down, Bottom-Up and Meet-in-the-Middle Design
- 4.4      Design Tasks and Tools**
  - 4.4.1    Creating: Synthesis
  - 4.4.2    Checking: Analysis
  - 4.4.3    Eliminating Deficiencies: Optimization
- 4.5      Physical Design Optimization and Constraints**
  - 4.5.1    Optimization Goals
  - 4.5.2    Constraint Categories
  - 4.5.3    Physical Design Optimization
- 4.6      Analog and Digital Design Flows**
  - 4.6.1    The Different Worlds of Analog and Digital Design
  - 4.6.2    Analog Design Flow
  - 4.6.3    Digital Design Flow
  - 4.6.4    Mixed-Signal Design Flow
- 4.7      Visions for Analog Design**
  - 4.7.1    A “Continuous” Layout Design Flow
  - 4.7.2    A “Bottom-Up Meets Top-Down” Layout Design Flow





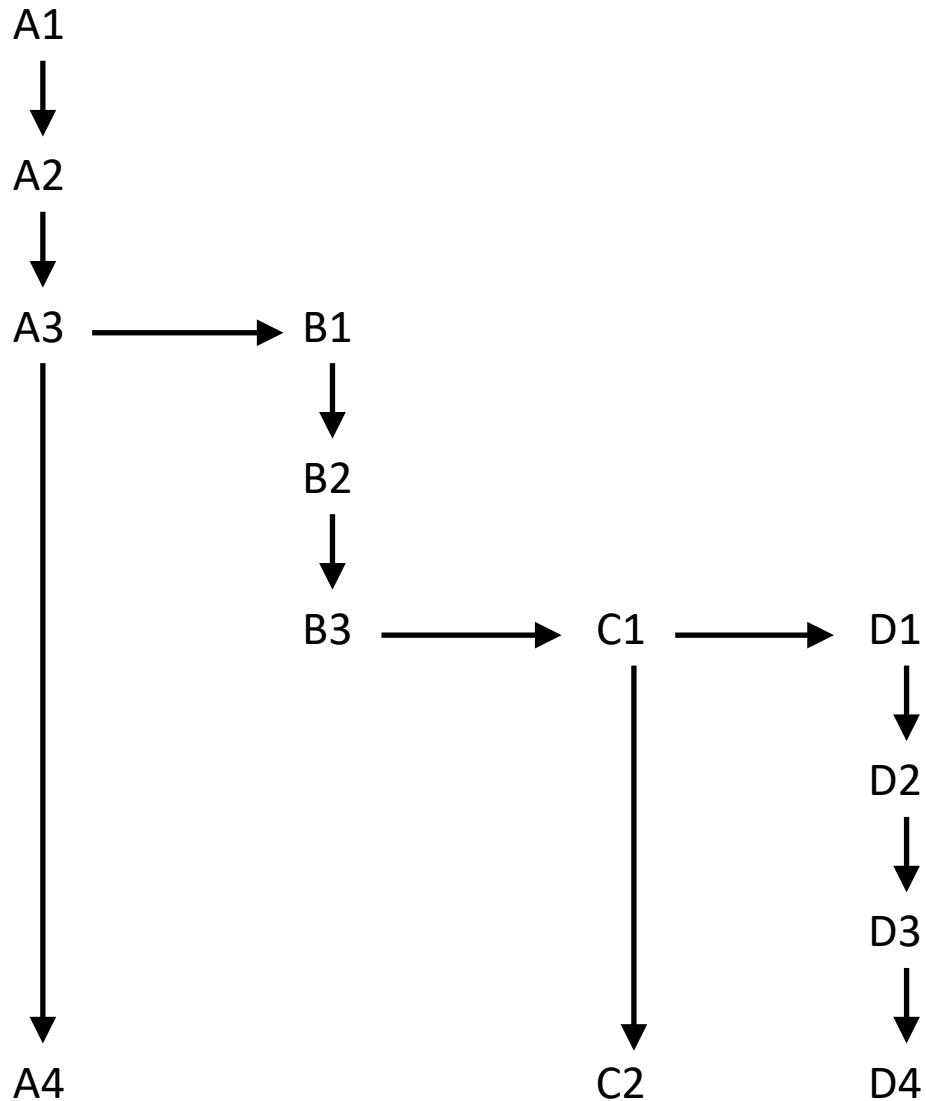


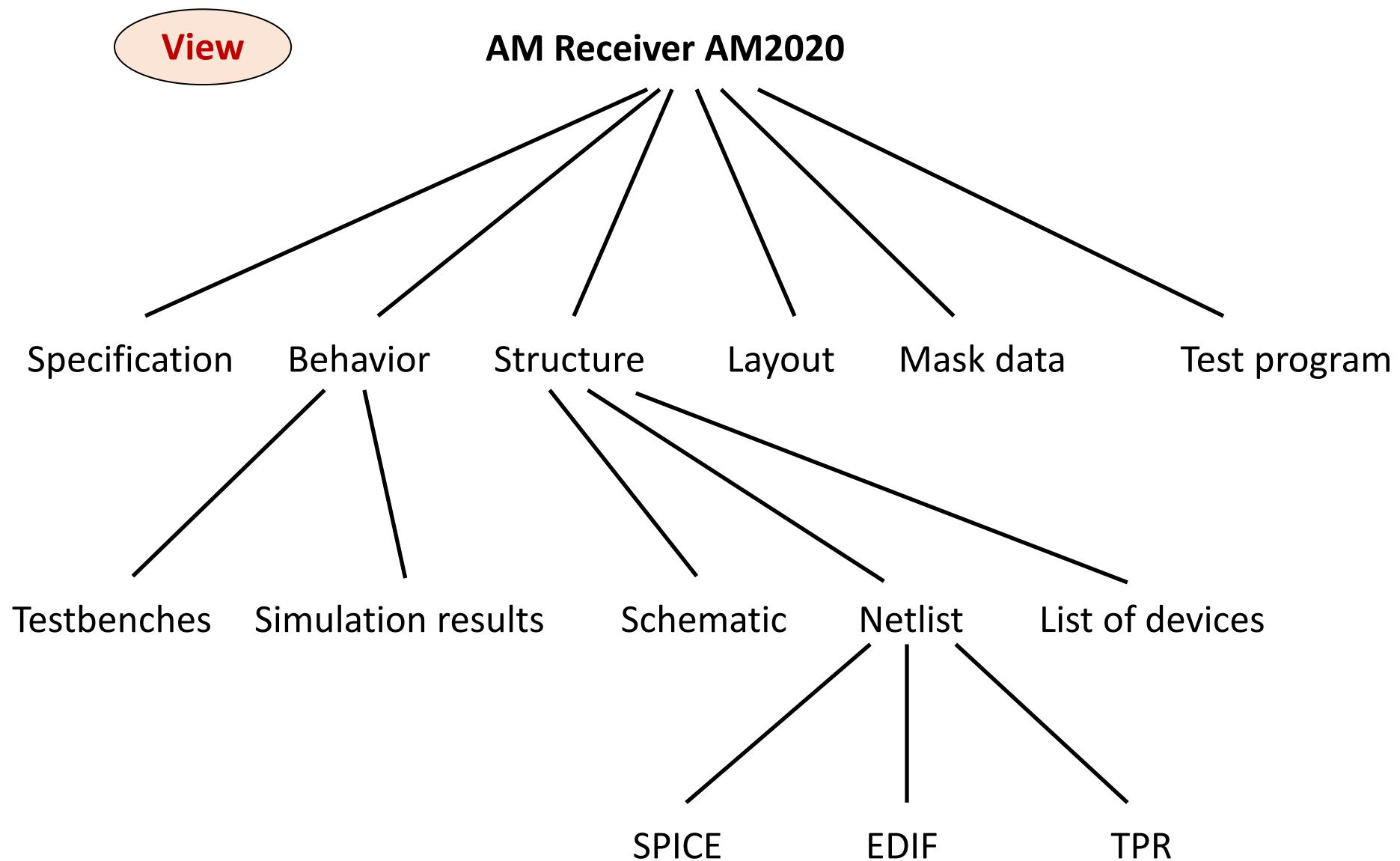


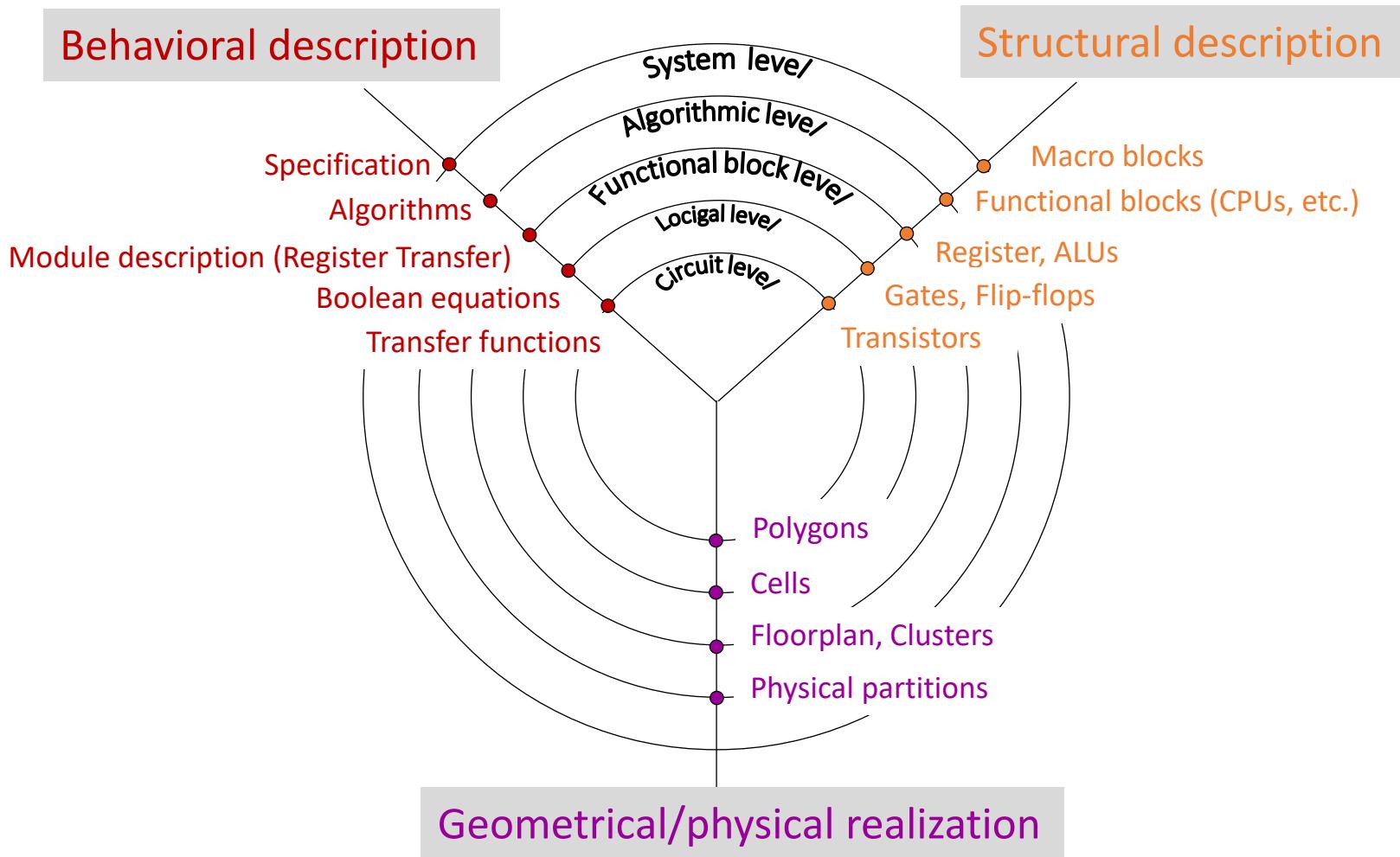


## AM Receiver AM2020

Version







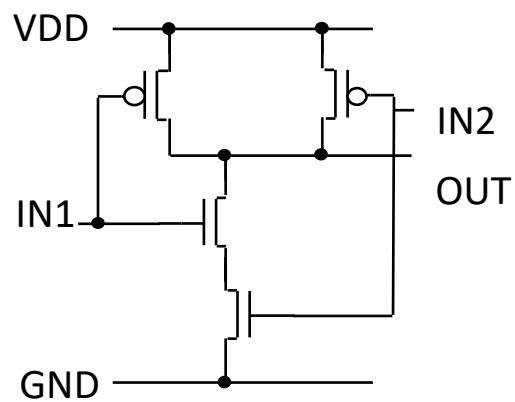
## Behavioral description

IN1	IN2	OUT
0	0	1
0	1	1
1	0	1
1	1	0

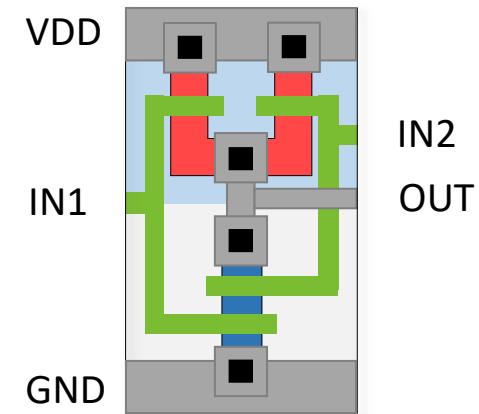
NAND gate



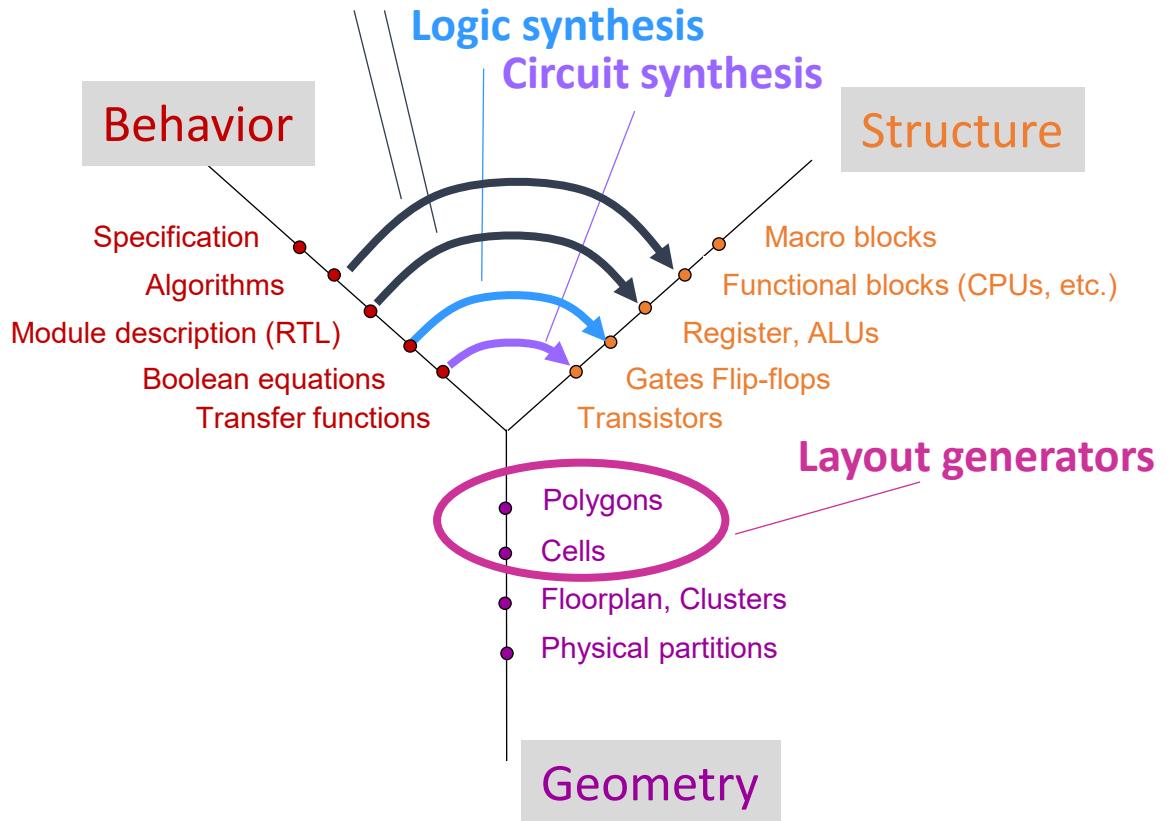
## Structural description



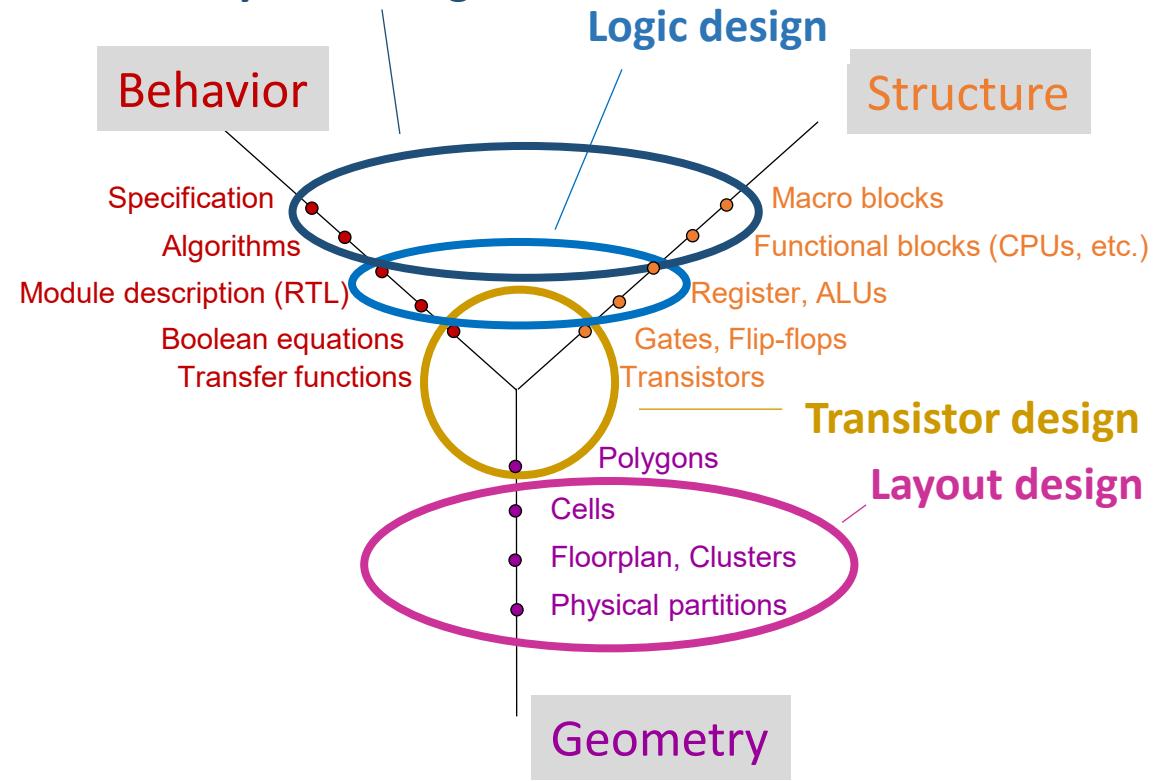
## Geometrical/physical realization

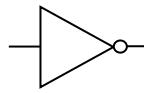


## Behavioral synthesis

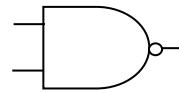


## System design

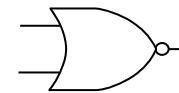


**INV**

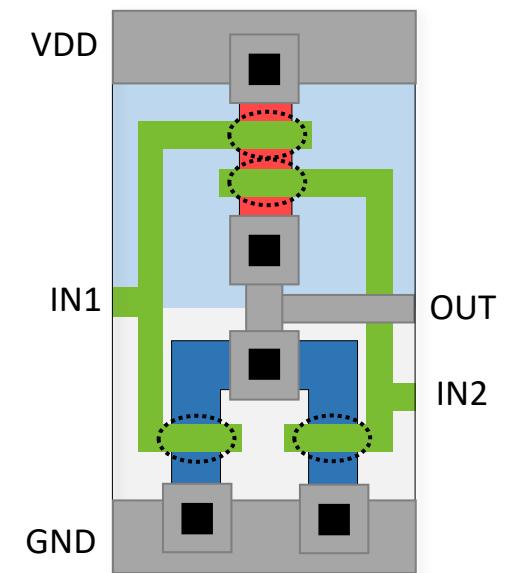
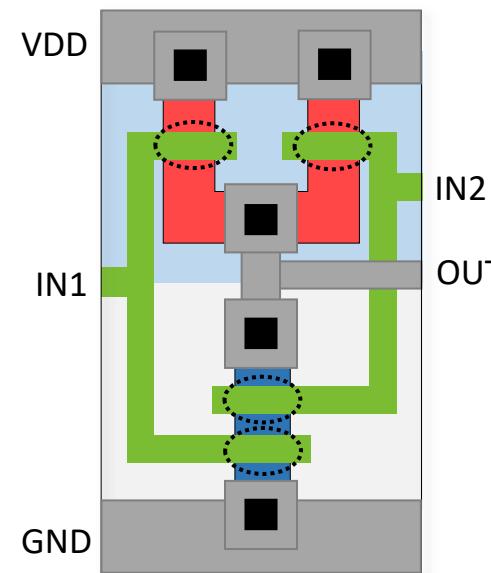
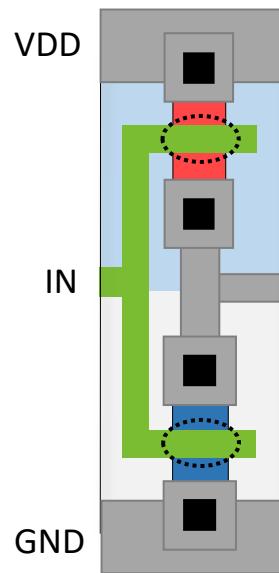
IN	OUT
0	1
1	0

**NAND**

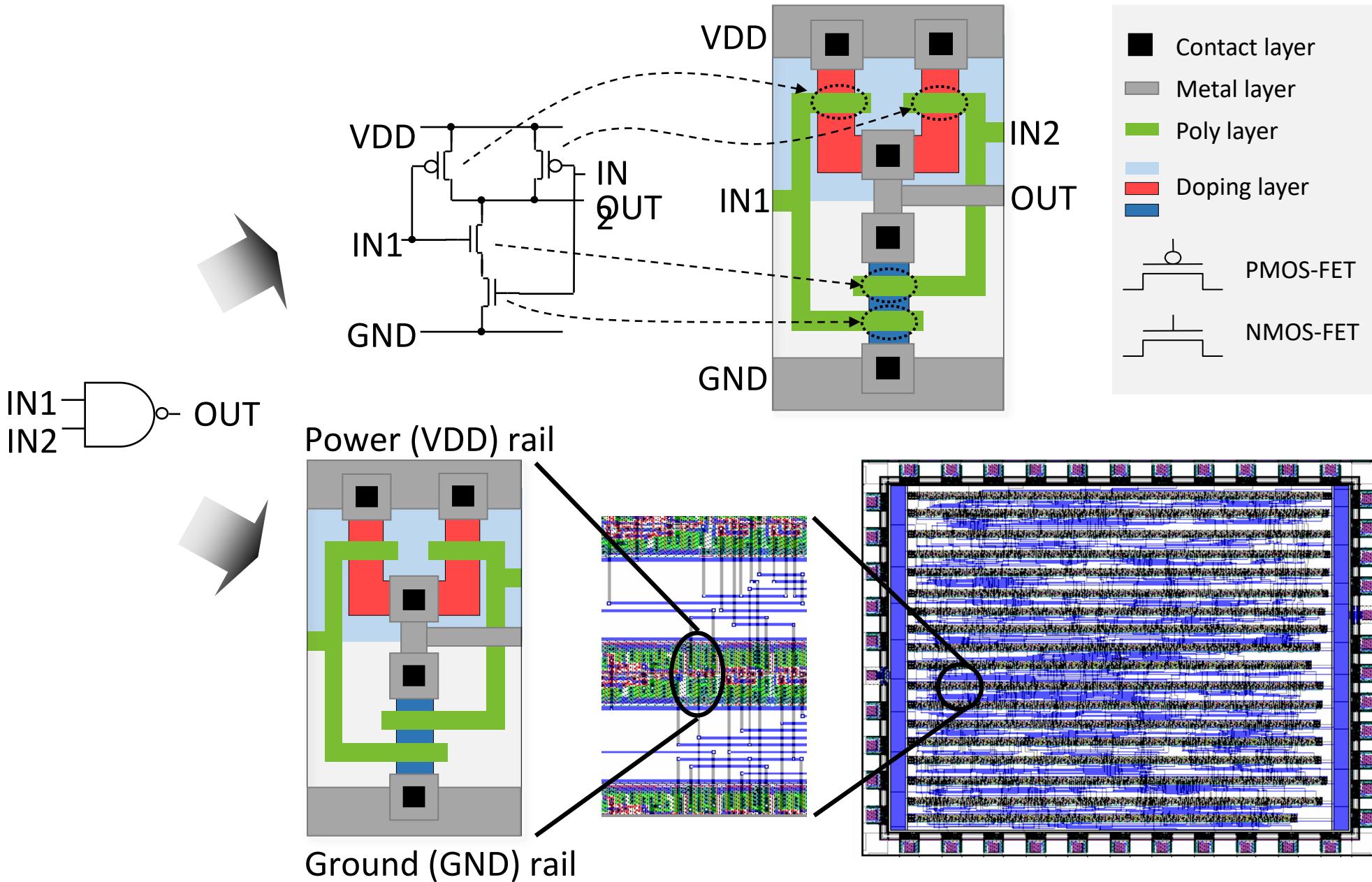
IN1	IN2	OUT
0	0	1
1	0	1
0	1	1
1	1	0

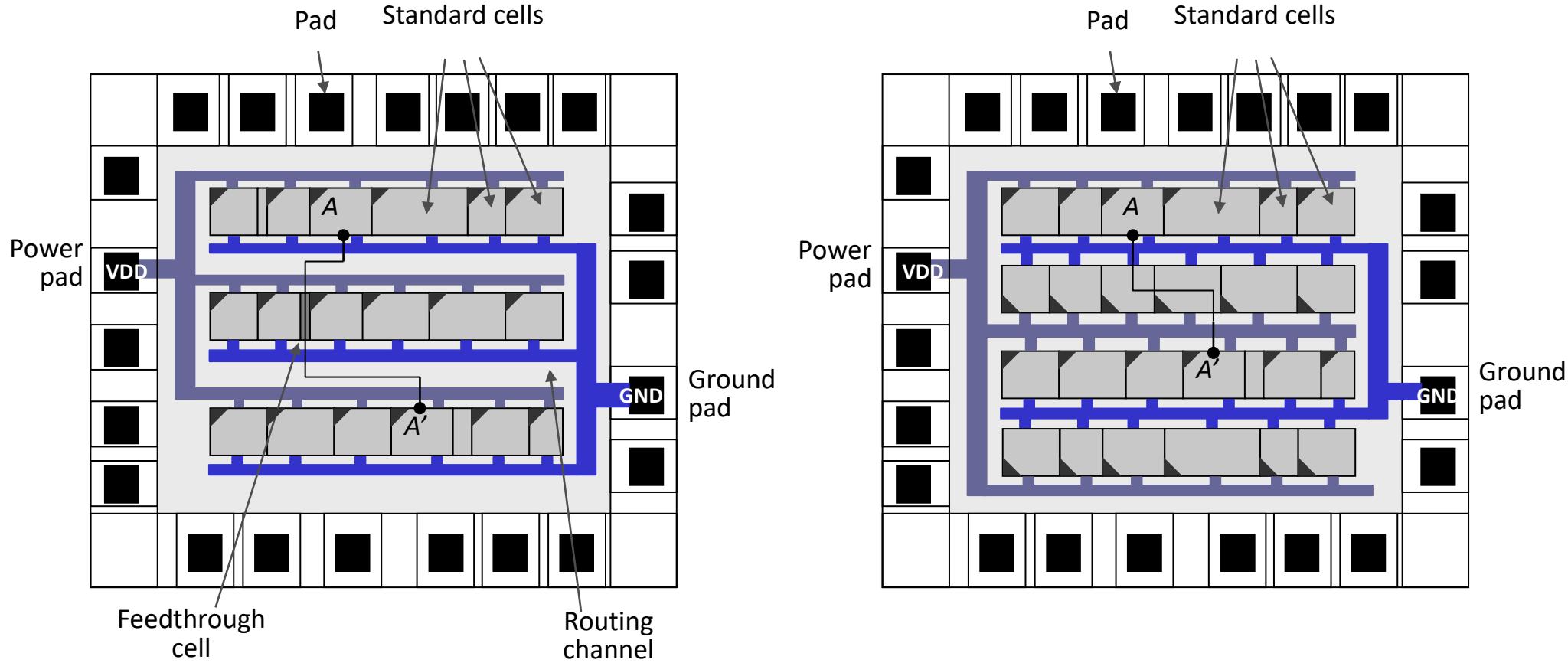
**NOR**

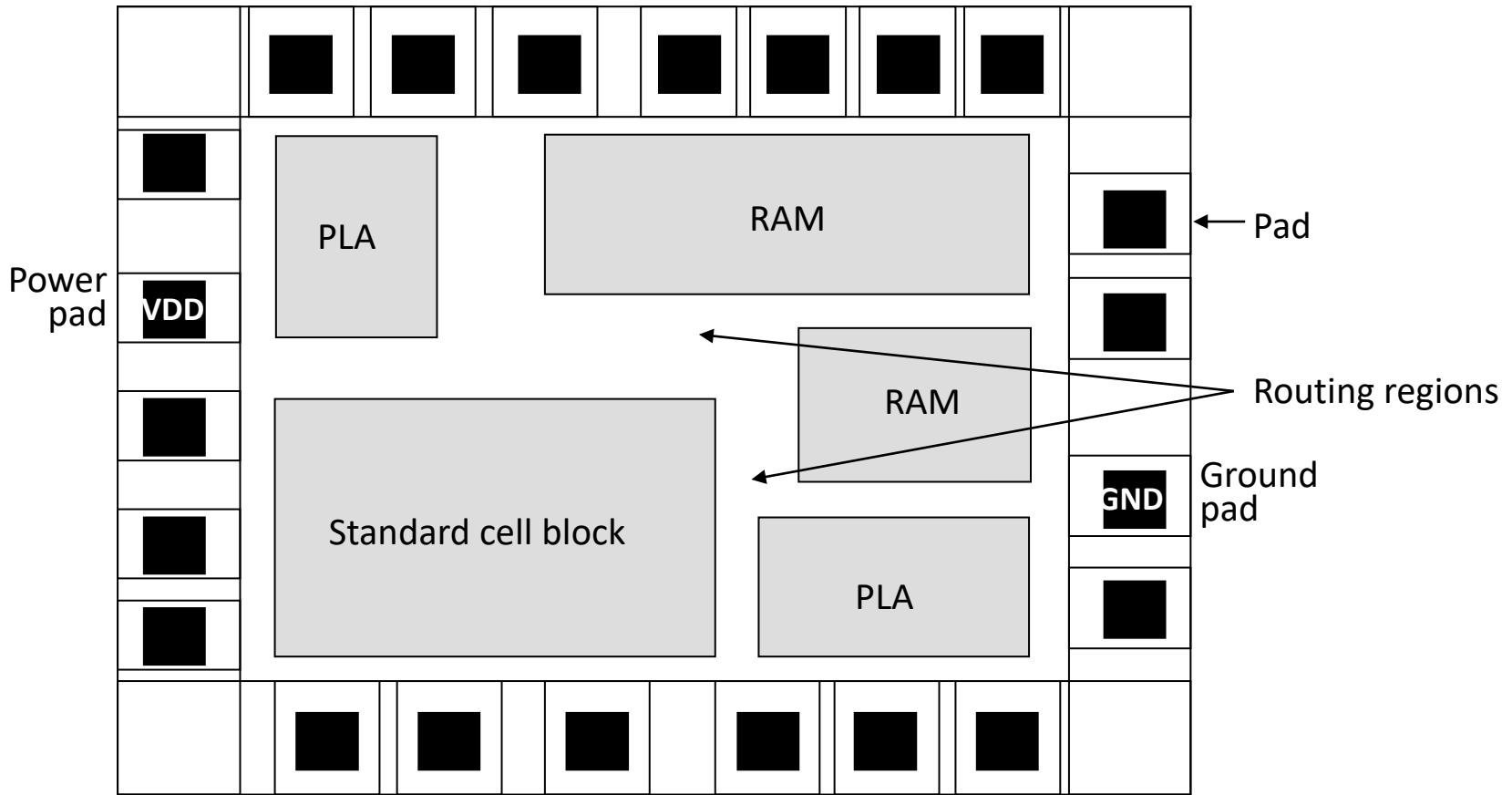
IN1	IN2	OUT
0	0	1
1	0	0
0	1	0
1	1	0

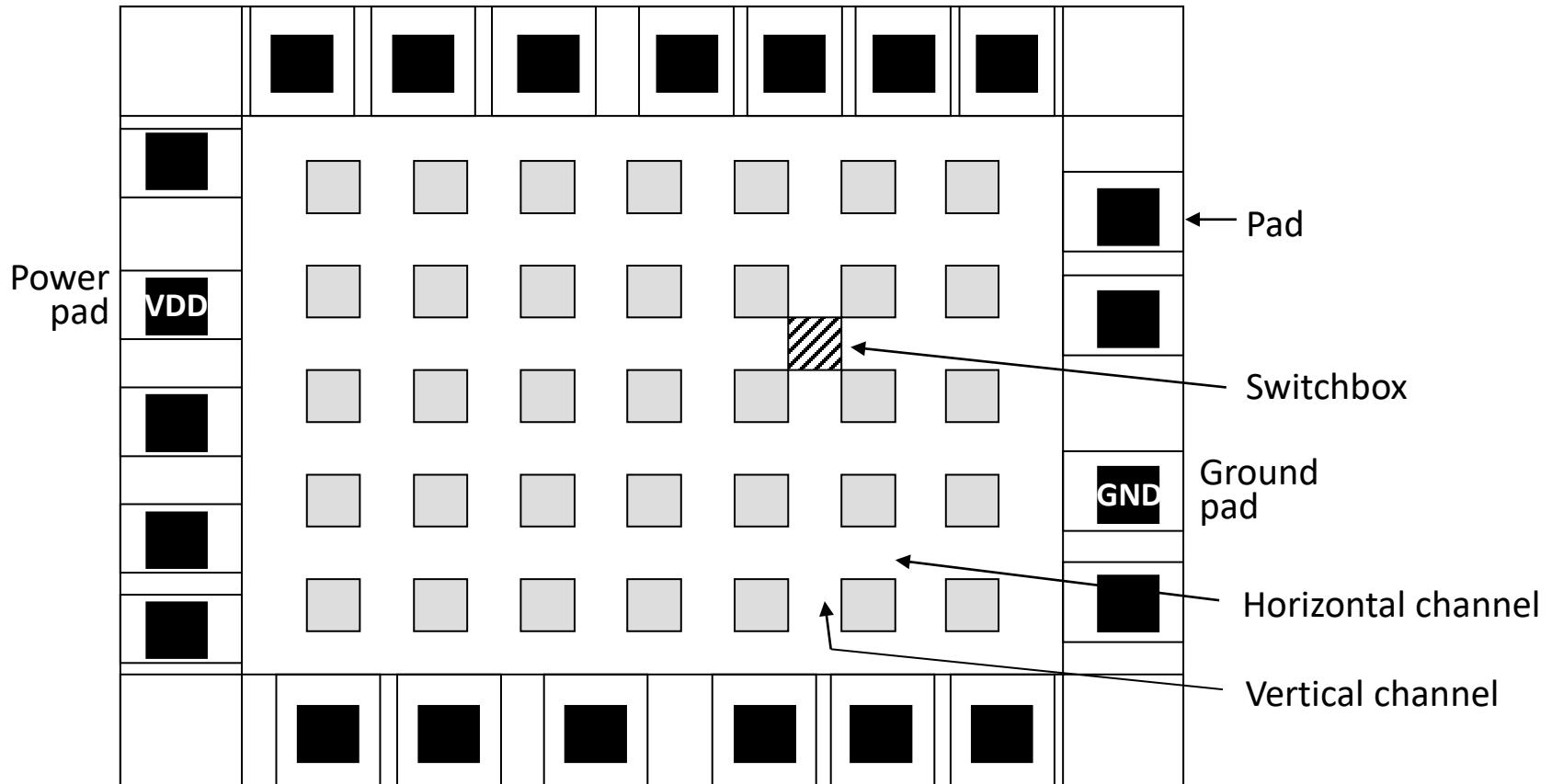


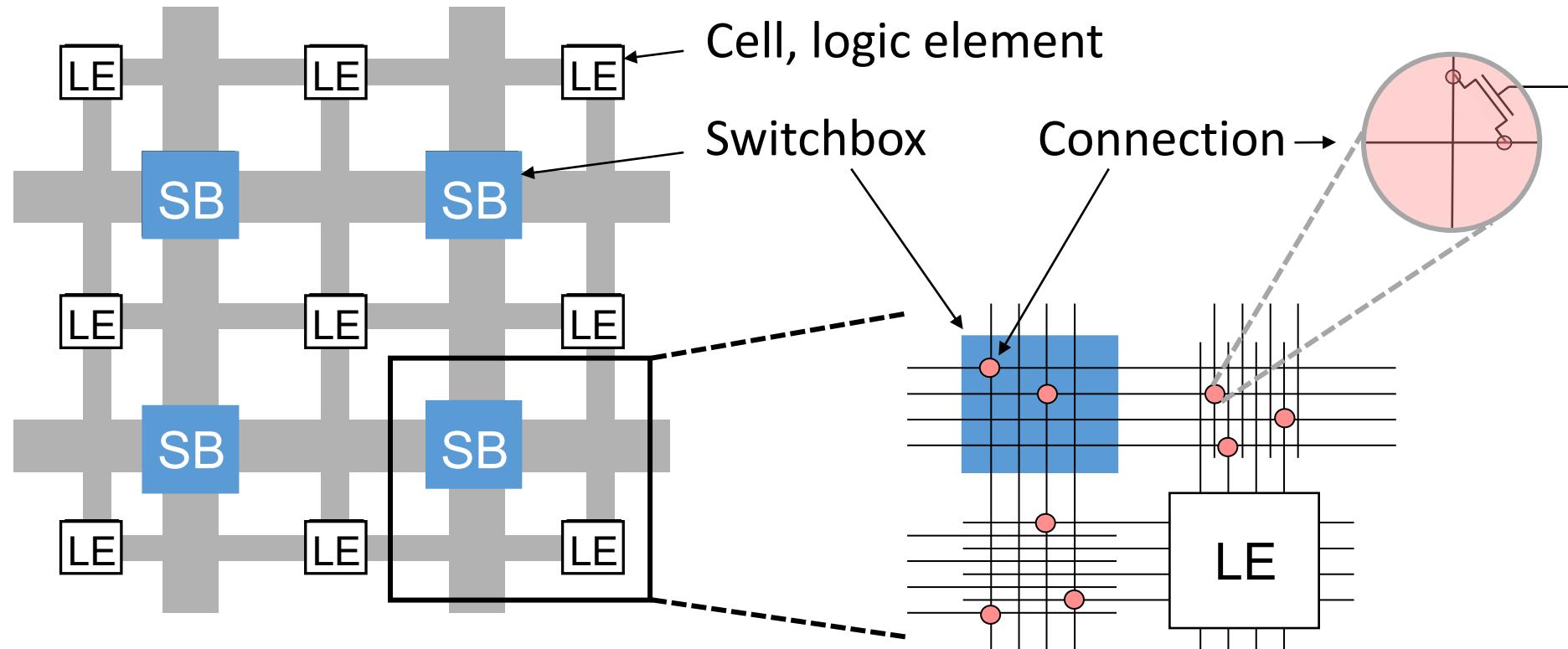
- Contact layer
- Metal layer
- Poly layer
- n-doping layer
- p+-doping layer
- n+-doping layer
- Transistor



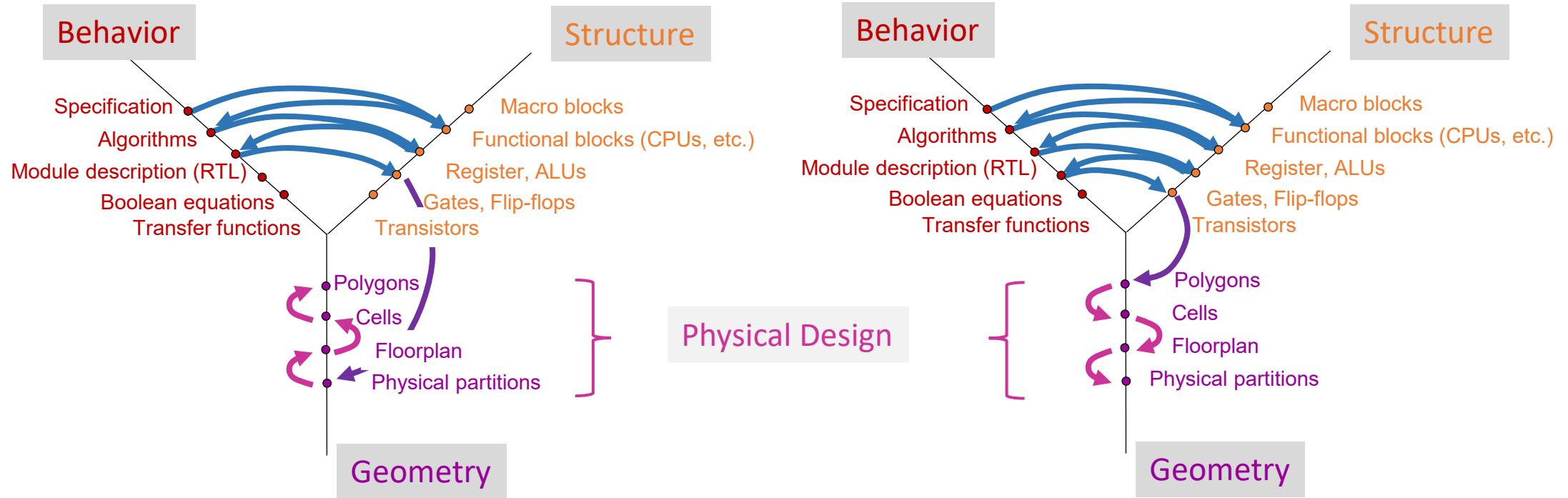


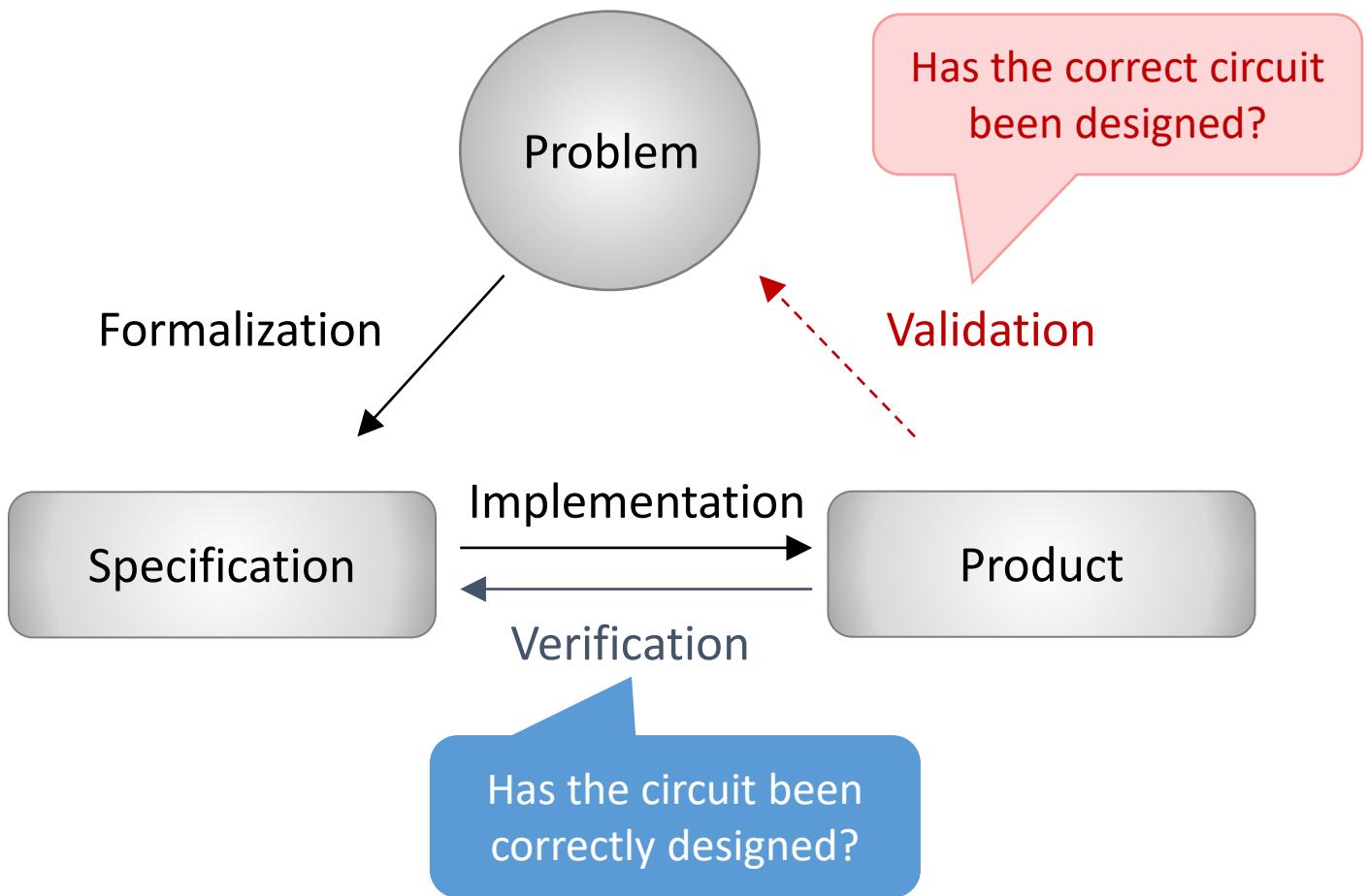


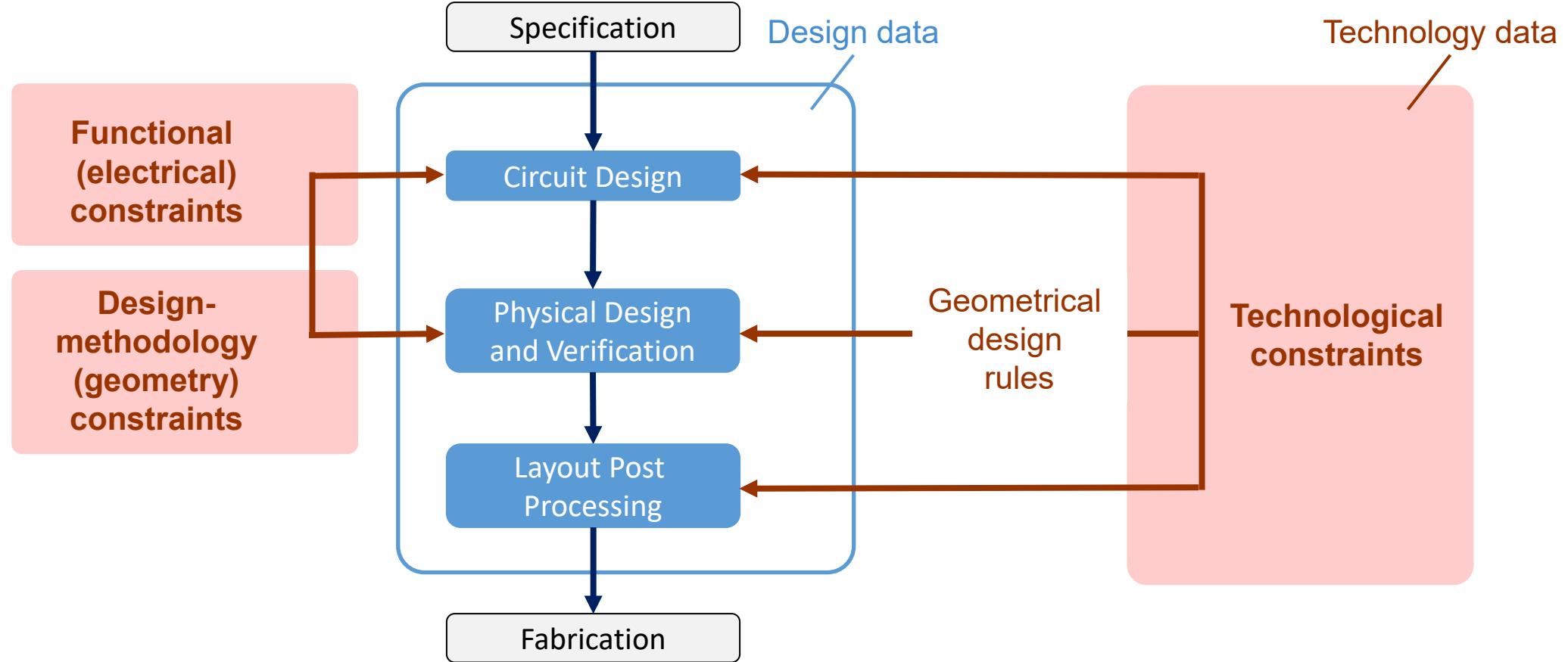


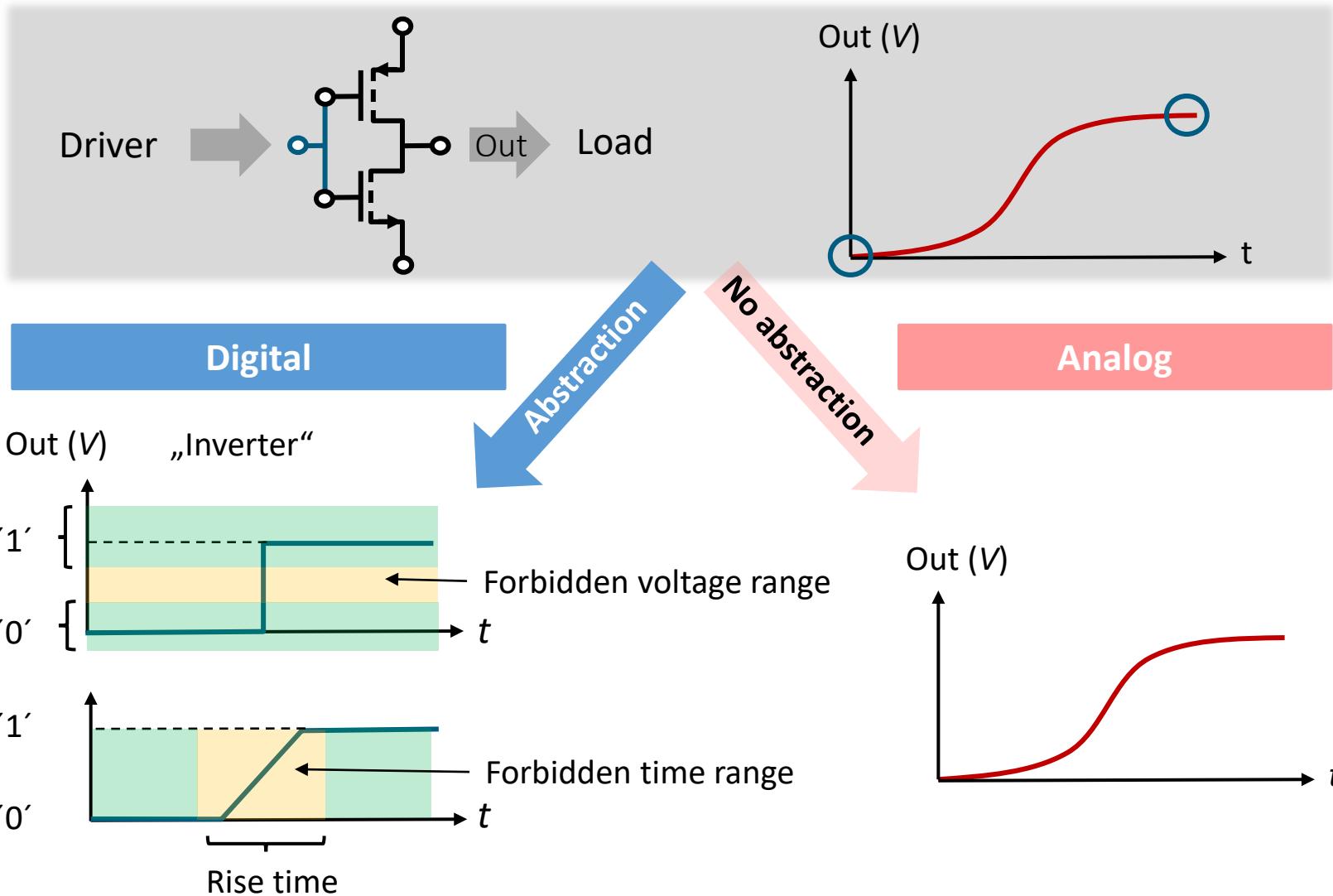


Design style	Design cost	Mask cost	Fab cost	Performance	Economic volume
Full custom	High	High	Low	High	High
Standard cell	Low	High	Medium	Medium	Wide range
Macro cell	High Low (reuse)	High	Low	High	Wide range
Gate array	Low	Medium	High	Low	Low
FPGA	Very low	None	High	Low	Low









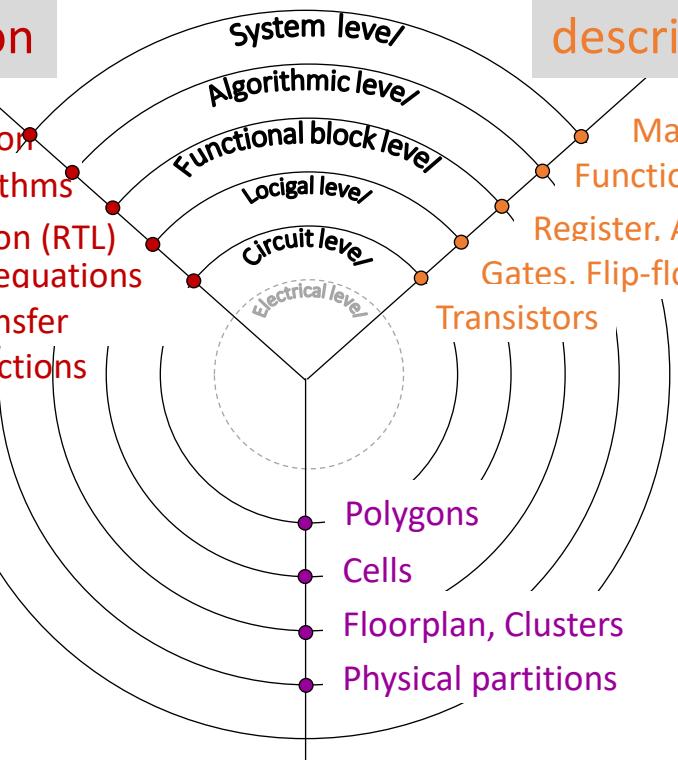
## Digital

### Behavioral description

Specification  
Algorithms  
Module description (RTL)  
Boolean equations  
Transfer functions

### Structural description

Macro blocks  
Functional blocks (CPUs, etc.)  
Register, ALUs  
Gates, Flip-flops  
Transistors



## Analog

### Behavioral description

Functional description  
Characteristic curve, transfer function

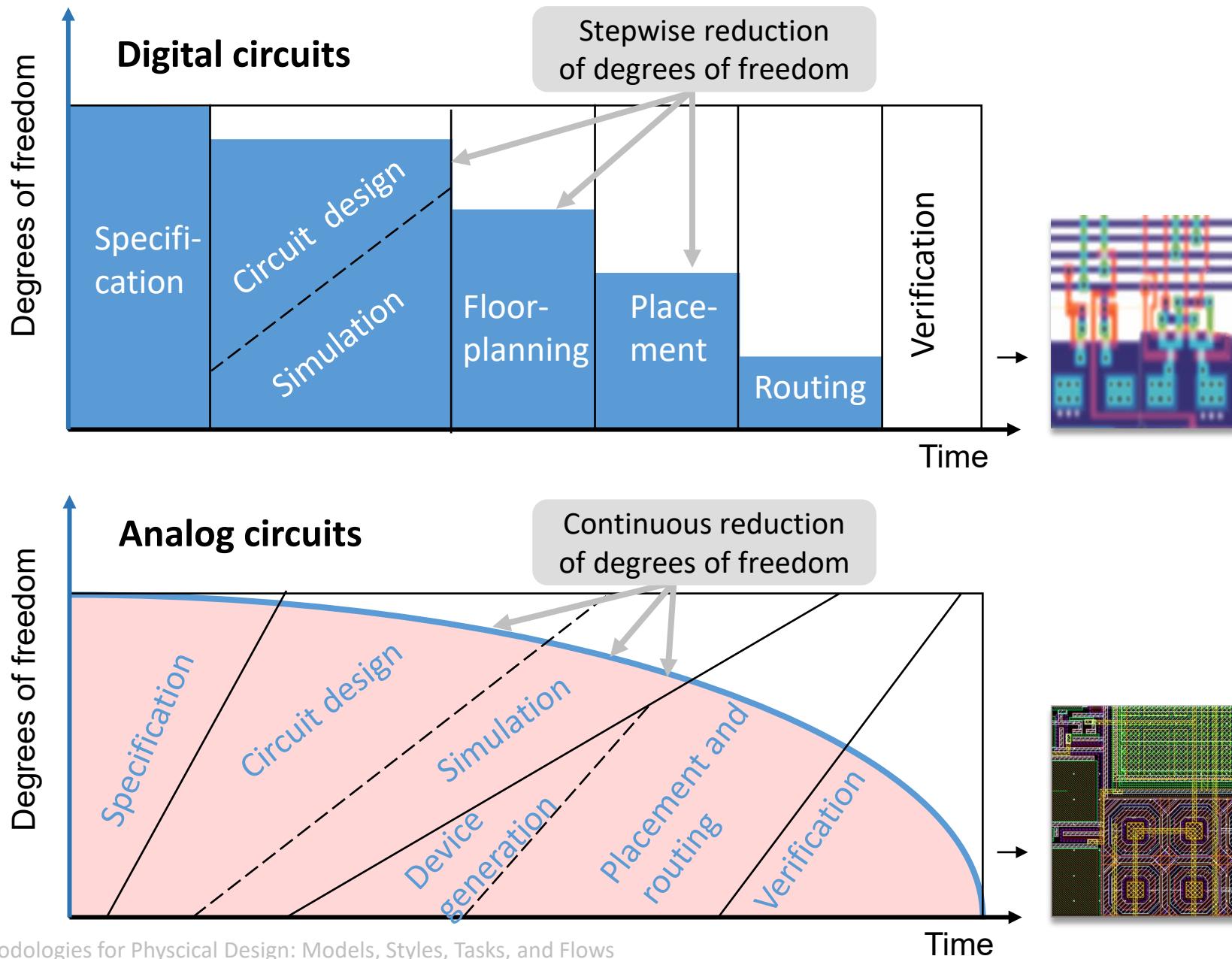
Models  
Differential functions

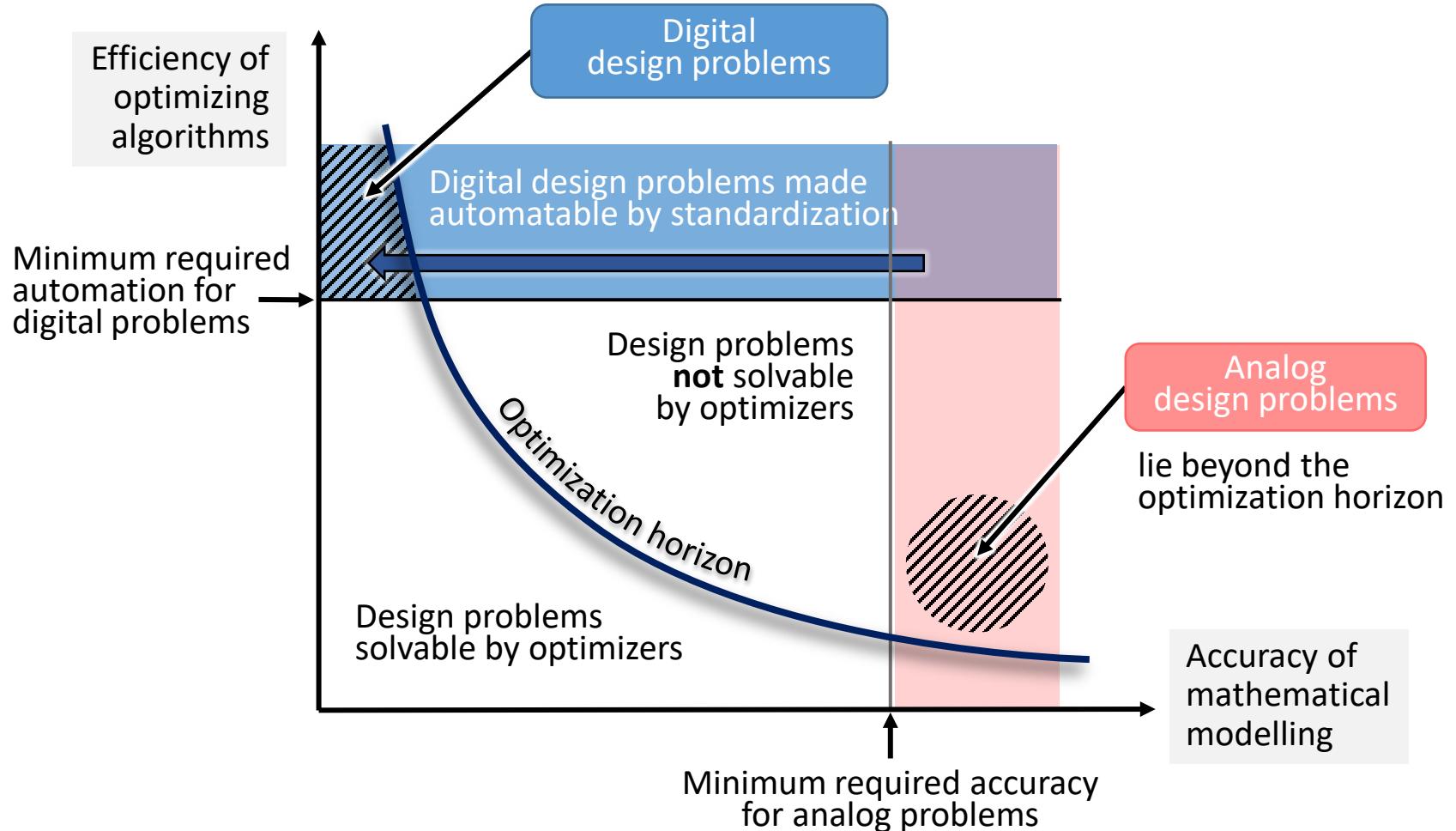
### Structural description

Block diagram  
Schematic, circuit diagram

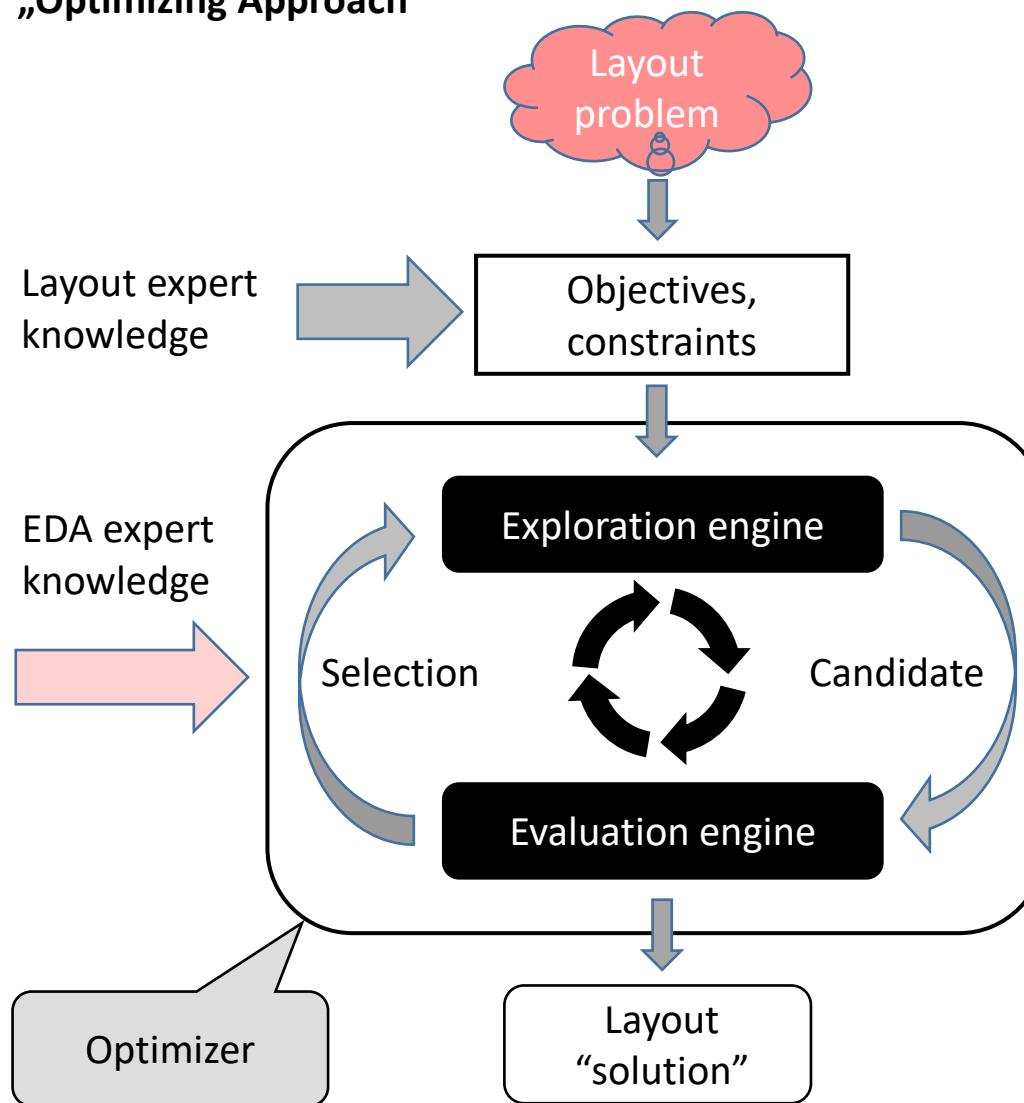
Device symbols  
Pins, diffusion areas  
Polygons  
Devices, device generators  
Blocks  
Floorplan

Geometrical/physical realization

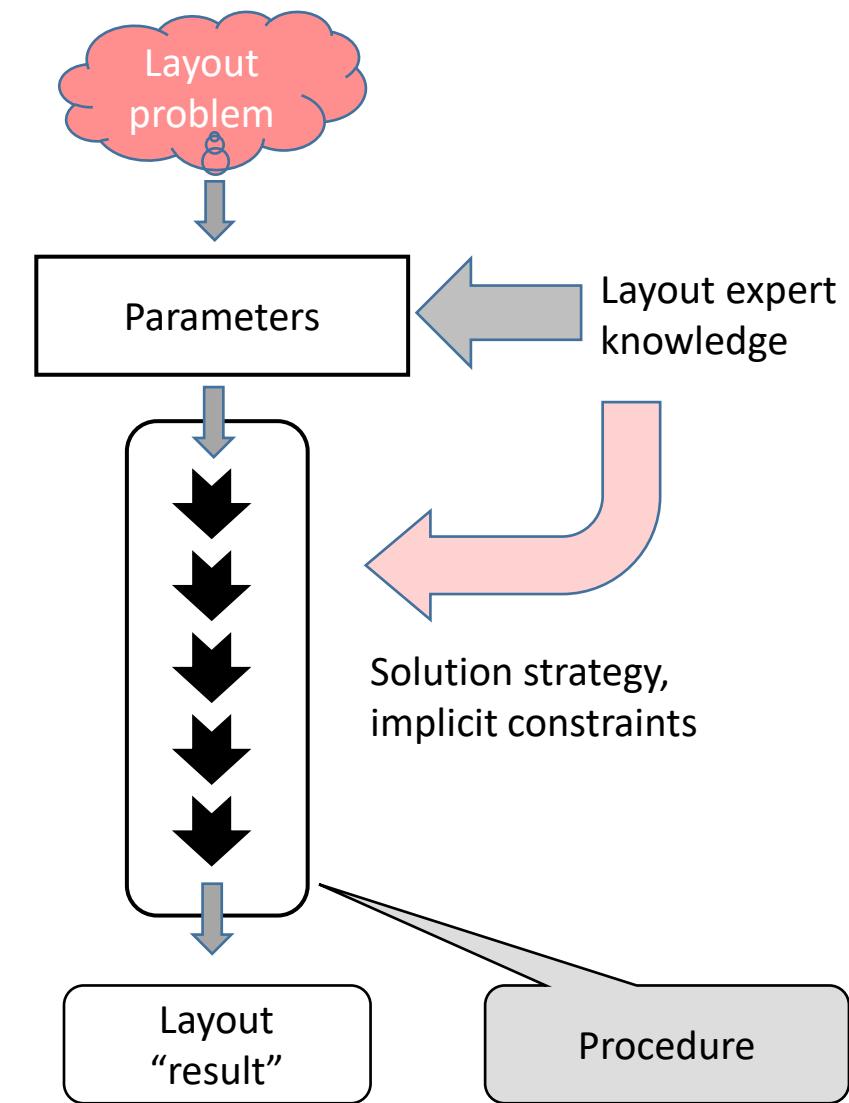


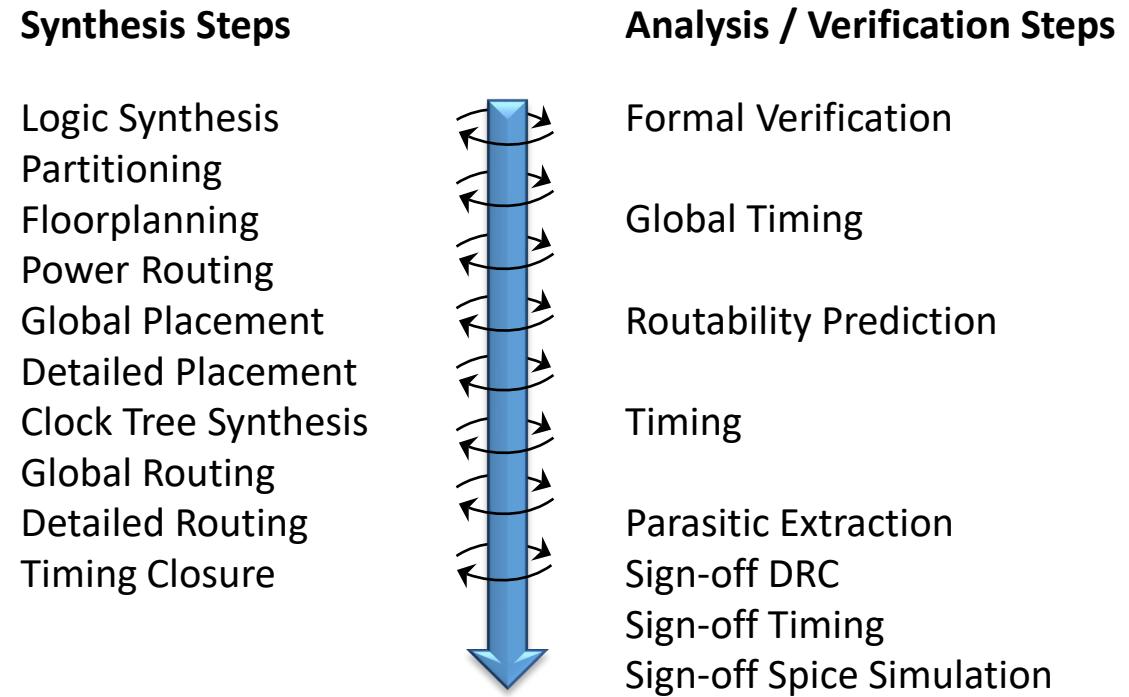


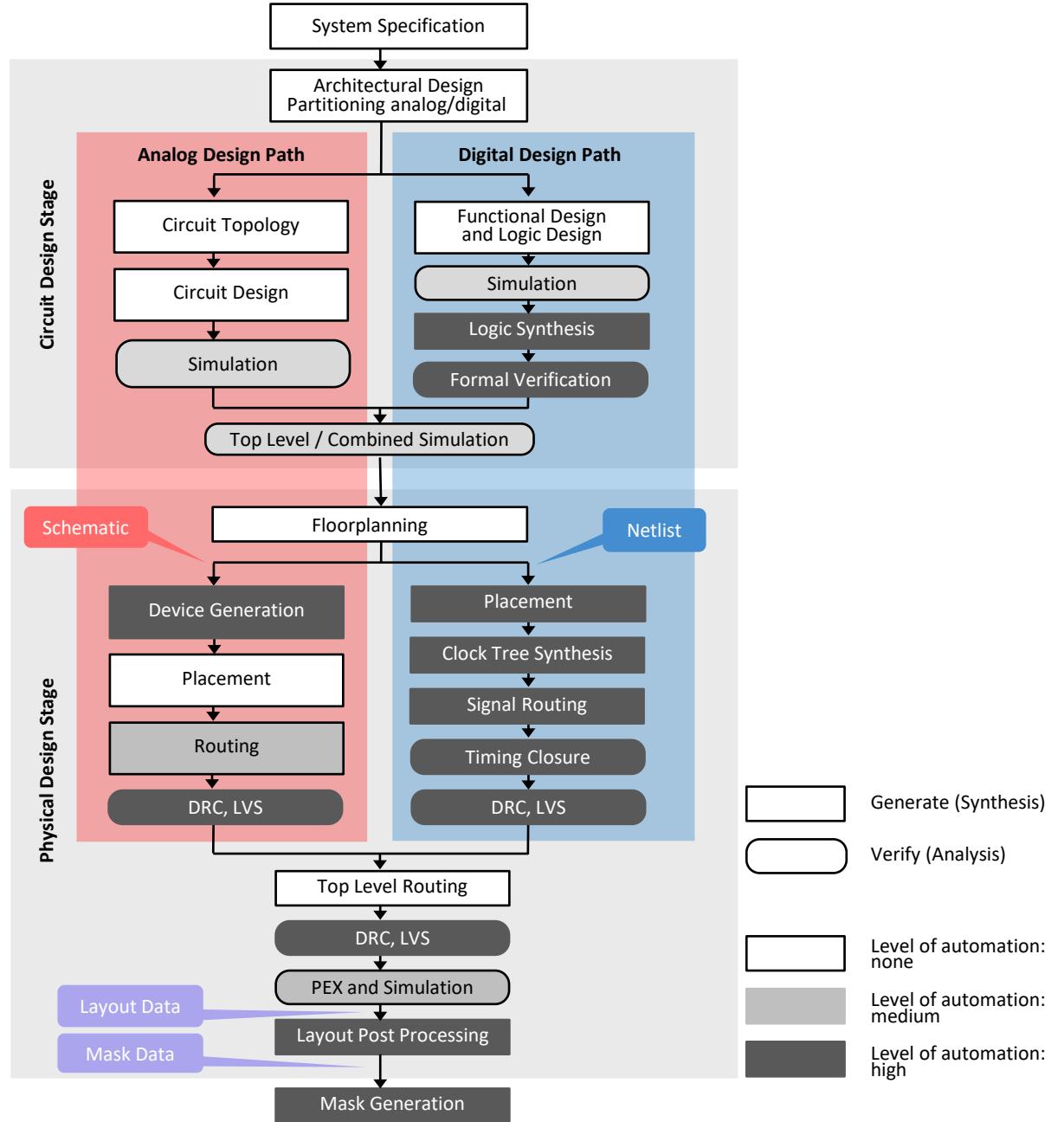
## Top-Down Design „Optimizing Approach“

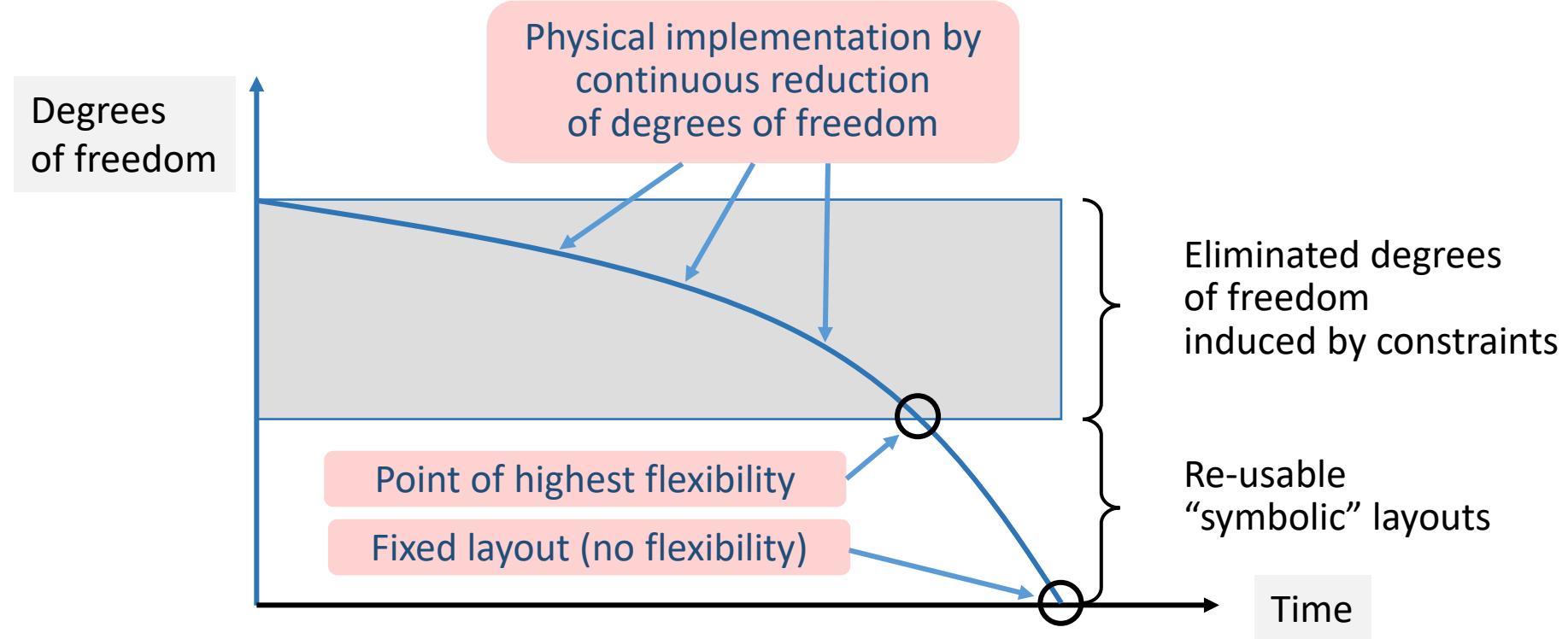


## Bottom-Up Design „Procedural Approach“

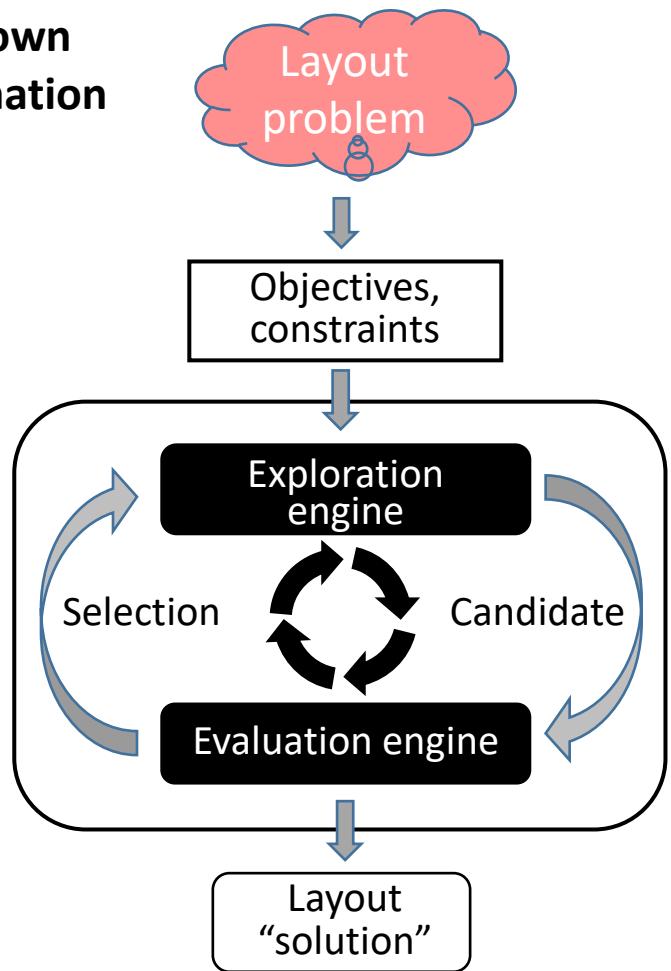








## Top-Down Automation



## Bottom-Up Automation

