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6.2 Wells
6.3 Devices: Layout, Connection, and Sizing
6.4 Cell Generators: From Parameters to Layout
6.5 The Importance of Symmetry
6.6 Layout Matching Concepts
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6.2 Wells
   6.2.1 Implementation
   6.2.2 Breakdown Voltage
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6.5 The Importance of Symmetry
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6.6 Layout Matching Concepts
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   6.6.6 Summary of Matching Concepts
Current $I$

Area $A$

Thickness $t$

Width $w$

Length $l$
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(a) $W_a = 2$

(b) $W_b = 1$

(c) $W_c = 1$

\[ R_a = R_b = 10R \]

\[ R_c = 10R - 2R / 2 \approx 9R \]
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Diagram (a): Any potential, n⁺ (NSD), p⁺ (PSD), Lightly doped n-well, p-epi or lightly doped p-substrate (p⁻-sub)

Diagram (b): n-well, p-well, p-epi or lightly doped p-substrate (p⁻-sub)

Diagram (c): Shallow trench isolation (STI), n-well, p-well, p-epi or lightly doped p-substrate (p⁻-sub)

Diagram (d): VDD, Deep-n⁺, p-epi, p⁺-substrate, p⁺-tub or p-tank, n-buried layer (NBL)

Diagram (e): Silicon on insulator (SOI), p-well, n-well, Oxide (SiO₂)
Star point connecting nets “SUB” and “GND”

“Ground” bondpad

Signal bondpads

Chp boundary

Separate net “SUB” for p-substrate tie down

Ground net “GND”

Circuit currents to GND

p-sub contact:

PSD

Active

Contact

Metal1

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Layout/top view:

- Layout shape of n-well
- Design rule spacing
- Outdiffusion
- Space-charge zone
- Electrical spacing
- Photo resist opening

Sectional view:

- n-well
- Space-charge regions
- p

Design rule spacing

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Diagram showing layout layers and components:
- **Active**
- **n⁺ (NSD)**
- **p⁺ (PSD)**
- **Poly**
- **Cont**
- **Metal1**

Key components and labels:
- D/S: Drain/Source
- G: Gate
- S/D: Source/Drain
- B: Body
- Nwell: N-well
- p-sub: p-substrate
- STI: Shallow Trench Isolation
- Cont: Contour lines
- Width (w)
- Length (l)
- Effective length (l_eff)

Cutting lines indicate layer separation and layout design considerations.
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(1) Split

(2) Flip

(3) Pack

(4) Route

Shared diffusion
Gate finger
Gate current $I_G$ vs. Gate finger length $l_G$

- $I_G$ vs. $l_G$
- Channel length $l$
- Gate finger

Electrical circuit:

- $I_G$
- $R_G$
- $C_{GB}$
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- **NSD resistor**
- **PSD resistor**
- **Nwell resistor**

- **p-sub contacts**
- **Well**
- **p-sub**
- **p-well**
- **PSD**
- **n-well**
- **NSD**
- **STI**
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Chapter 6: Special Layout Techniques for Analog IC Design
Chapter 6: Special Layout Techniques for Analog IC Design

- Polysilicon (Poly)
- Contacts (Pwell)
- Gate oxide
- Polysilicon (Poly)
- N+ ( NSD)
- P+ ( PSD)

**Cutting line**
- Width \( w \)
- Length \( l \)

**NMOS-Cap**
- Source (S)
- Drain (D)
- Gate (G)

**Components**
- C1
- C2
- Channel
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Chapter 6: Special Layout Techniques for Analog IC Design

Silicon Oxide

Metal3
Via2
CapMetal
Metal2
Capacitor top plate
Capacitor bottom plate
Capacitor dielectric
Oxide
Silicon

Width \( w \)
Length \( l \)

C1
C2

MIM

C1
C2

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Cutting line

Single emitter

Multi emitter

NBL
Deep-n+
Nwell
NSD
Active
Base
PSD

Emitter area

NSD
Base width
PSD

p-epi
p-sub
Deep-n+
NBL
Nwell
Base

C
E
B

STI
Chapter 6: Special Layout Techniques for Analog IC Design

Cutting line

NSD
NBL
Nwell
Active
Base
PSD

Base width

p-epi
NSD
p-sub
NBL
Base
Nwell
PSD

B
E
C

Layout layers
- Nwell
- Metal1
- Active
- Cont
- $n^+$ (NSD)
- NBL
- $p^+$ (PSD)
- Base

$B \rightarrow E \rightarrow C$

$B \rightarrow \text{Cont} \rightarrow E \rightarrow C$

$B \rightarrow \text{Nwell} \rightarrow E \rightarrow C$

$B \rightarrow \text{Base} \rightarrow E \rightarrow C$

$B \rightarrow \text{Active} \rightarrow E \rightarrow C$

$B \rightarrow \text{PSD} \rightarrow E \rightarrow C$

$B \rightarrow \text{NSD} \rightarrow E \rightarrow C$

$B \rightarrow \text{p-epi} \rightarrow E \rightarrow C$

$B \rightarrow \text{STI} \rightarrow E \rightarrow C$
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Primitive device library

Symbol | Model | Layout

Cell generator

Process design kit (PDK)
<table>
<thead>
<tr>
<th>Command</th>
<th>Line</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Active = list(&quot;Oxide&quot;; &quot;drawing&quot;); Poly = list(&quot;Poly&quot;; &quot;drawing&quot;); NSD = list(&quot;Nimp&quot;; &quot;drawing&quot;); PSD = list(&quot;Pimp&quot;; &quot;drawing&quot;); &quot;Create initial shapes.&quot;</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>&quot;Create initial shapes.&quot;</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>GroupName</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>layerName {coordinates x1:y1, x2:y2, x3:y3, x4:y4}</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Create 5 rectangles for MOS-FET core</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Create 3 rectangles for left bulk contact</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Create 3 rectangles for right bulk contact</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Calculate stretch lengths</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>Perform stretch operations</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>GroupName</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>Copy (fingers-1) times the MOS-FET core with (fpitch) in x-direction</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>Move right bulk (fpitch) in x-direction</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>Delete bulk contacts depending on values of &quot;leftBulk&quot; and &quot;rightBulk&quot;</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>Create 1 dummy contact</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>Fill all Metal1 with this contact shape</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>Delete dummy contact</td>
<td></td>
</tr>
</tbody>
</table>

Chapter 6: Special Layout Techniques for Analog IC Design

Initial layout:
- BulkLeft
- Core
- BulkRight
- Active
- n⁺ (NSD)
- p⁺ (PSD)
- Poly
- Metal1
- Cont

PCell menu:
- Width: 2 μm
- Length: 400 nm
- Fingers: 2

Generated PCell instance:
- PCell menu:
- Width: 2 μm
- Length: 400 nm
- Fingers: 2

<table>
<thead>
<tr>
<th>Manufacturing-specific “distance” (fabrication history)</th>
<th>Relative accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td>Within a fab</td>
<td>± 30%</td>
</tr>
<tr>
<td>Within a lot</td>
<td>± 20%</td>
</tr>
<tr>
<td>Within a wafer</td>
<td>± 15%</td>
</tr>
<tr>
<td>Within a reticle</td>
<td>± 10%</td>
</tr>
<tr>
<td>Within a chip</td>
<td>± 5%</td>
</tr>
<tr>
<td>Within a chip with further layout measures</td>
<td>± 1% to ± 0.01%</td>
</tr>
</tbody>
</table>
Chapter 6: Special Layout Techniques for Analog IC Design
Resistor body

Resistor head

Contact hole

\[ l_1 = 3 \]

\[ l_2 = 1 \]

\[ R_1 < 3R_2 \rightarrow \text{no matching!} \]

\[ R_1 \approx 3R_2 \rightarrow \text{bad matching!} \]

\[ l_{corr} \]

\[ l_1 \]

\[ 3 \]

\[ l_2 \]

\[ R_1 \]

\[ R_2 \]

Metal 1

\[ l_{1a,b,c} = 1 \]

\[ R_{1a} \]

\[ R_{1b} \]

\[ R_{1c} \]

\[ R_2 \]

\[ l_2 = 1 \]

\[ R_1 = 3R_2 \rightarrow \text{good matching!} \]
Current mirror circuit

No splitting ➔ **bad matching!**

Splitting ➔ **good matching!**
Chapter 6: Special Layout Techniques for Analog IC Design

Minimum matching

Good matching

Very good matching
Multi-emitter PNP transistor

Multi-collector PNP transistor
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Die

Circuit block

Large distance

Bad matching

Minimum distance

Good matching

Very good matching

Common centroid

(I)

A1 A2 B

(II)

A1 B A2

Die

Circuit block

Wafer

A1

A2

B

x

y

x

y

x

y

x

x1 x2 x3
Interdigitated layout

Common centroid layout

Current mirror schematic

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Chapter 6: Special Layout Techniques for Analog IC Design

Thermal distribution

Power transistor
Thermal gradient
Isotherm

Heat source
Good matching
Bad matching

Mechanical stress

Highest stress gradient
Isobar
Centerlines

Bad matching
Best matching
Good matching
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Misalignment of contact

Affected resistor
Not affected resistor

Bad matching

Both resistors are affected in the same way

Good matching

Good matching
Chapter 6: Special Layout Techniques for Analog IC Design

Good matching

Antiparallel current flow

Hot

Cold

Parallel current flow

Bad matching

Geometrical symmetry

“Matching” symmetry

Symmetry axis

Device A

S

D

Device B

S

D

Hot

Cold

Bad matching

Good matching
(a) **Matching for normal requirements**

<table>
<thead>
<tr>
<th>Devices</th>
<th>Effect / explanation</th>
</tr>
</thead>
<tbody>
<tr>
<td>All</td>
<td>Prerequisite for matching!</td>
</tr>
<tr>
<td>All</td>
<td>Internal device fringe effects</td>
</tr>
<tr>
<td></td>
<td>(Sect. 6.6.1)</td>
</tr>
<tr>
<td>All</td>
<td>Unknown gradients (Sect. 6.6.2)</td>
</tr>
<tr>
<td>R, T</td>
<td>Alignment tolerances, carrier mobility</td>
</tr>
<tr>
<td></td>
<td>(Sect. 6.6.5)</td>
</tr>
<tr>
<td>C</td>
<td>Internal device fringe effects</td>
</tr>
<tr>
<td></td>
<td>(Sect. 6.6.1)</td>
</tr>
</tbody>
</table>

(b) **Matching for higher requirements**

<table>
<thead>
<tr>
<th>Devices</th>
<th>Effect / explanation</th>
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<tbody>
<tr>
<td>All</td>
<td>Unknown gradients (Sect. 6.6.2)</td>
</tr>
<tr>
<td>All</td>
<td>Thermal gradient (known gradient)</td>
</tr>
<tr>
<td></td>
<td>(Sect. 6.6.4)</td>
</tr>
<tr>
<td>All</td>
<td>External device fringe effects</td>
</tr>
<tr>
<td></td>
<td>(Sect. 6.6.3)</td>
</tr>
<tr>
<td>R, T</td>
<td>Thermoelectric effect (Sect. 6.6.5)</td>
</tr>
<tr>
<td>R, T</td>
<td>Internal device fringe effects</td>
</tr>
<tr>
<td></td>
<td>(Sect. 6.6.1)</td>
</tr>
<tr>
<td>M</td>
<td>Well proximity effect (Sect. 6.6.3)</td>
</tr>
</tbody>
</table>

(c) **Matching for highest requirements**

<table>
<thead>
<tr>
<th>Devices</th>
<th>Effect / explanation</th>
</tr>
</thead>
<tbody>
<tr>
<td>All</td>
<td>Unknown gradients (Sect. 6.6.2)</td>
</tr>
<tr>
<td>All</td>
<td>Carrier mobility (Sect. 6.6.5)</td>
</tr>
<tr>
<td>All</td>
<td>Depending on circuit function</td>
</tr>
</tbody>
</table>