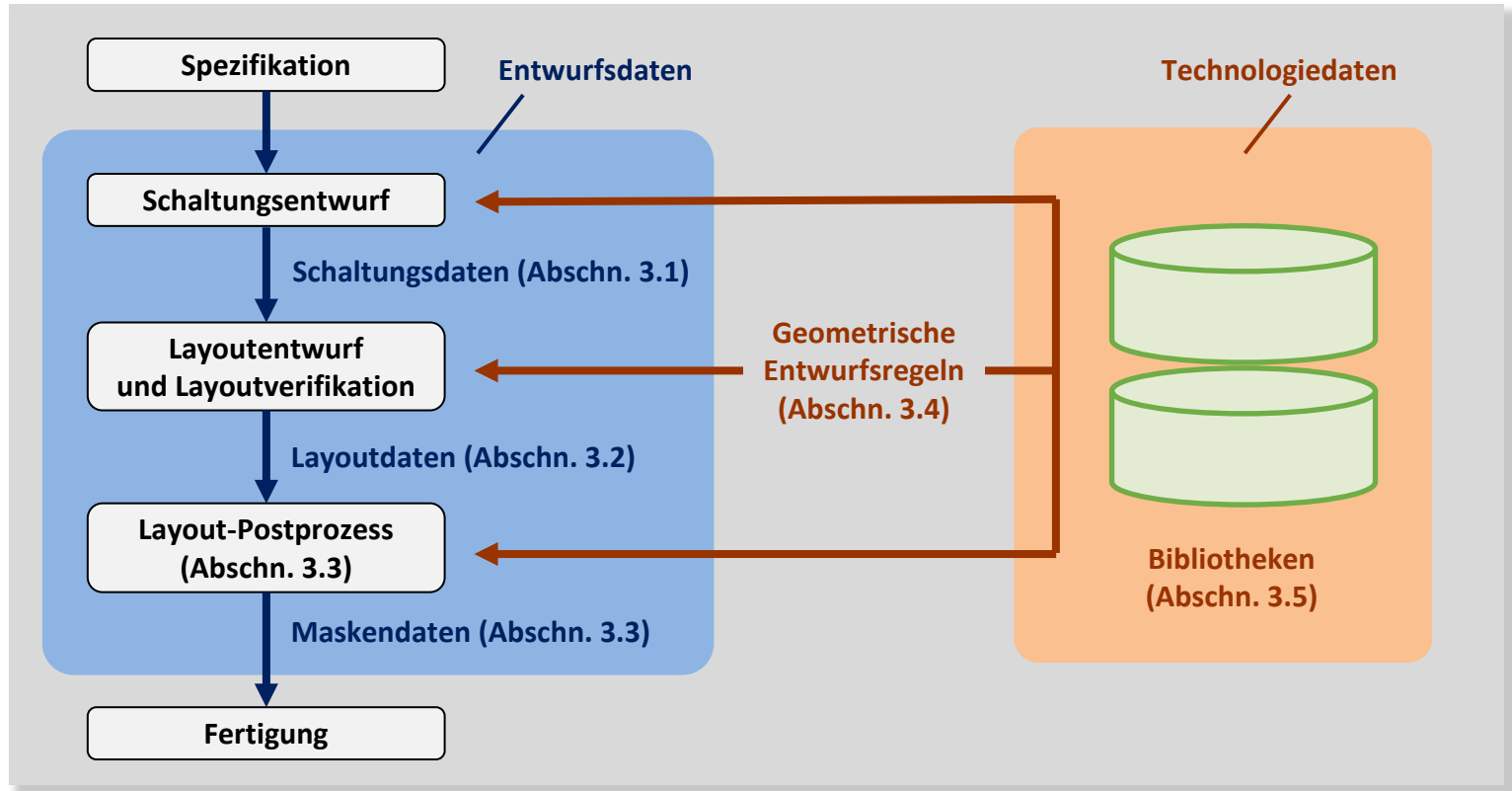
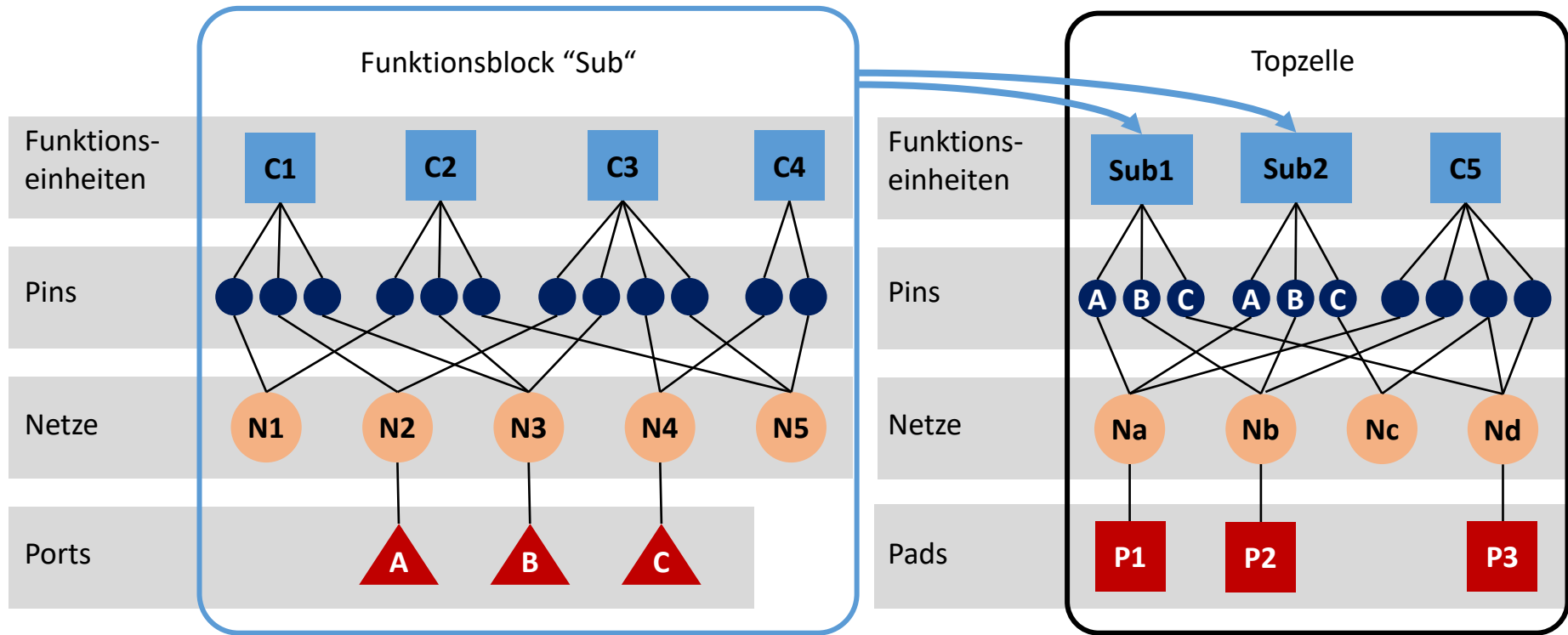
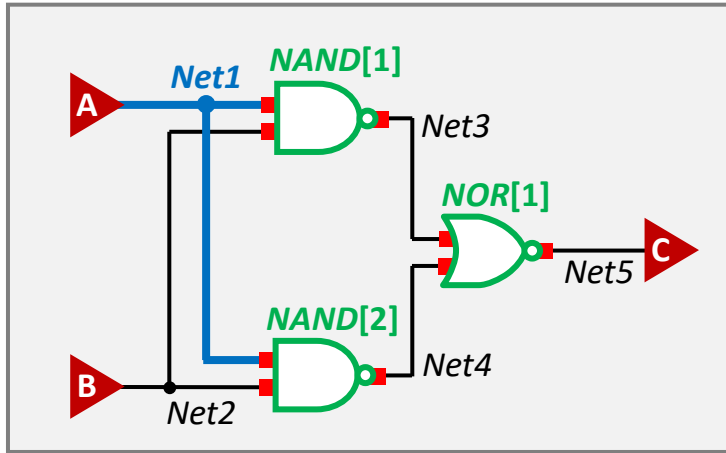


- 3.1 Schaltungsdaten: Schaltpläne und Netzlisten
- 3.2 Layoutdaten: Layer und Polygone
- 3.3 Maskendaten: Layout-Postprozess
- 3.4 Geometrische Entwurfsregeln
- 3.5 Bibliotheken









Pinorientierte Netzliste

(A: **Net1**)

(B: Net2)

(C: Net5)

(NAND[1]: IN1 **Net1**, IN2 Net2, OUT Net3)

(NAND[2]: IN1 **Net1**, IN2 Net2, OUT Net4)

(NOR[1]: IN1 Net3, IN2 Net4, OUT Net5)

Netzorientierte Netzliste

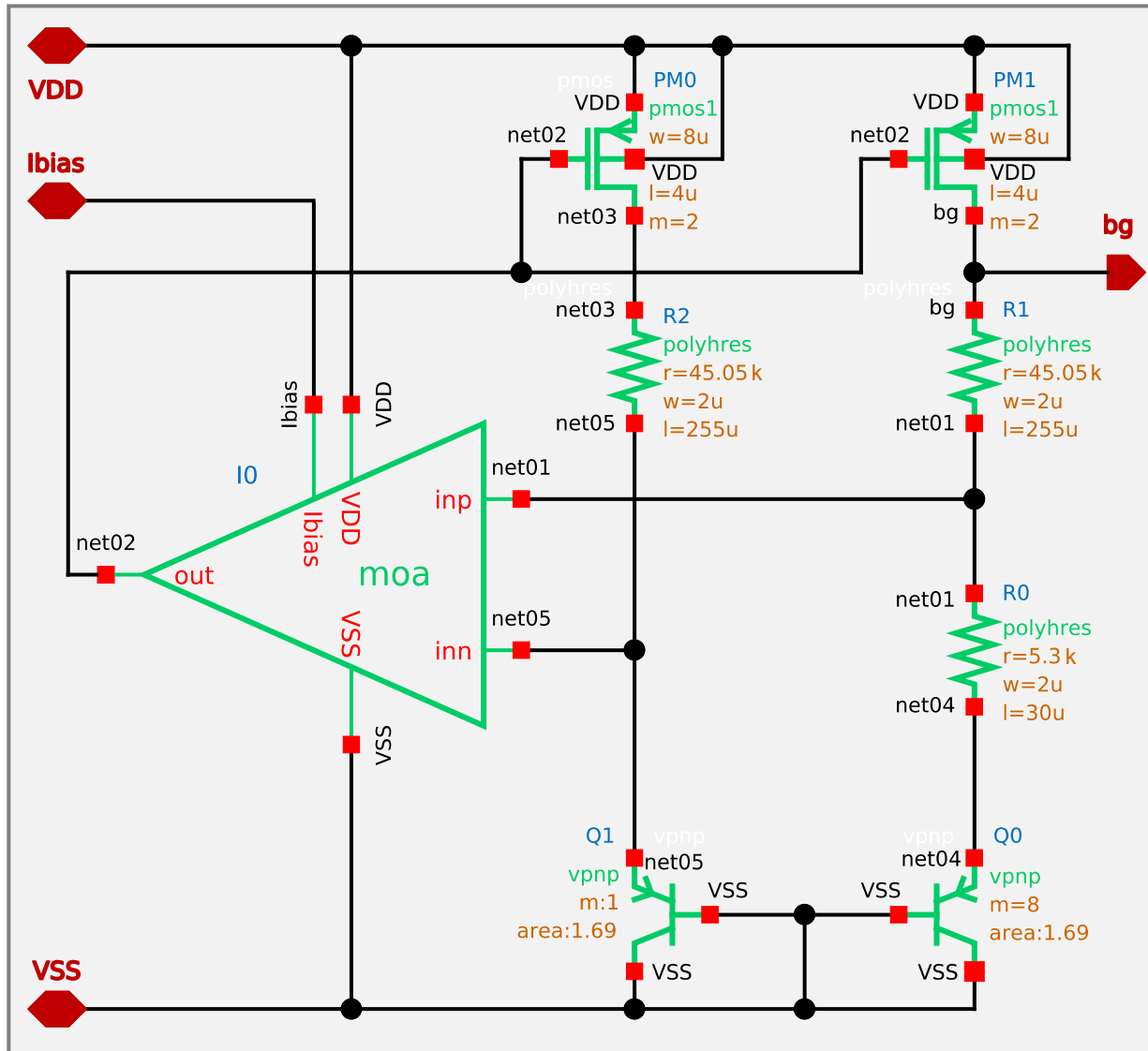
(**Net1**: A, NAND[1].IN1, NAND[2].IN1)

(Net2: B, NAND[1].IN2, NAND[2].IN2)

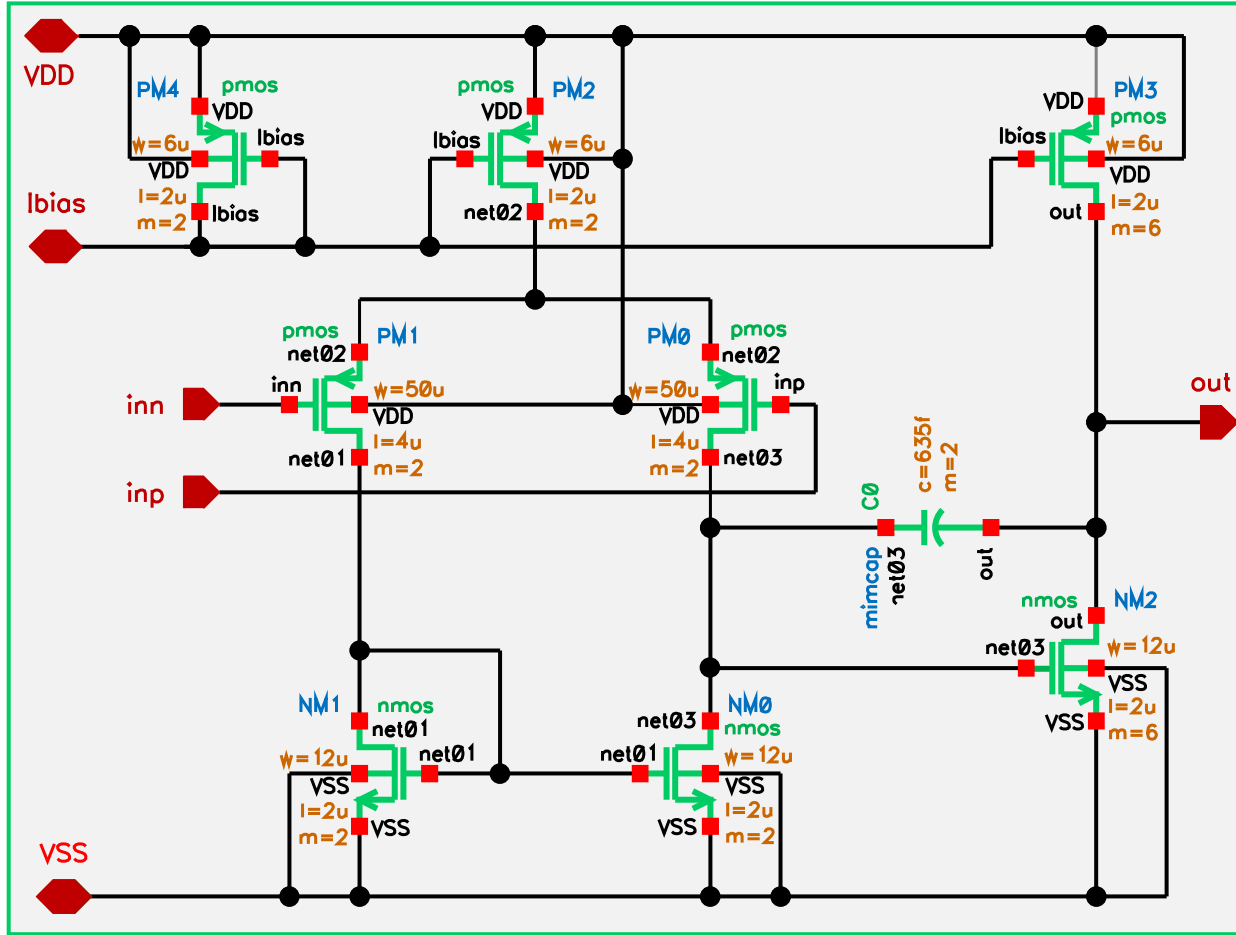
(Net3: NAND[1].OUT, NOR[1].IN1)

(Net4: NAND[2].OUT, NOR[1].IN2)

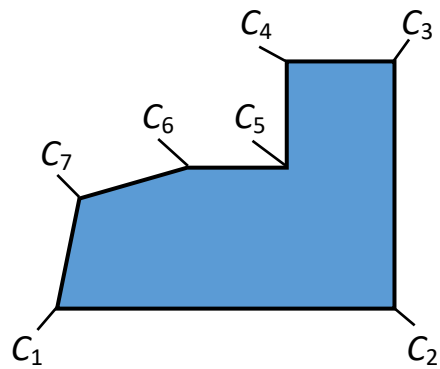
(Net5: NOR[1].OUT, C)



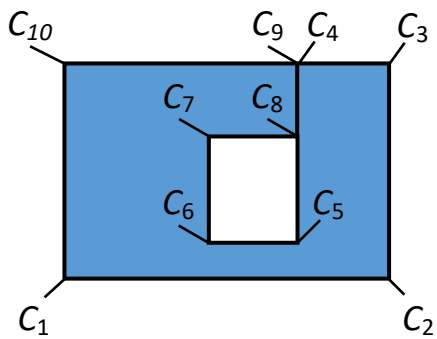
```
.SUBCKT bgap Ibias VDD VSS bg
QQ1 VSS VSS net05 vnpn M=1 EA=1.69
QQ0 VSS VSS net04 vnpn M=8 EA=1.69
XI0 Ibias VDD VSS net05 net01 net02 / moa
MPM1 bg net02 VDD VDD pmos W=8u L=4u M=2
MPM0 net03 net02 VDD VDD pmos W=8u L=4u M=2
RR2 net03 net05 45.05k polyhres W=2u L=255u
RR1 bg net01 45.05k polyhres W=2u L=255u
RR0 net01 net04 5.3k polyhres W=2u L=30u
.ENDS
```



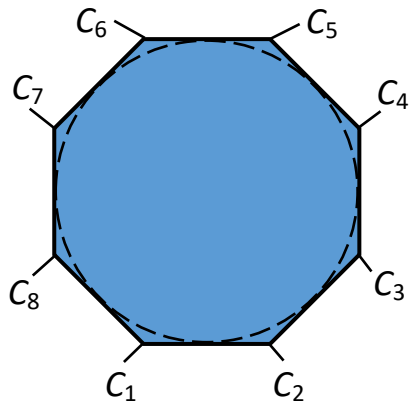
```
.SUBCKT moa Ibias VDD VSS inn inp out
MPM4 Ibias Ibias VDD VDD pmos W=6u L=2u M=2
MPM3 out Ibias VDD VDD pmos W=6u L=2u M=6
MPM0 net03 inp net02 VDD pmos W=50u L=4u M=2
MPM1 net01 inn net02 VDD pmos W=50u L=4u M=2
MPM2 net02 Ibias VDD VDD pmos W=6u L=2u M=2
MNM2 out net03 VSS VSS nmos W=12u L=2u M=6
MNM1 net01 net01 VSS VSS nmos W=12u L=2u M=2
MNM0 net03 net01 VSS VSS nmos W=12u L=2u M=2
CC0 net03 out 635f mimcap M=2
.ENDS
```



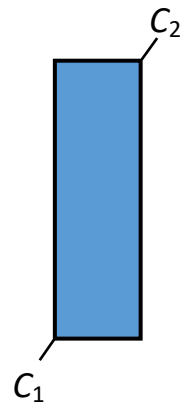
(a)



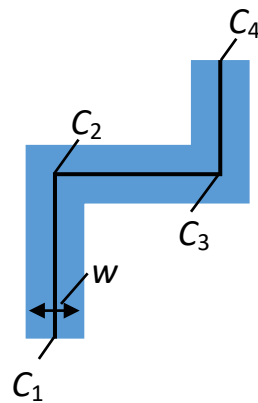
(b)



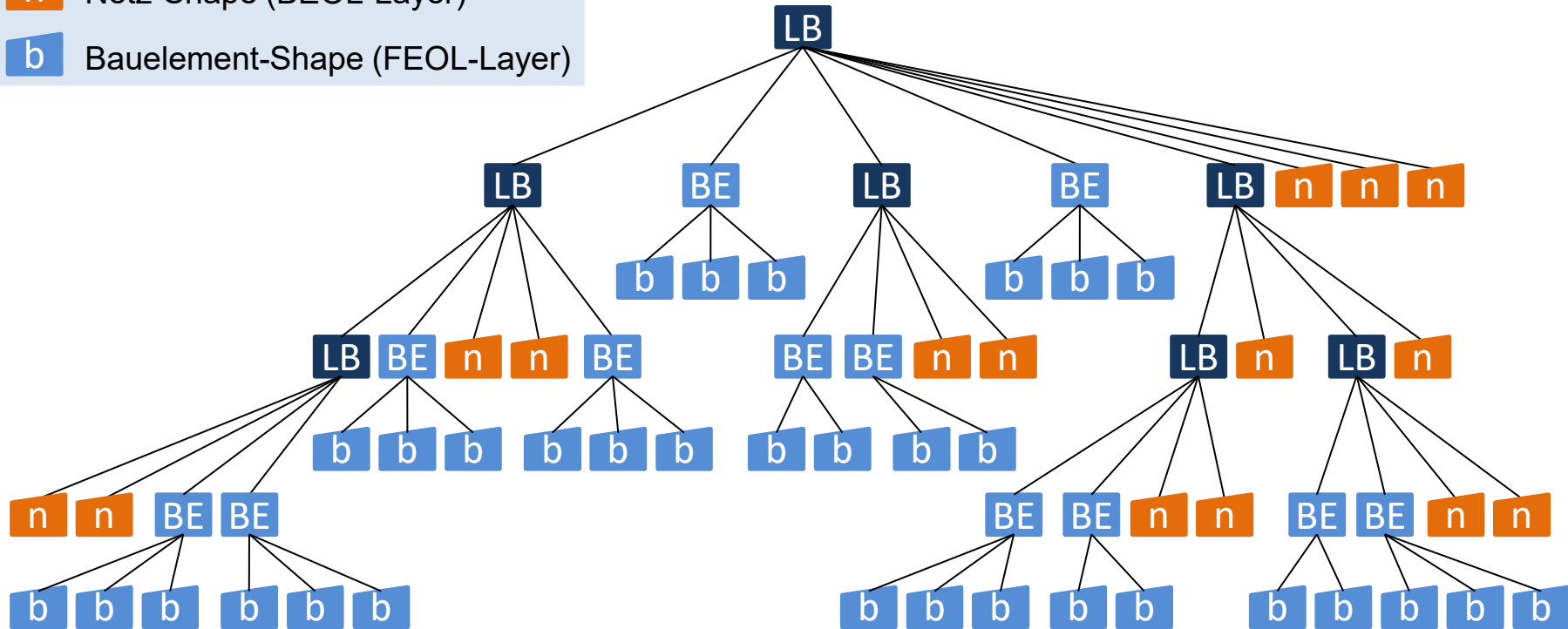
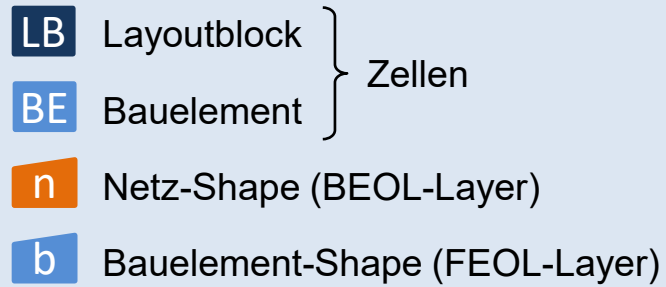
(c)



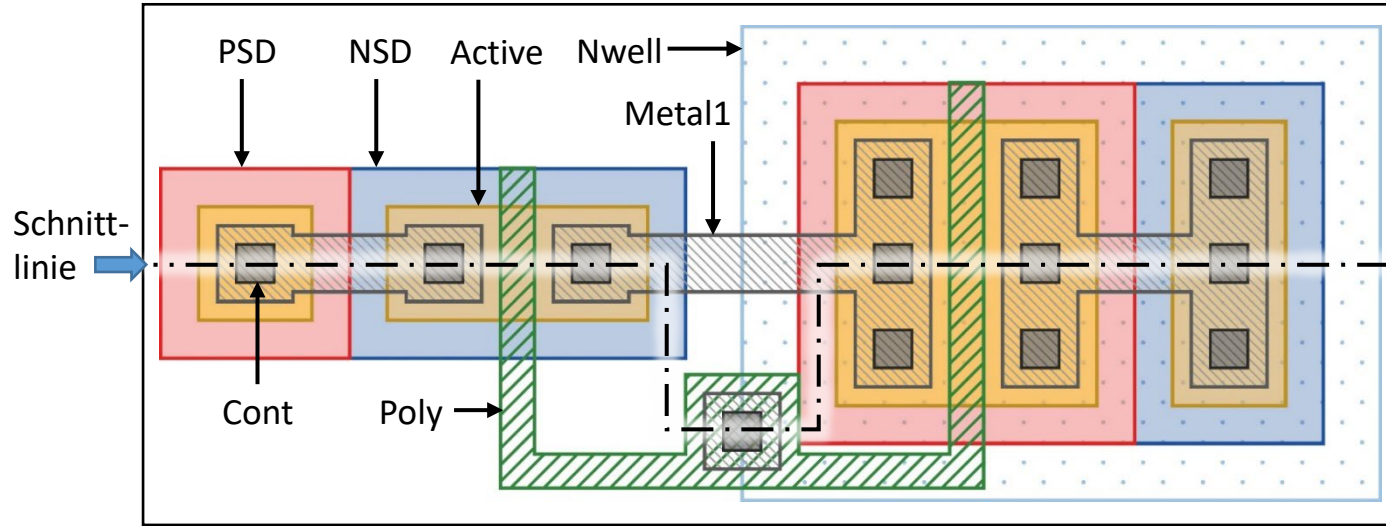
(d)



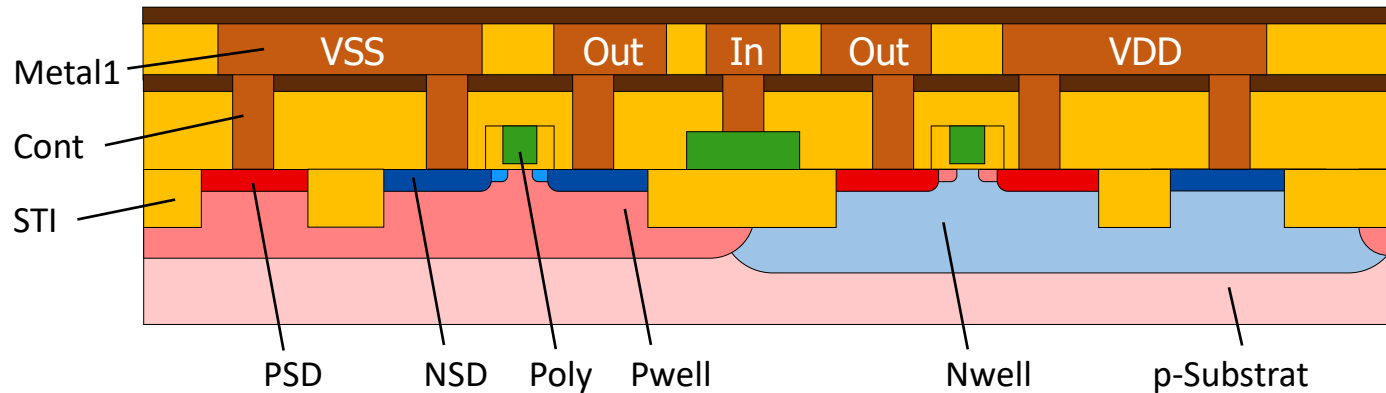
(e)



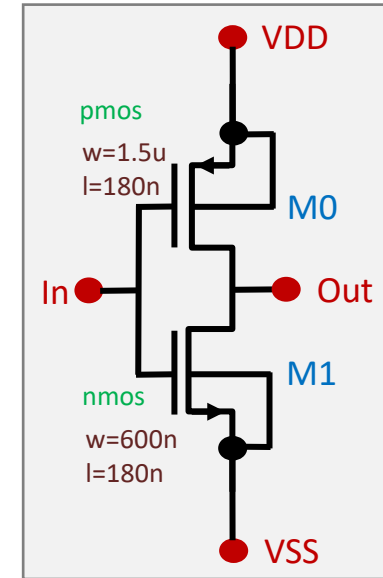
Layoutdarstellung

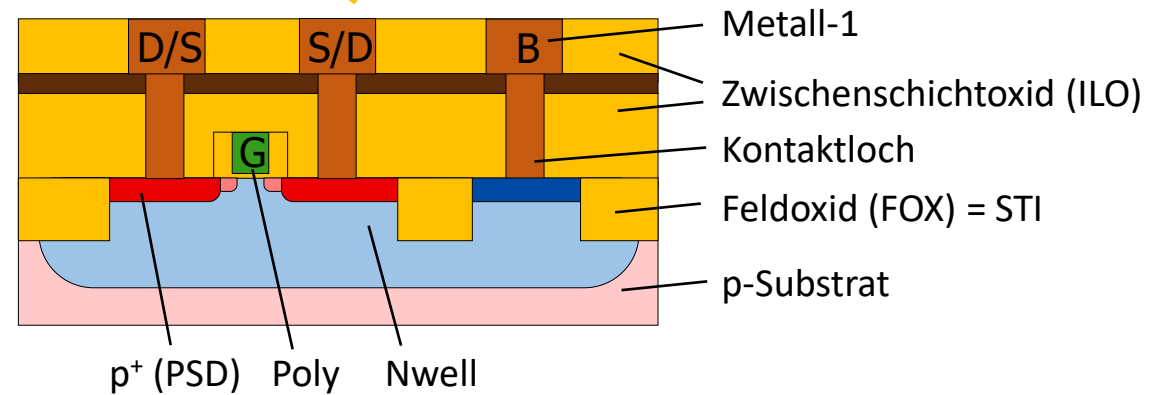
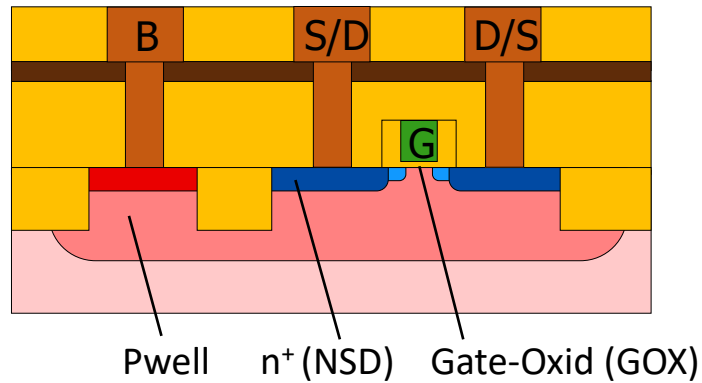
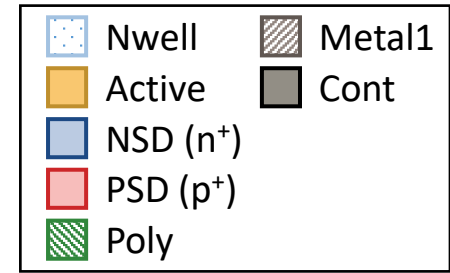
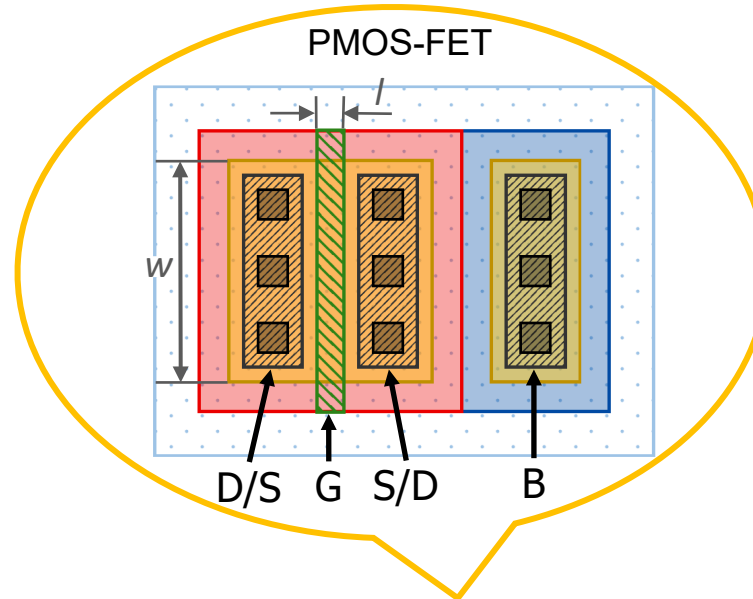
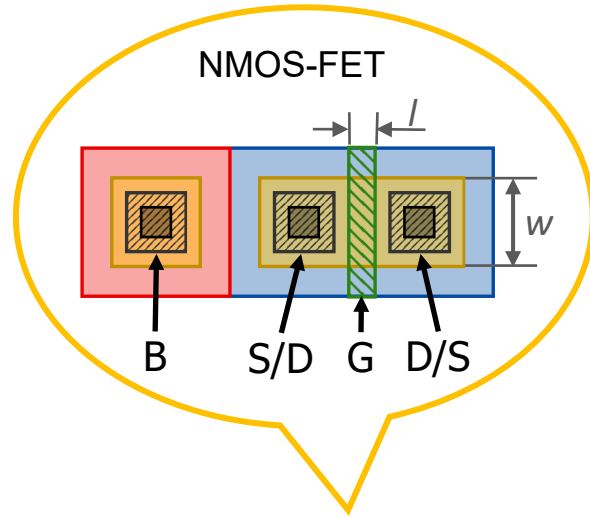


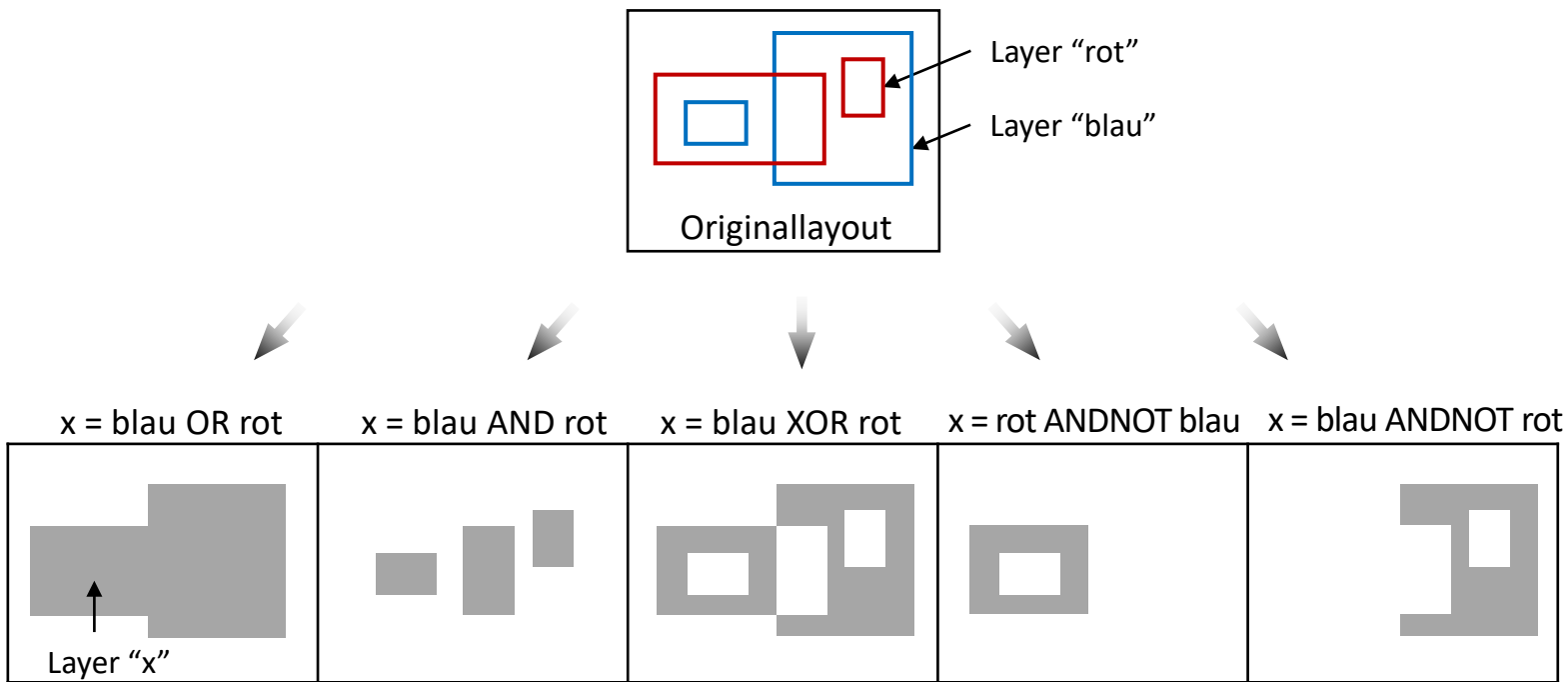
Querschnittsdarstellung

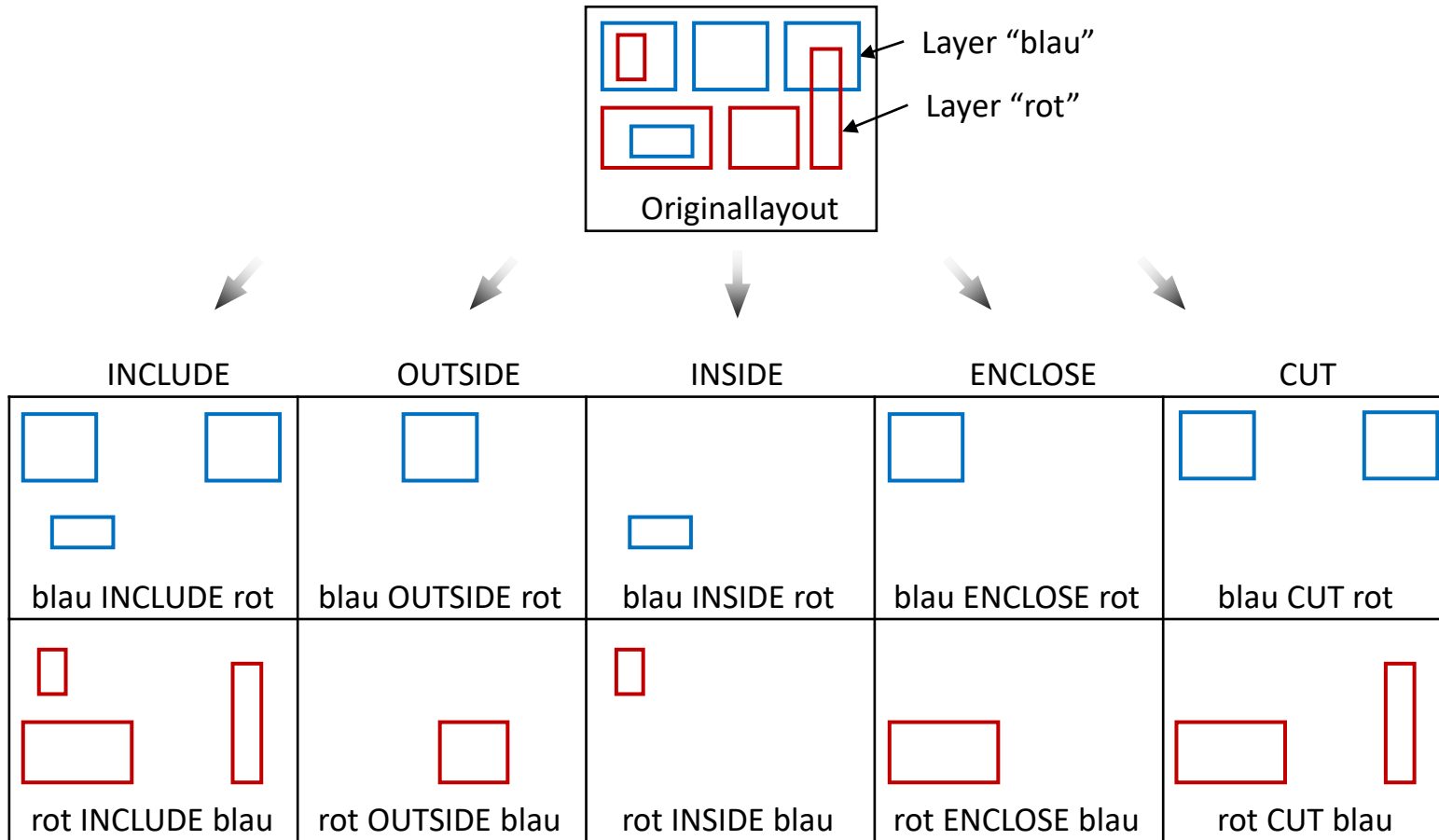


Schaltplandarstellung

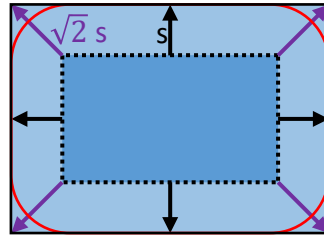




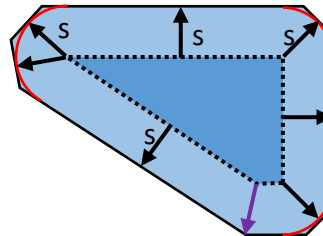
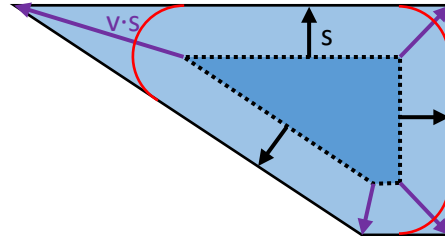
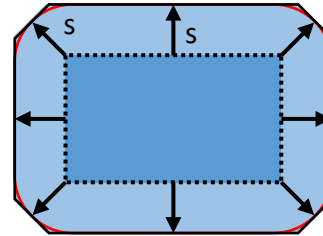


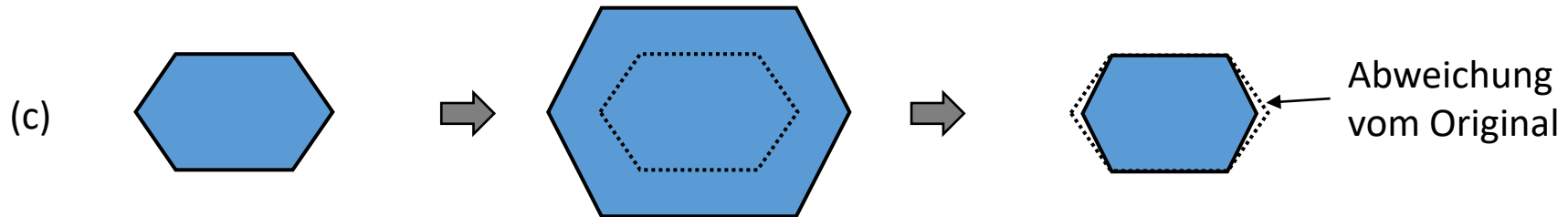
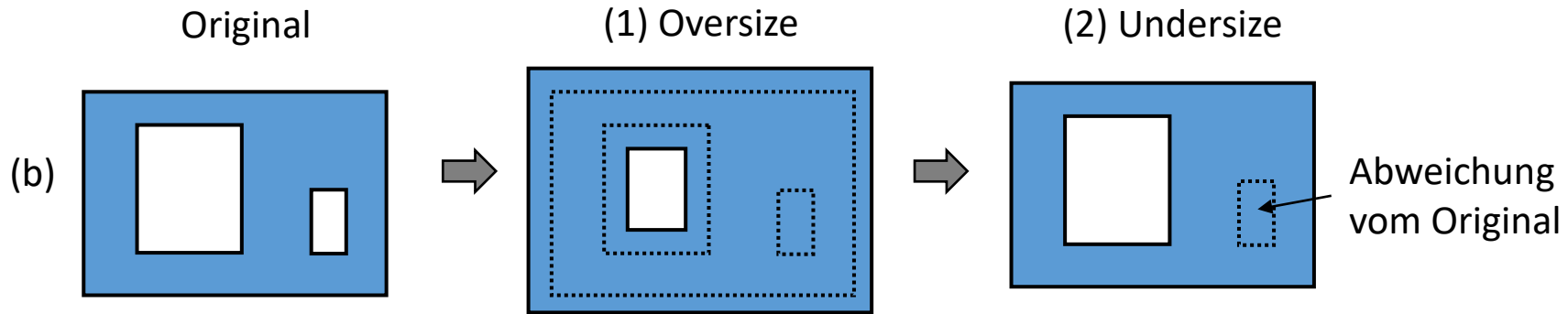
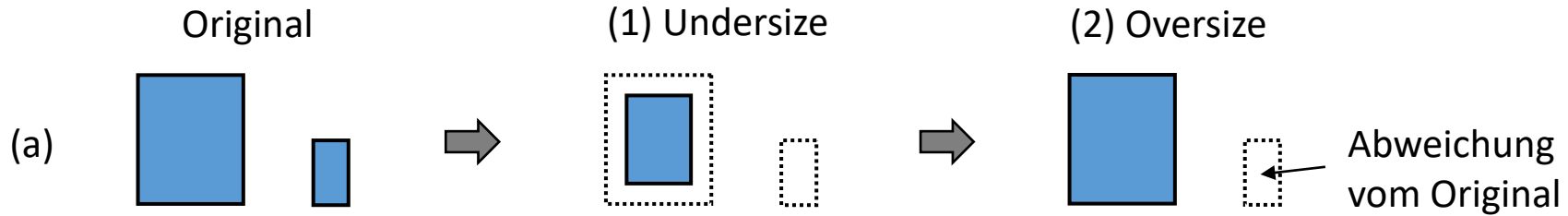


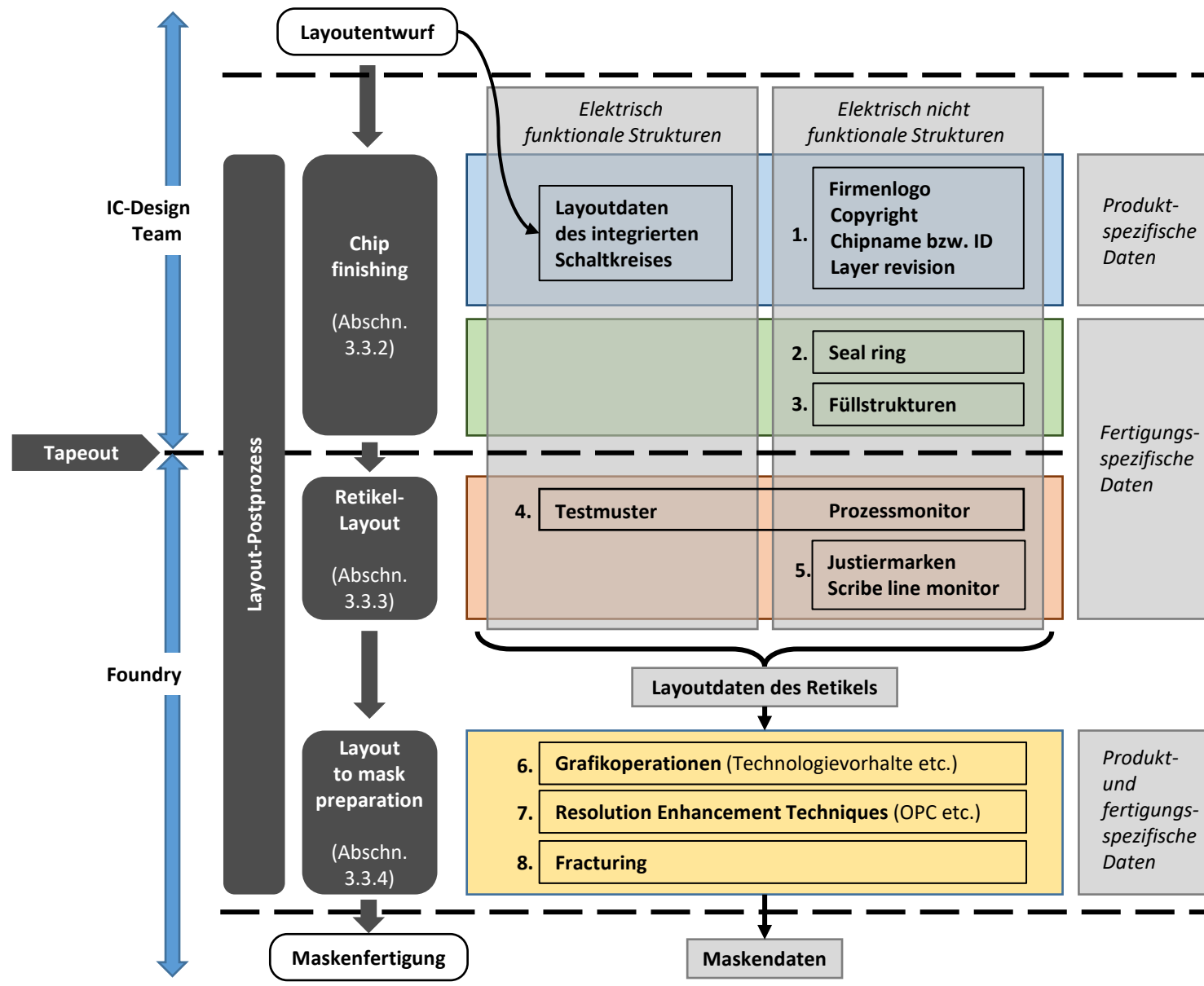
Sizing ohne Abschrägung

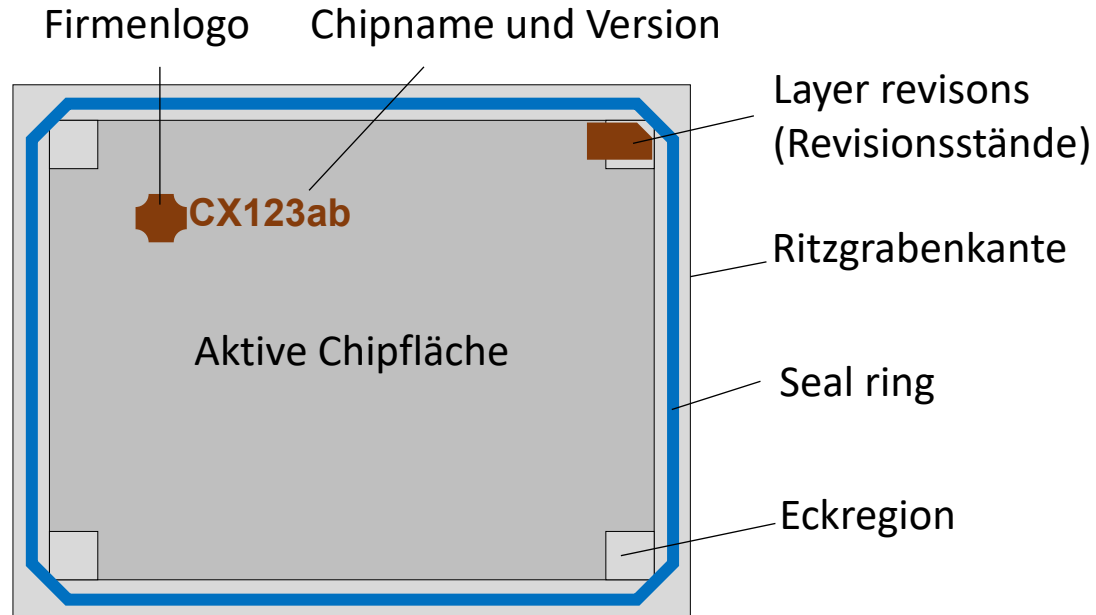


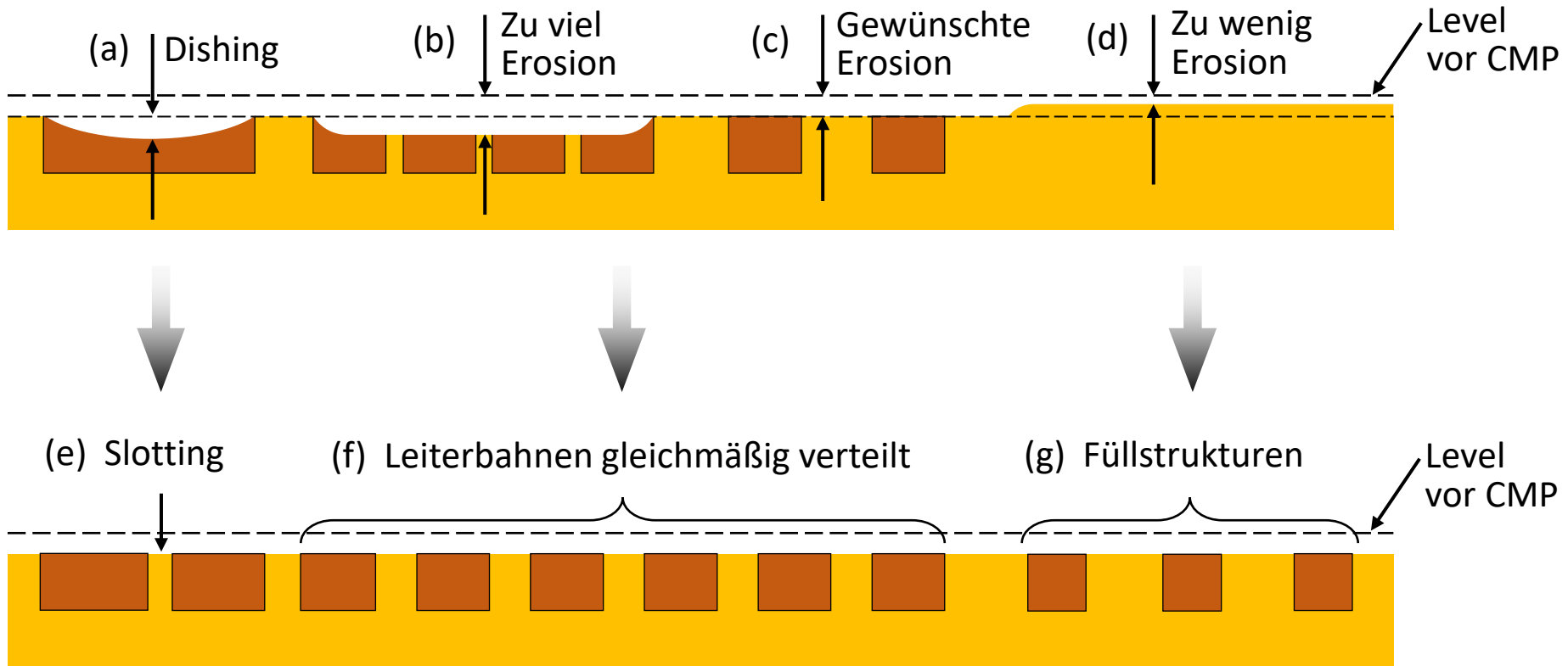
Sizing mit Abschrägung

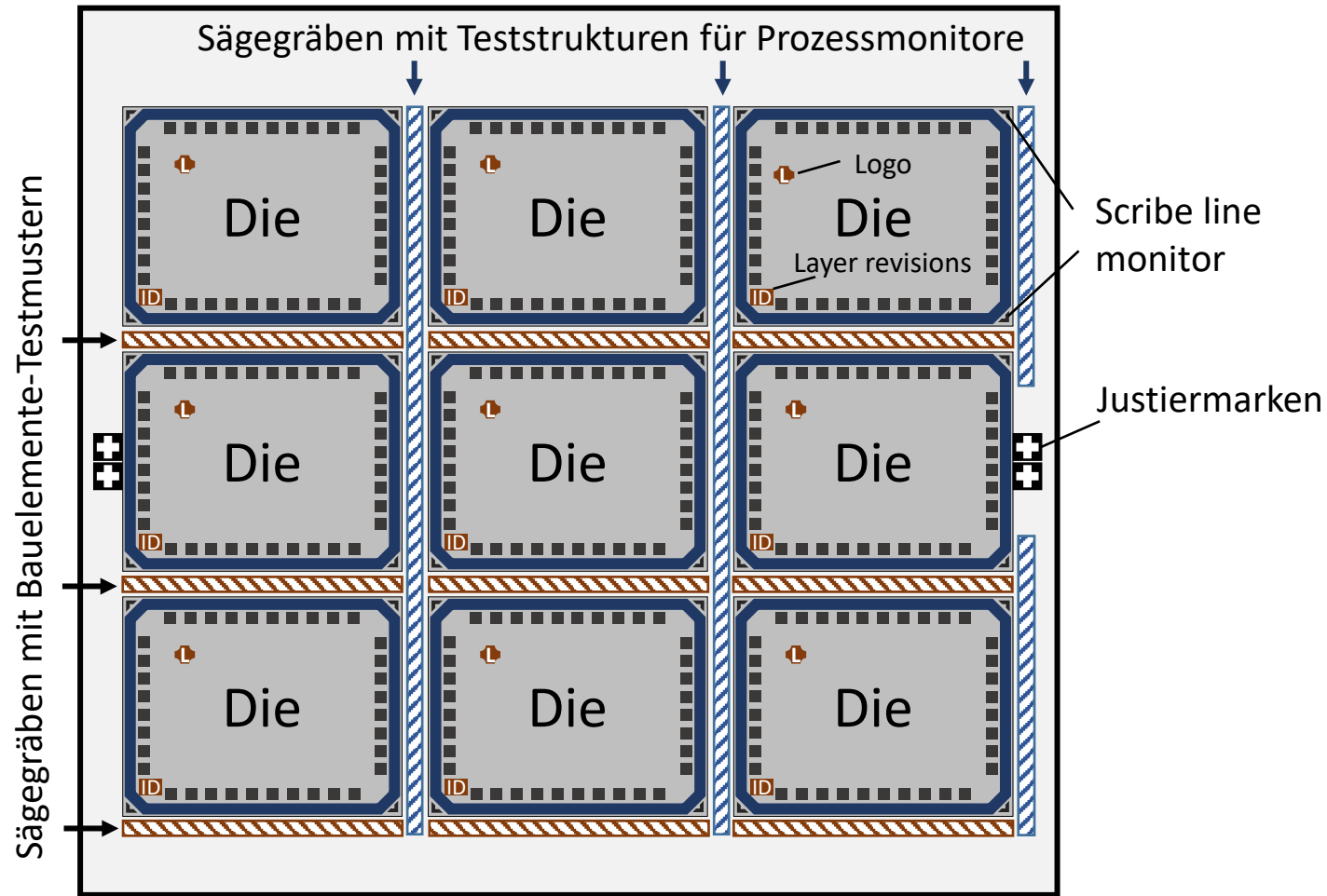




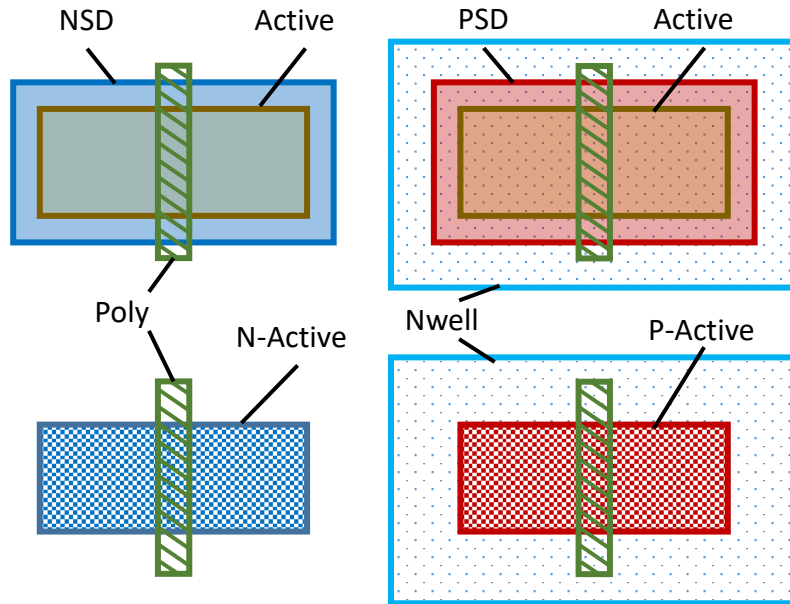






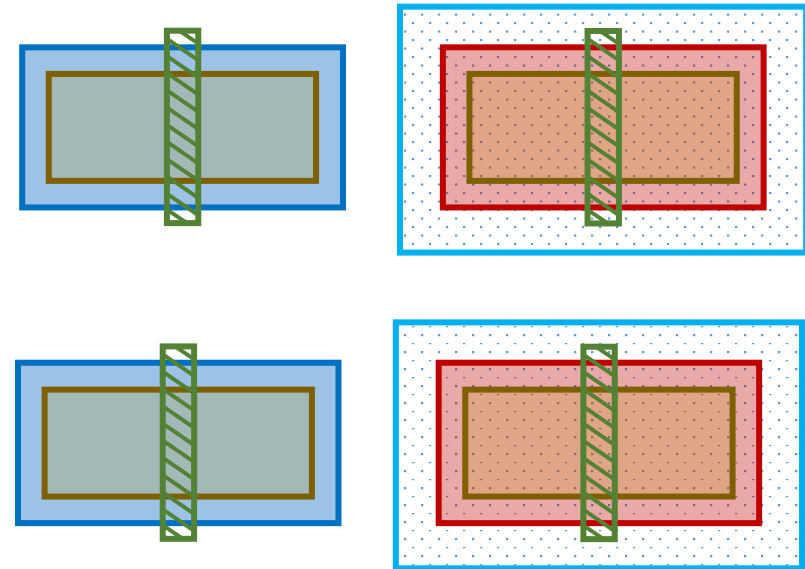


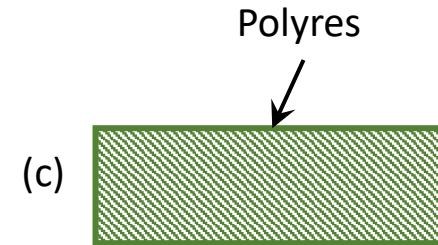
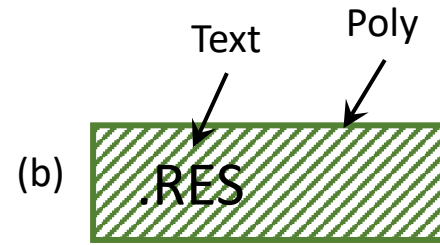
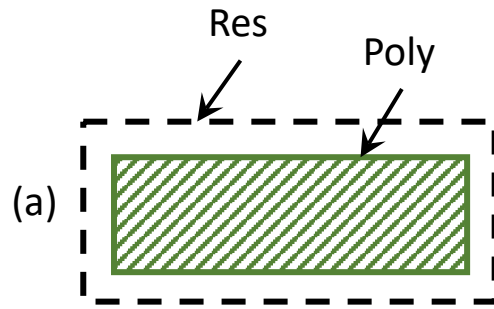
Layoutdaten

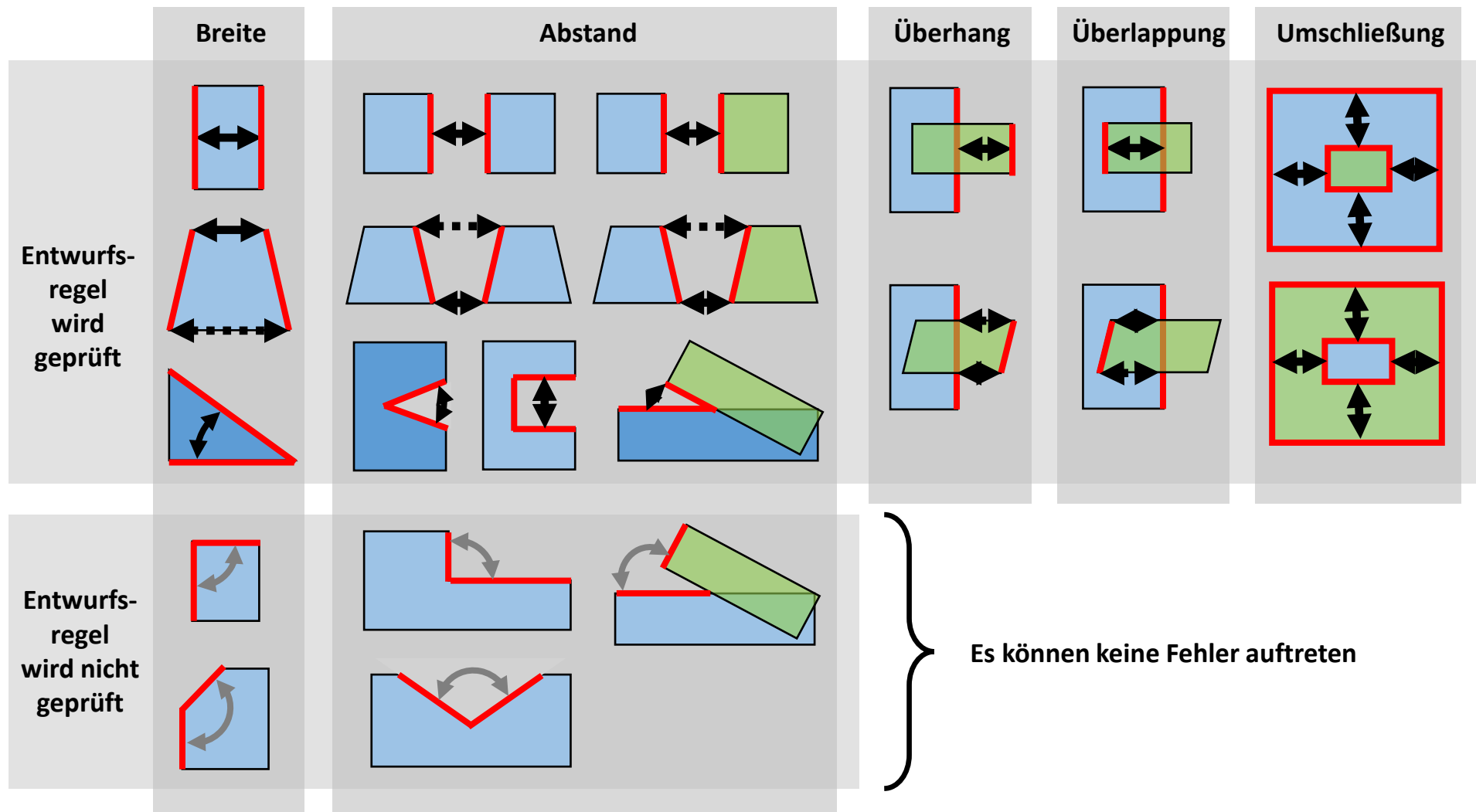


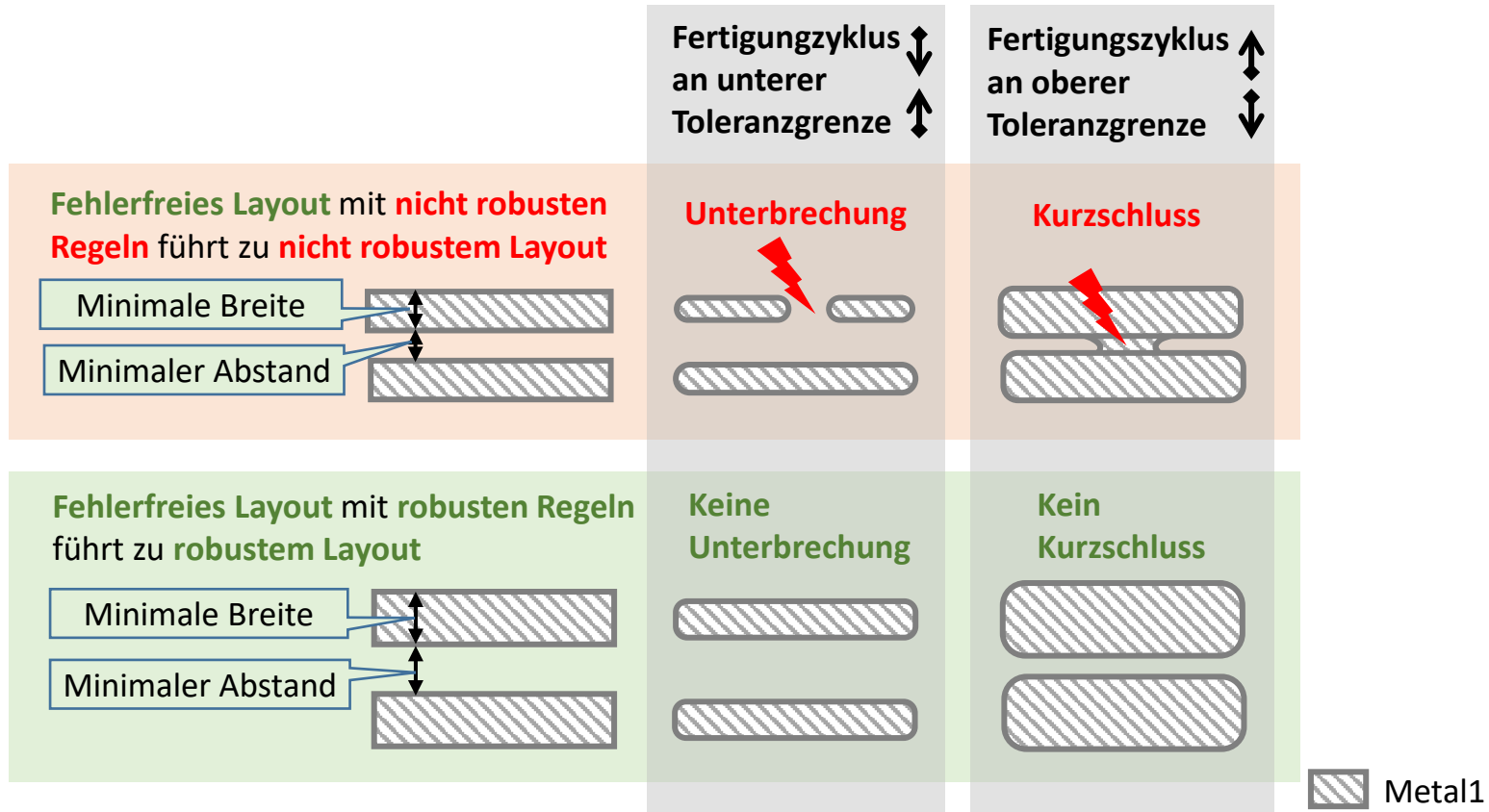
Layout-
Postprozess A

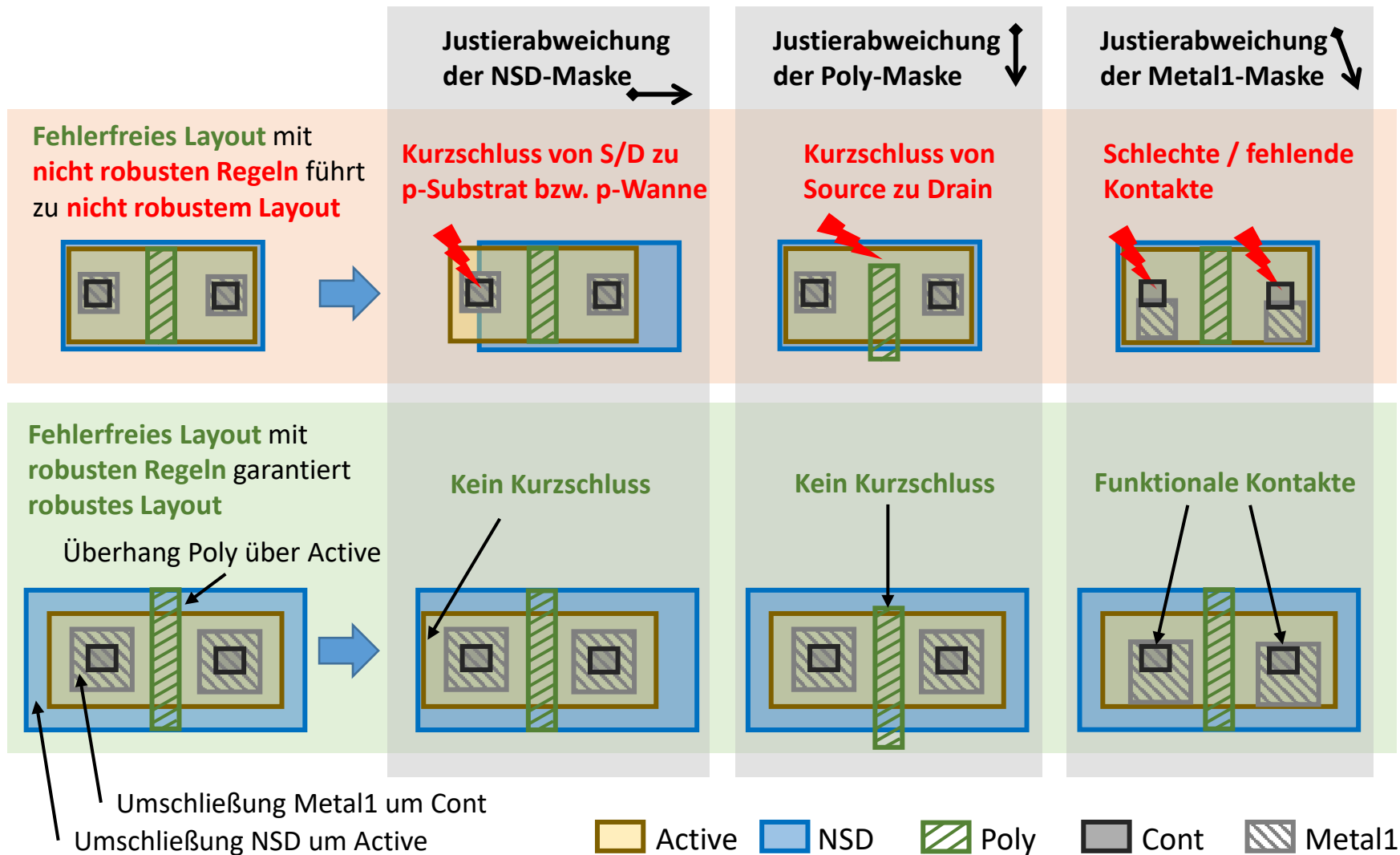
Maskendaten

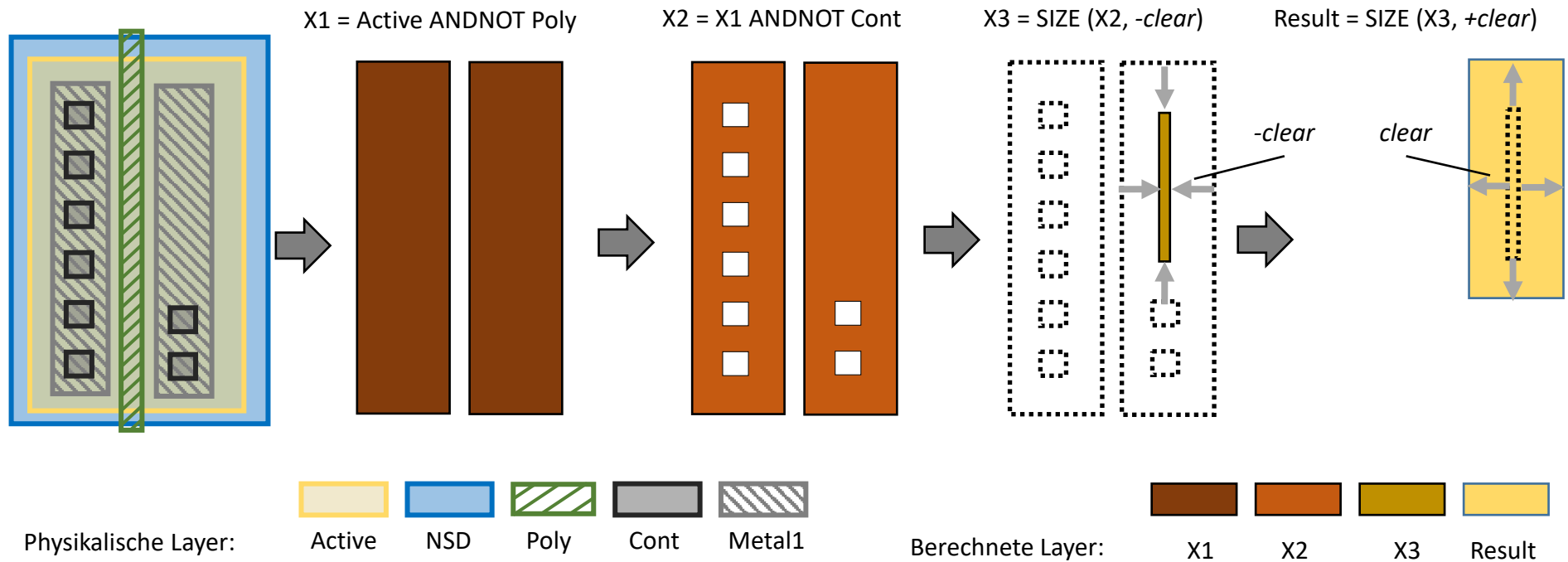


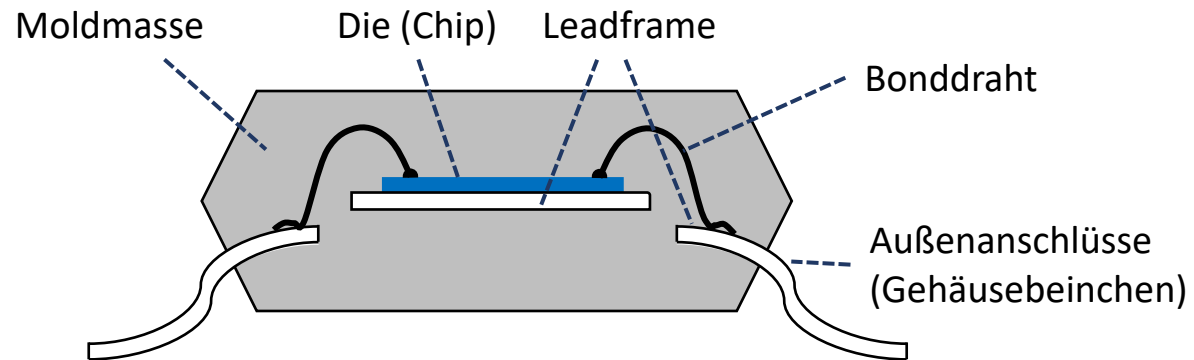


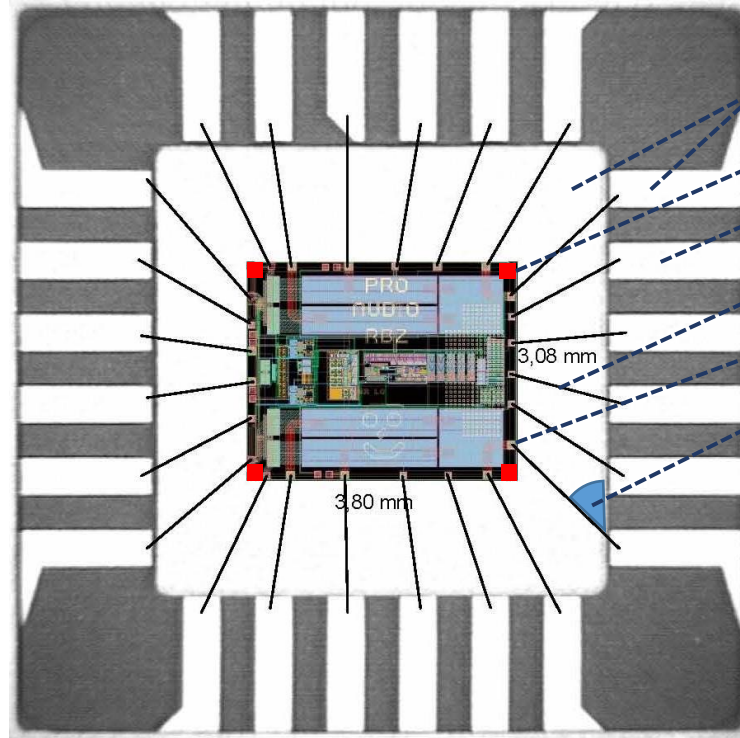












- Leadframe
- Verbotene Zone für Bondpads
- Kontaktstelle auf Leadframe
- Bonddraht
- Bondpad
- Bonddraht-Winkel

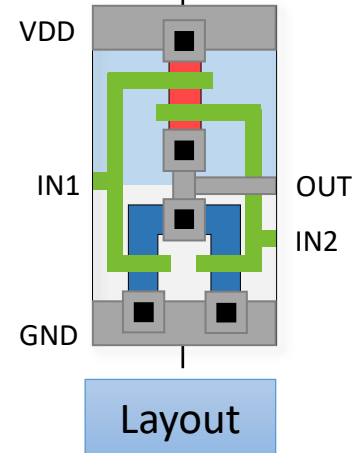
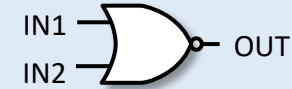
Verhaltensmodell

```
entity NOR2 is  
  port(IN1: in std_logic;  
        IN2: in std_logic;  
        OUT: out std_logic)  
end entity NOR2;
```

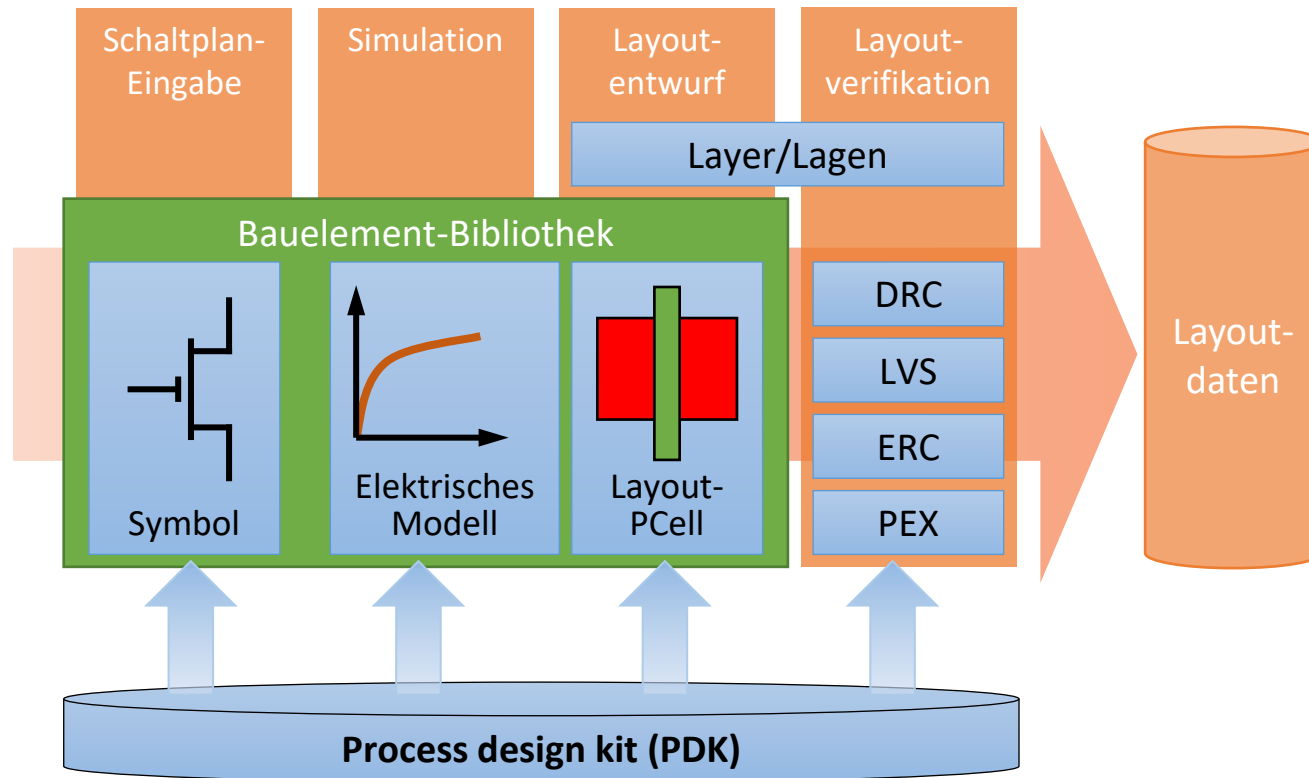
is

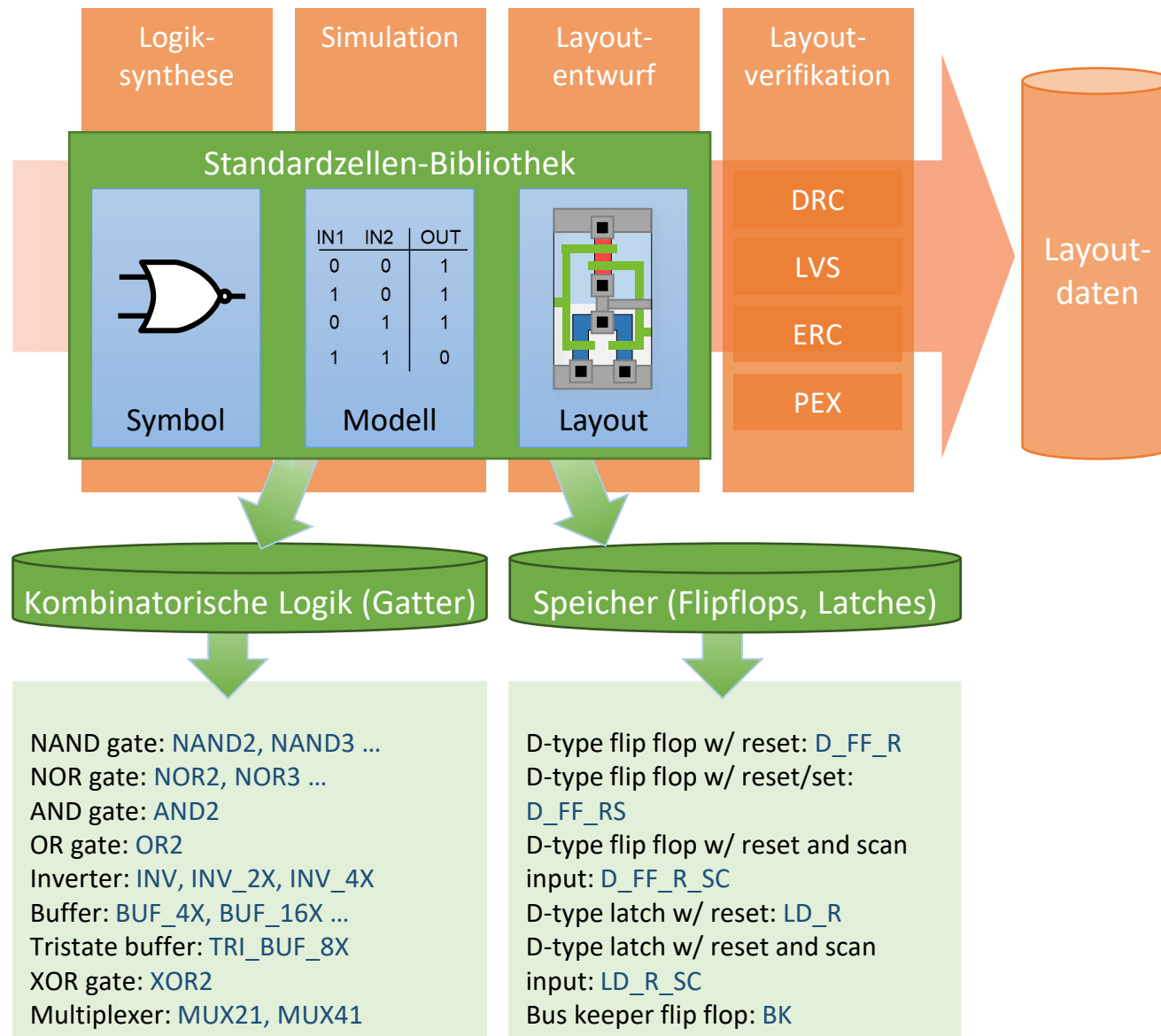
```
  OUT <= NOT(IN1 OR IN2);  
end architecture RTL;
```

Symbol



Layout





Schematic Library

Example.slib

Component	Description
JFET-N	N-Channel JFET
JFET-P	P-Channel JFET
SMD-R	SMD Resistor

Place Add Delete Edit

Pins	Name	Type	SOT23
→S	1	Passive	S
→G	2	Passive	G
→D	3	Passive	D

Add Delete Edit

Model	Type	Description
SOT23	Footprint	3 Leads; Body 3.0 x 2.6

Add Delete Edit

The diagram shows an N-Channel JFET symbol on a grid. The symbol consists of a vertical line with a horizontal line crossing it. The top terminal is labeled 'D', the middle terminal is labeled 'G', and the bottom terminal is labeled 'S'. Red arrows point from the labels to the corresponding pins.

Name der Symbol-Bibliothek

Symbole in dieser Bibliothek

Selektiertes Symbol

Symbol-Editor

Pinnamen, Pinzuordnung

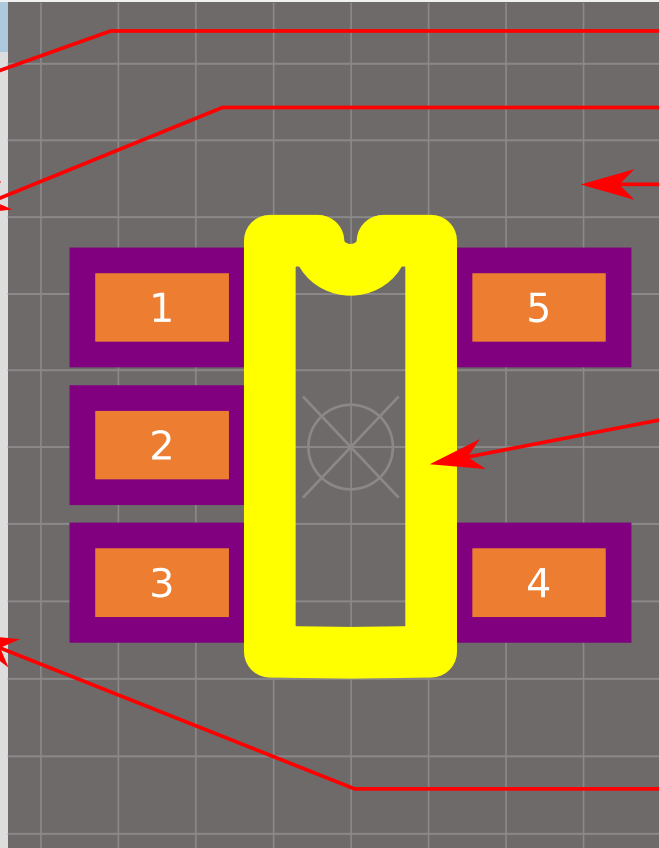
Referenz zum Footprint

Footprint Library

Example.fplib

Components		
Name	Pads	Primitives
 SOIC-8 (RN-8)	8	15
 SOT23-5 (RJ-5)	5	12
 SSOP16 (GN)	16	24

Component Primitives				
Type	Name	X-Size	Y-Size	Layer
ARC		0.2mm		TopOverlay
Track		0.2mm		TopOverlay
Track		0.2mm		TopOverlay
Pad	1	1mm	0.5mm	Top Layer
Pad	2	1mm	0.5mm	Top Layer
Pad	3	1mm	0.5mm	Top Layer
Pad	4	1mm	0.5mm	Top Layer



Name der Footprint-Bibliothek

Footprints in dieser Bibliothek

Footprint-Editor

Selektierter Footprint

Grafikelemente des Footprints

The screenshot shows a 'Model Library' window with a text area containing the following text:

```
*****  
* Copyright (c) 2000-2012 Linear Technology Corporation. *  
* All rights reserved. *  
*****  
  
.model 1N4001 D  
+Is=14.11n N=1.984 Rs=33.89m Ikf=94.81  
+Xti=3 Eg=1.11 Cjo=25.89p M=.44  
+Vj=.3245 Fc=.5 Bv=75 Ibv=10u Tt=5.7u  
+Iave=1 Vpk=50 mfg=GI type=silicon
```

Red arrows point from the following labels to the text in the window:

- Modellname** points to `1N4001`.
- Modellkategorie (Diode)** points to `D`.
- Bauelementspezifischer Parametersatz** points to the parameter list starting with `+Is=14.11n`.