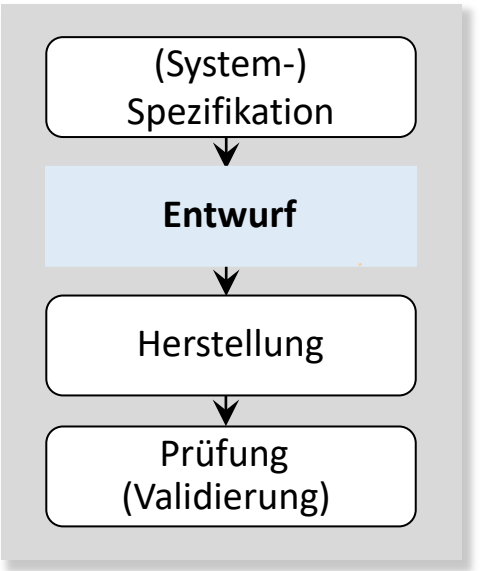
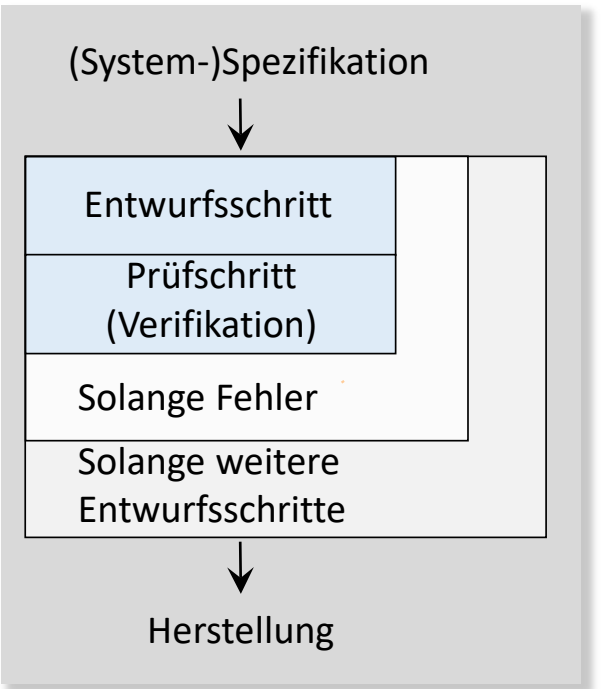
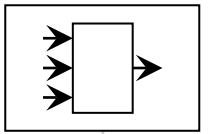
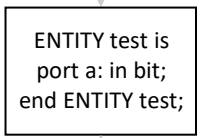
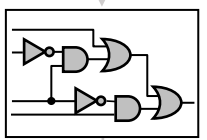
Kapitel 4 - Layoutentwurf im Überblick: Modelle, Stile, Aufgaben und Abläufe

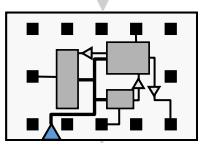


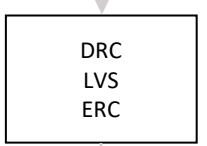


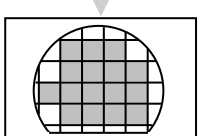


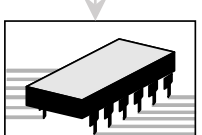












System-spezifikation

Architektur-entwurf

Verhaltens- und logischer Entwurf

Schaltungs-entwurf

Layoutentwurf

Layoutverifikation

Layout-Postprozess

Herstellung

Verpackung und Prüfung

Partitionierung

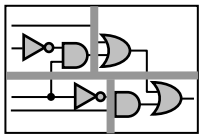
Floorplanning

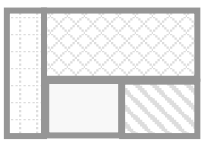
Platzierung

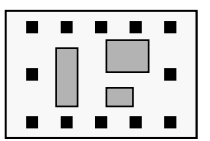
Clock-Tree-Synthese

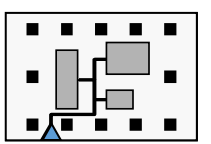
Signalverdrahtung

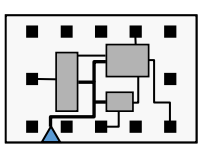
Timing Closure

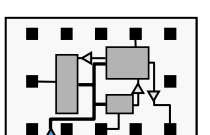


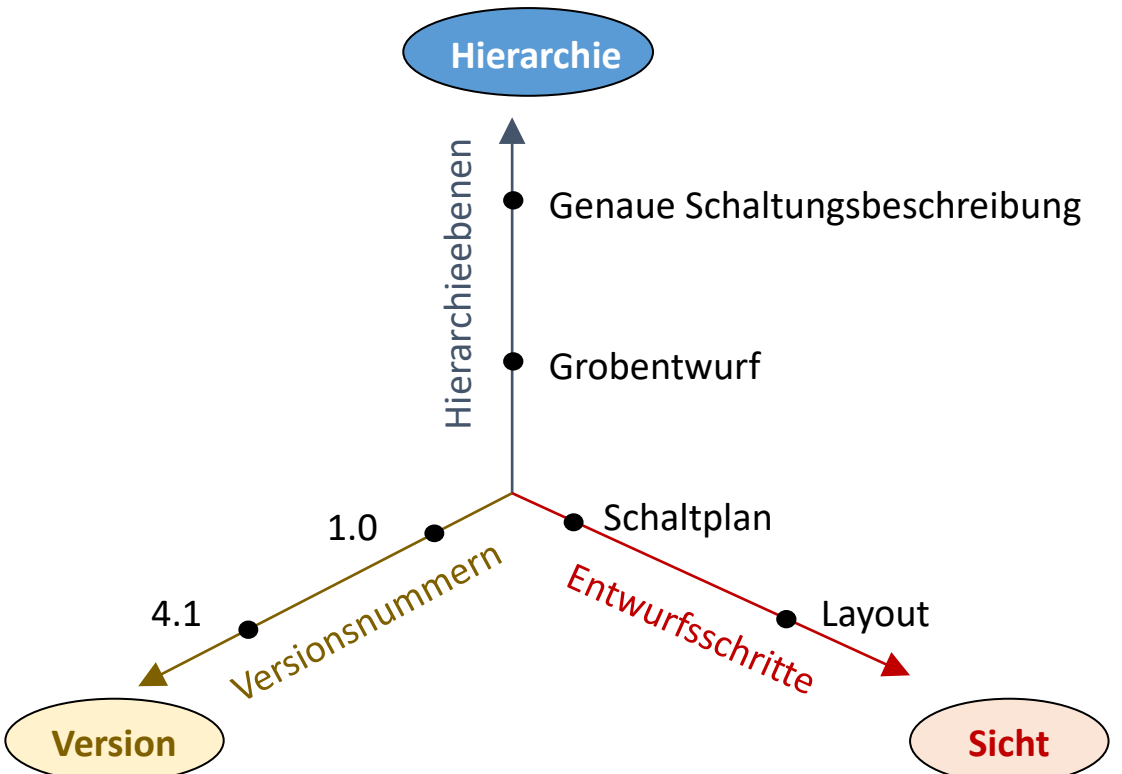


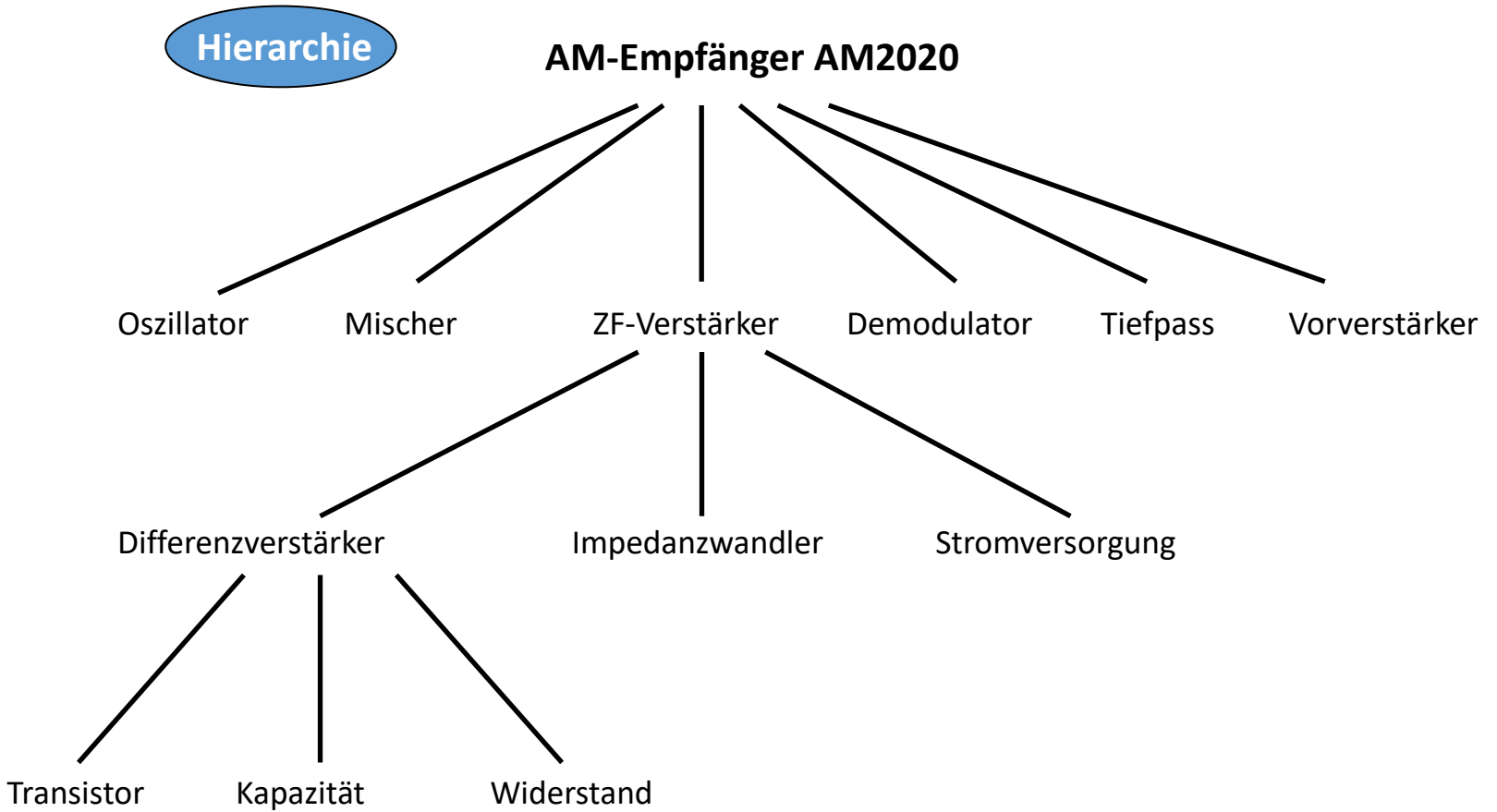


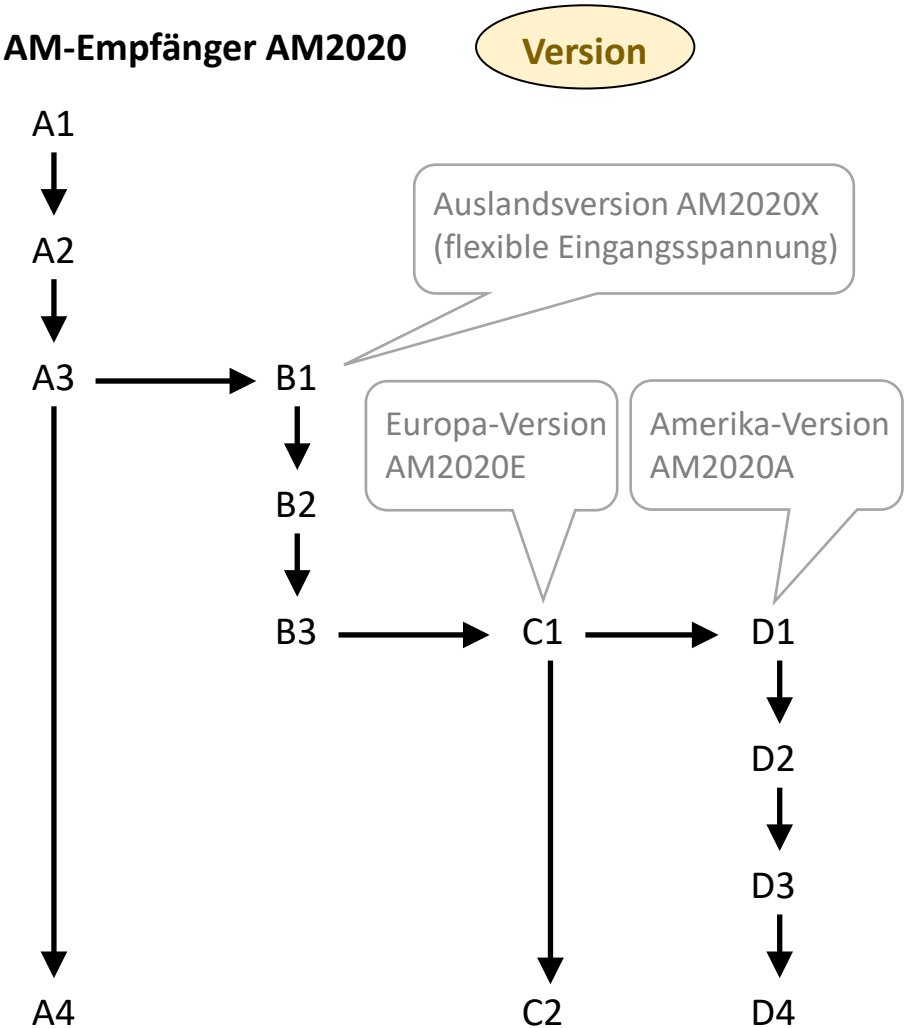


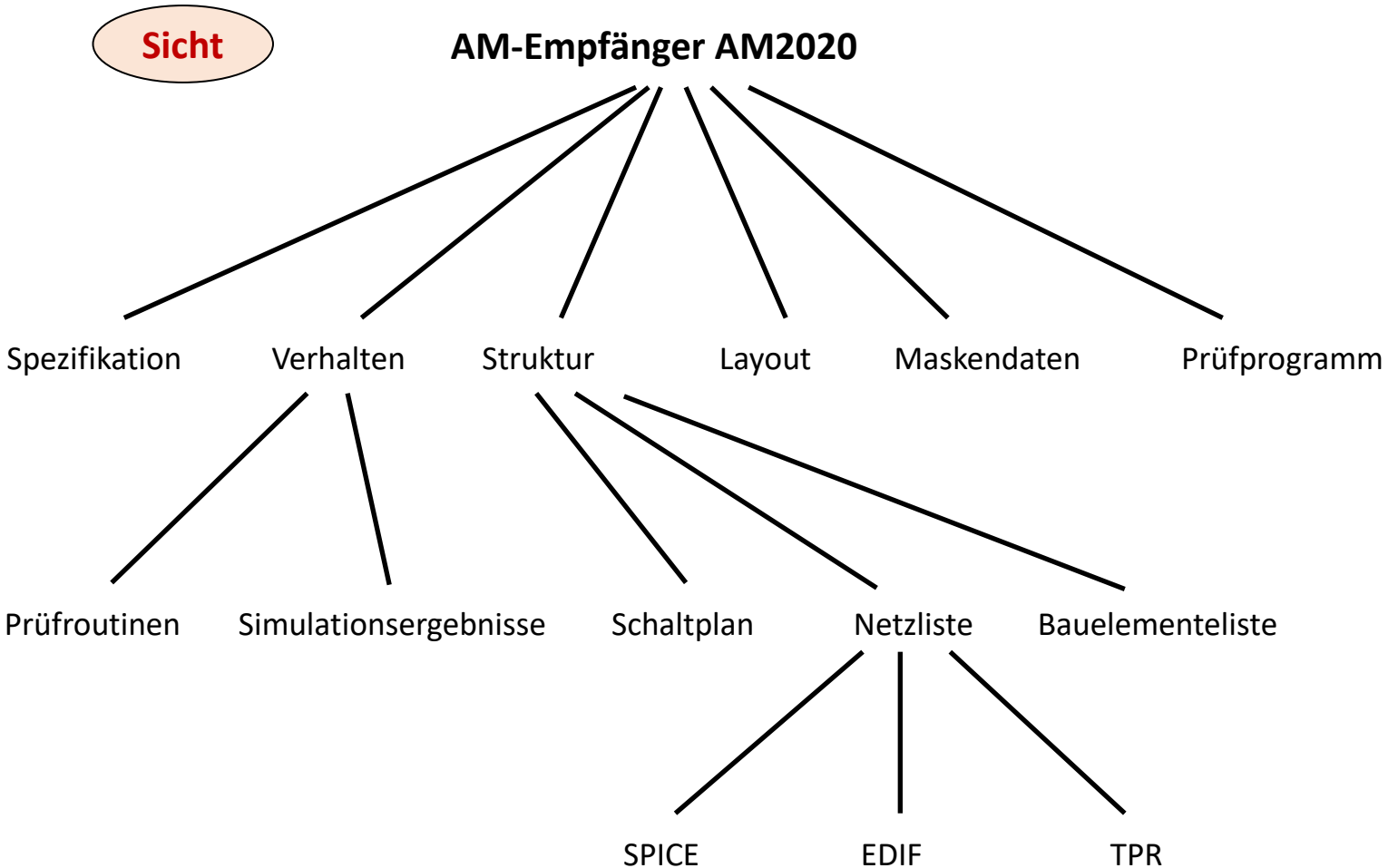


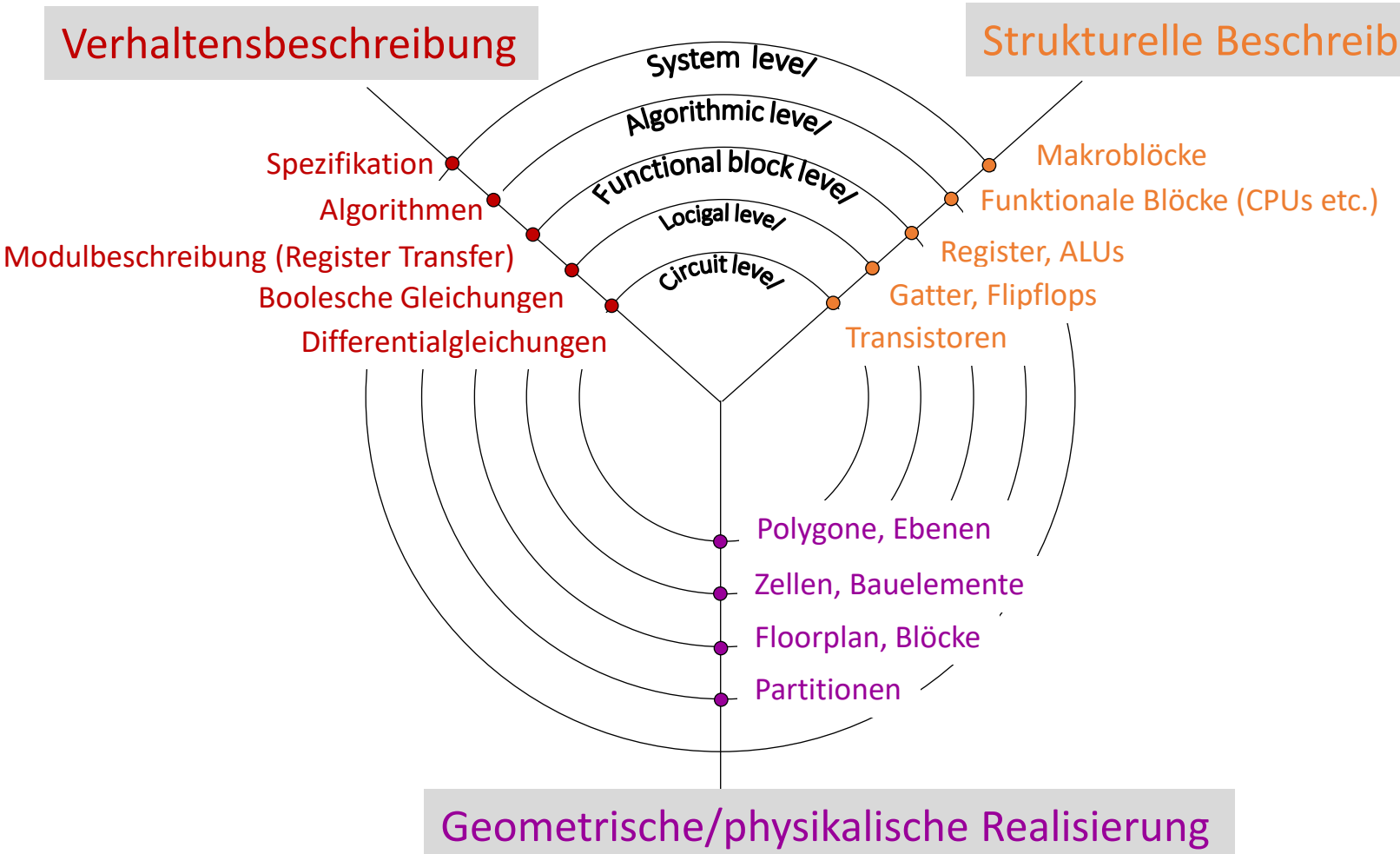








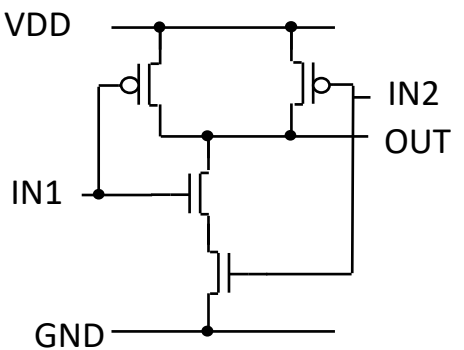




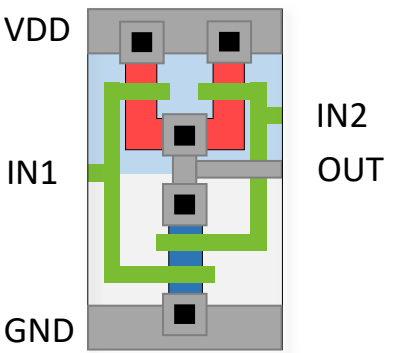
Verhaltens-beschreibung

IN1	IN2	OUT
0	0	1
0	1	1
1	0	1
1	1	0

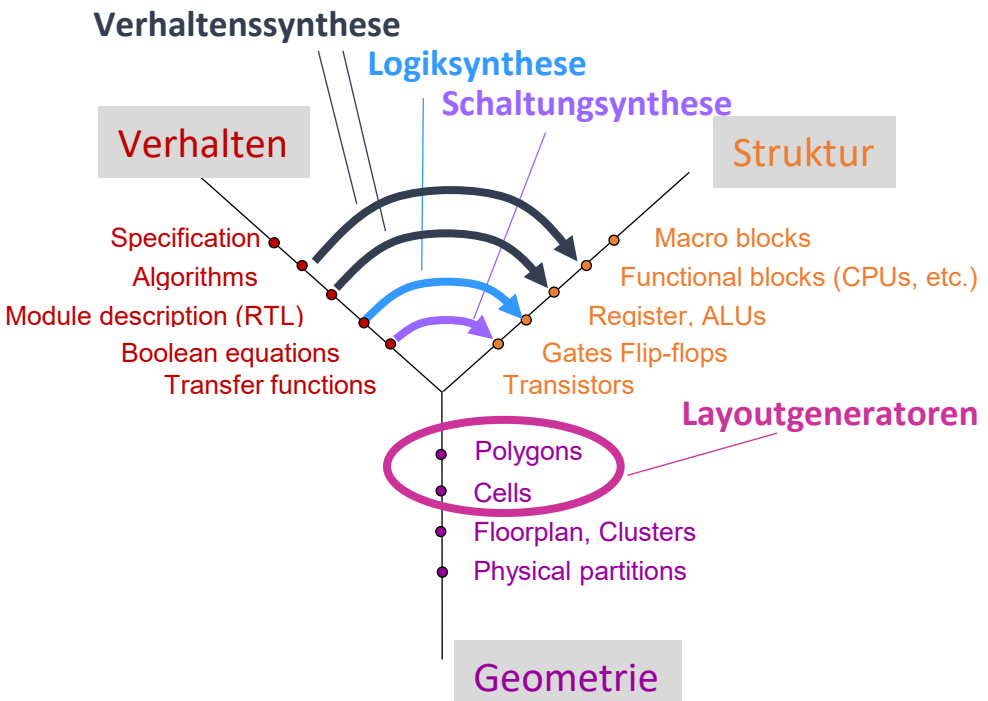
Strukturelle Beschreibung

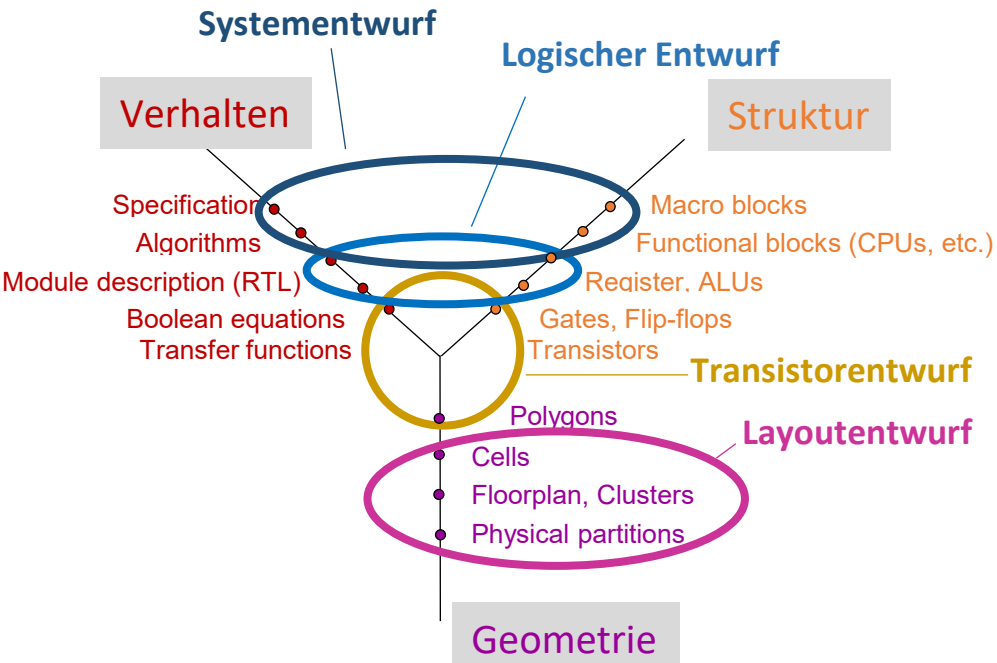


Geometrische/physikalische Realisierung

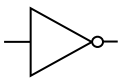


NAND gate 





INV

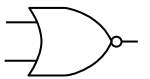


IN	OUT
0	1
1	0

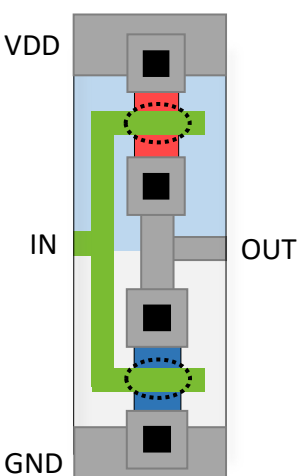
NAND

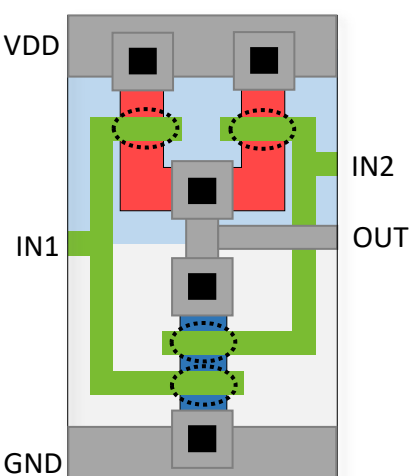
IN1	IN2	OUT
0	0	1
1	0	1
0	1	1
1	1	0

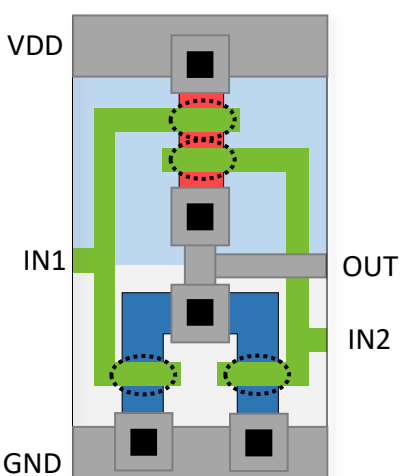
NOR

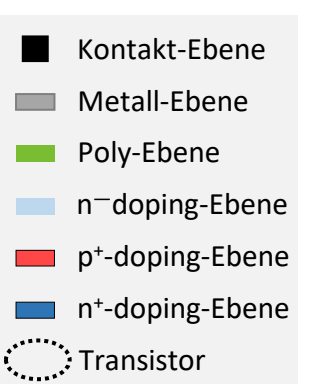


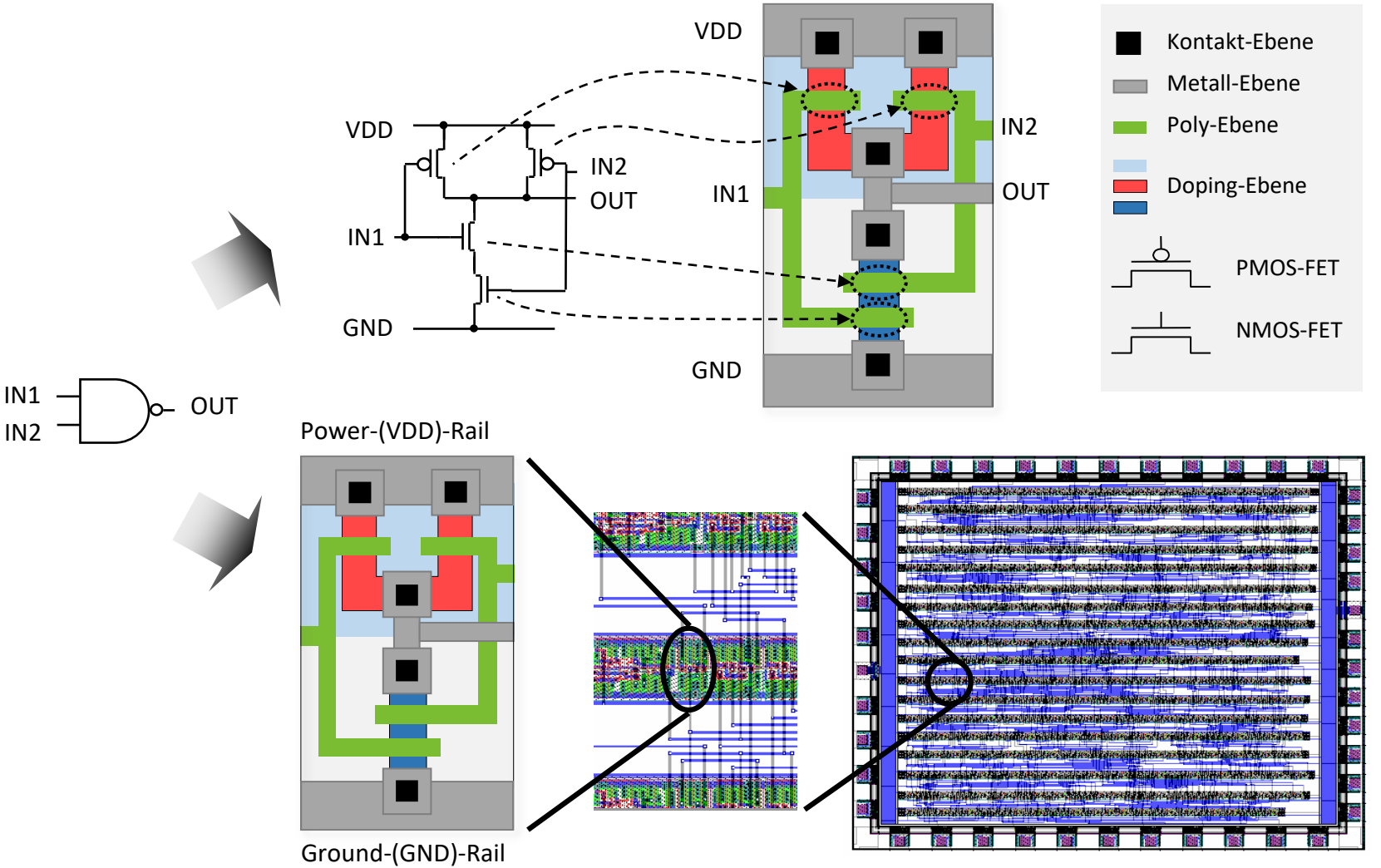
IN1	IN2	OUT
0	0	1
1	0	0
0	1	0
1	1	0

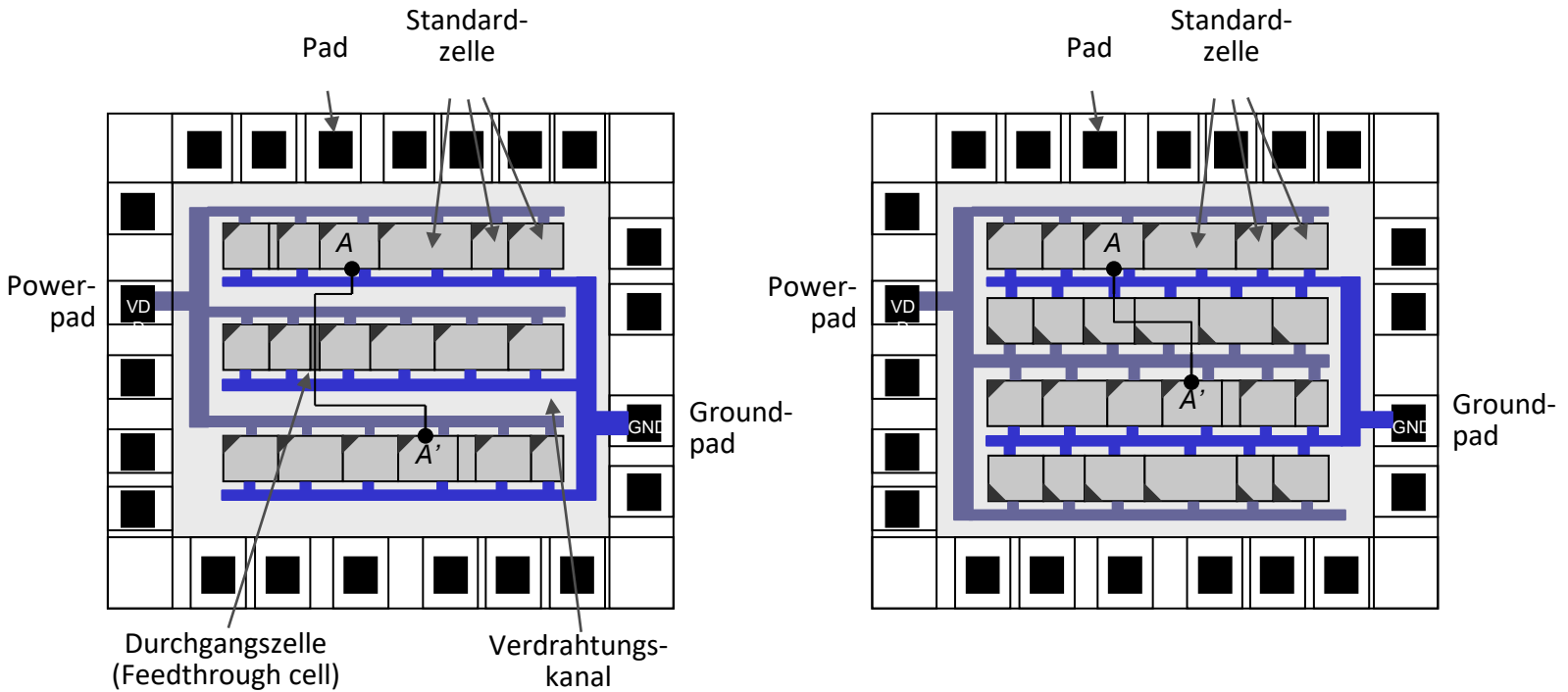


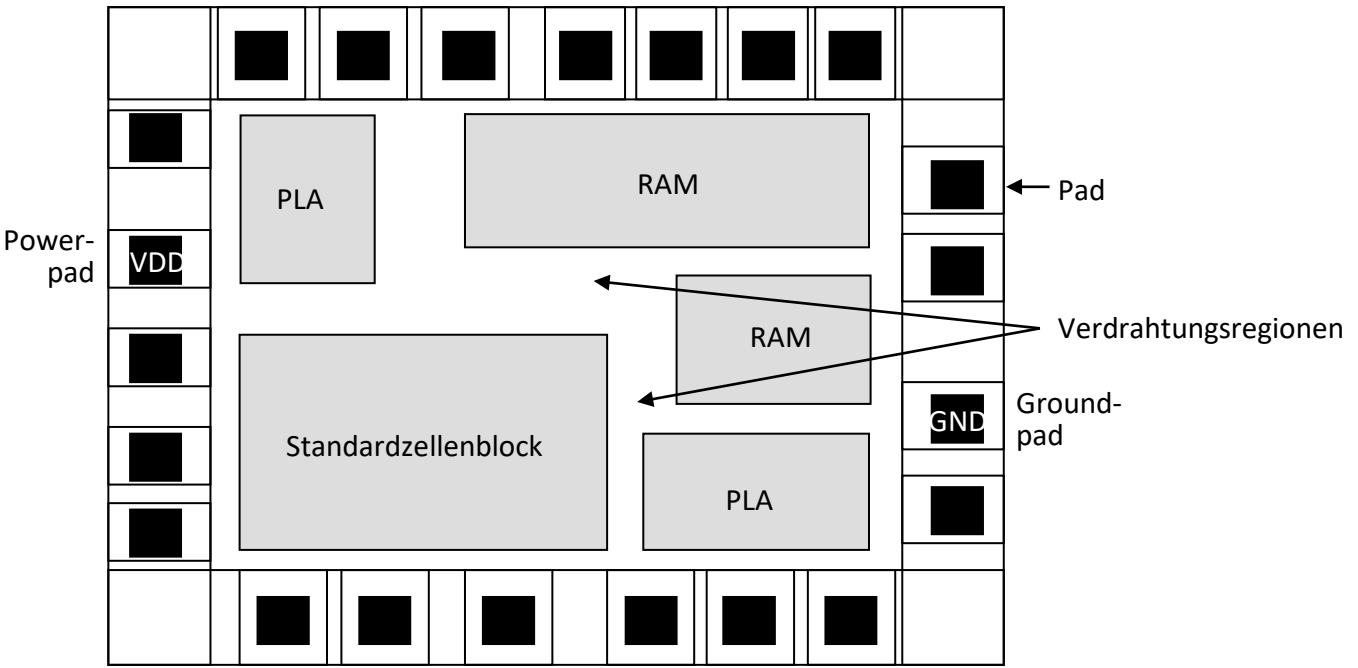


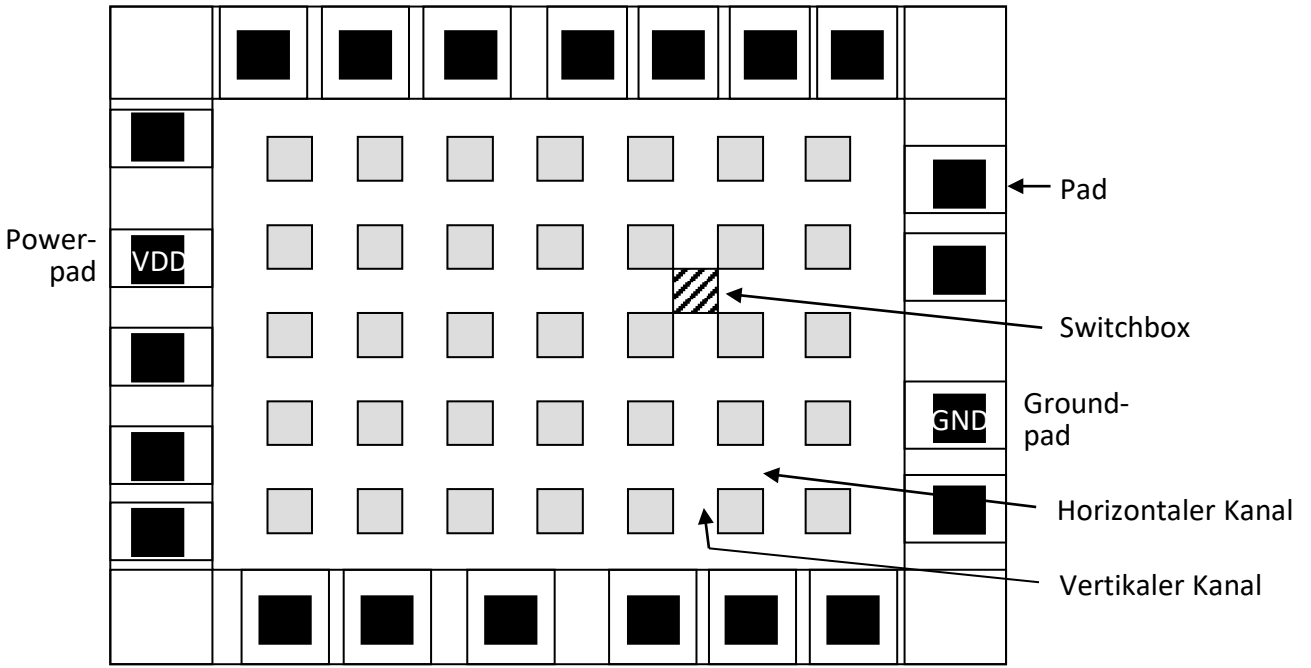


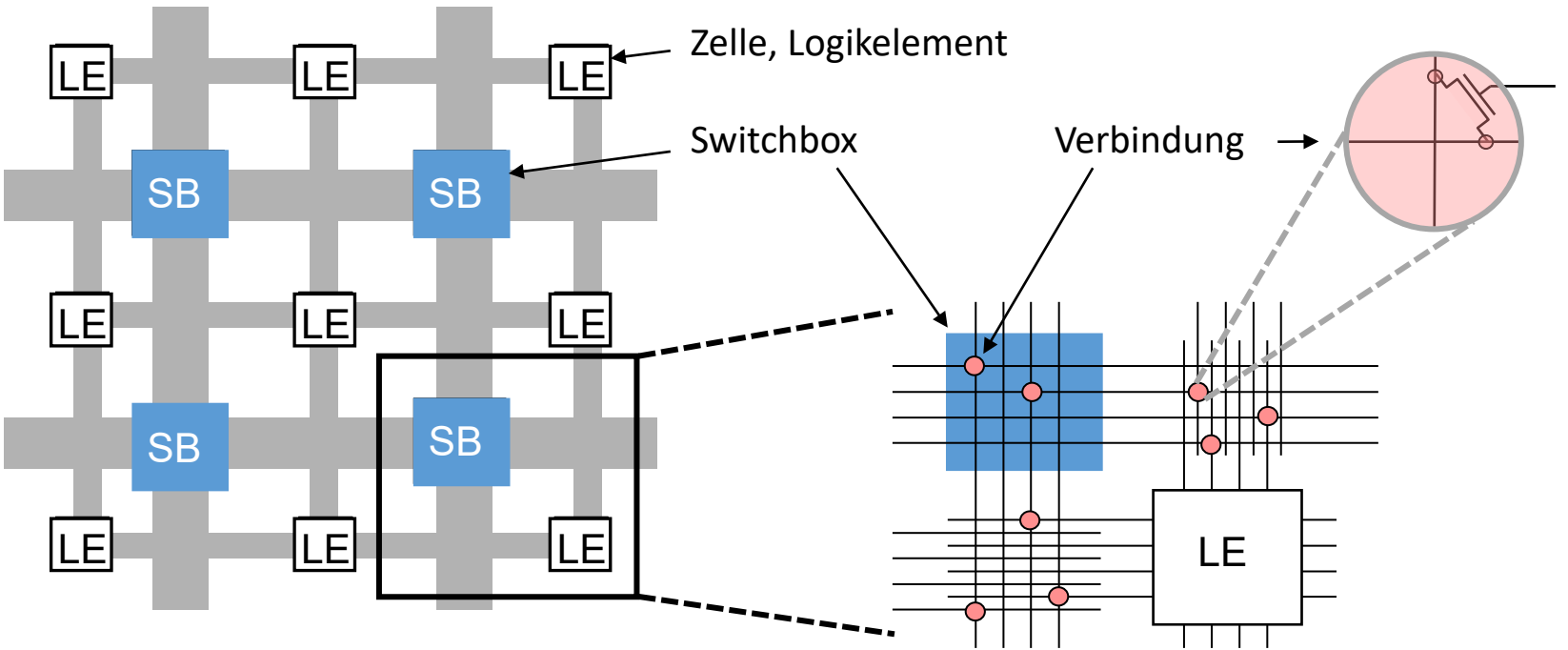




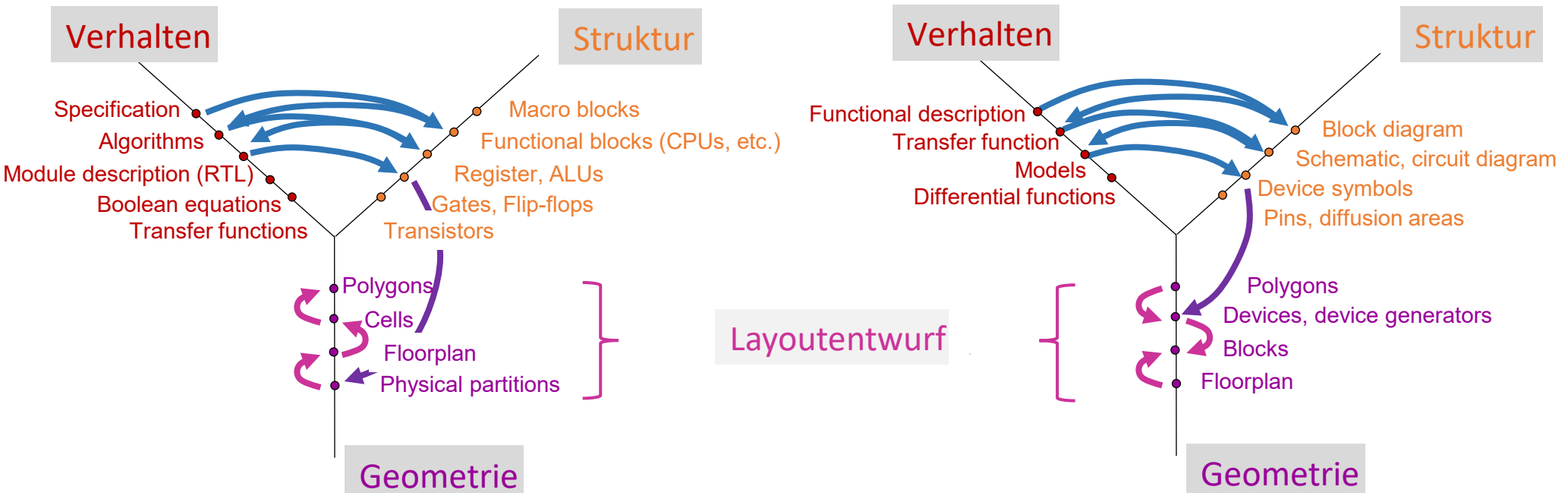


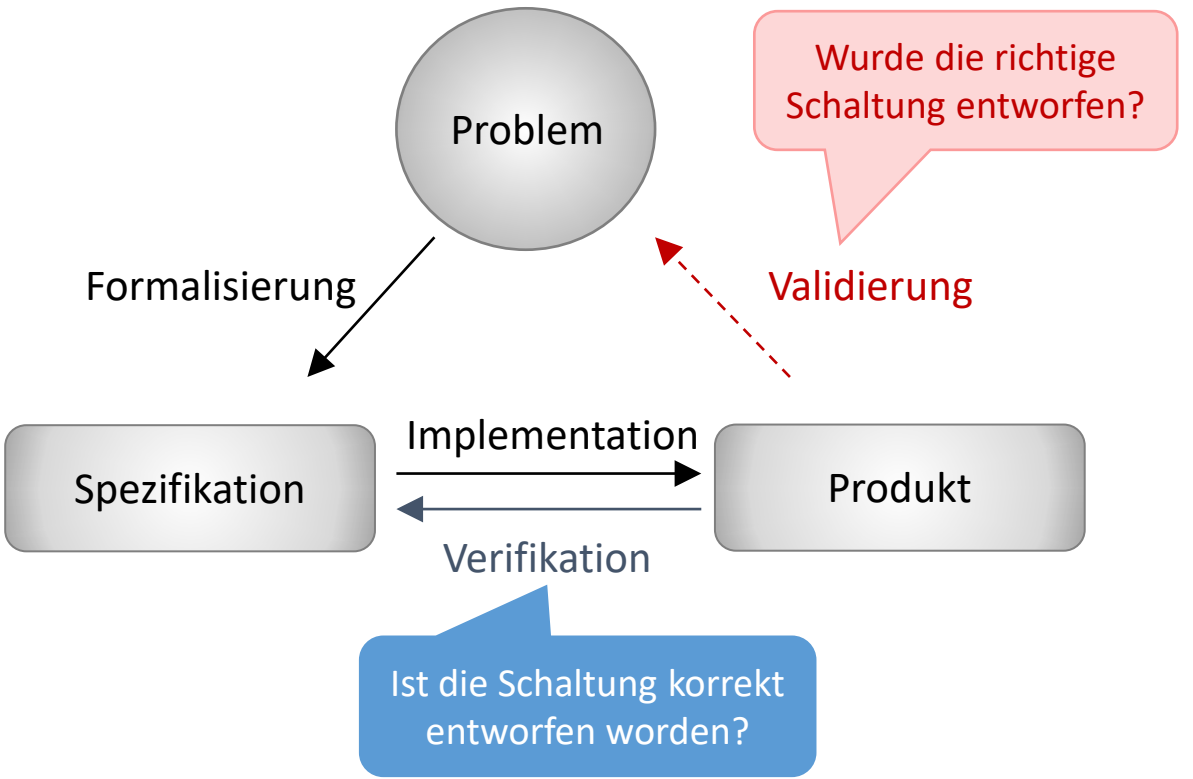


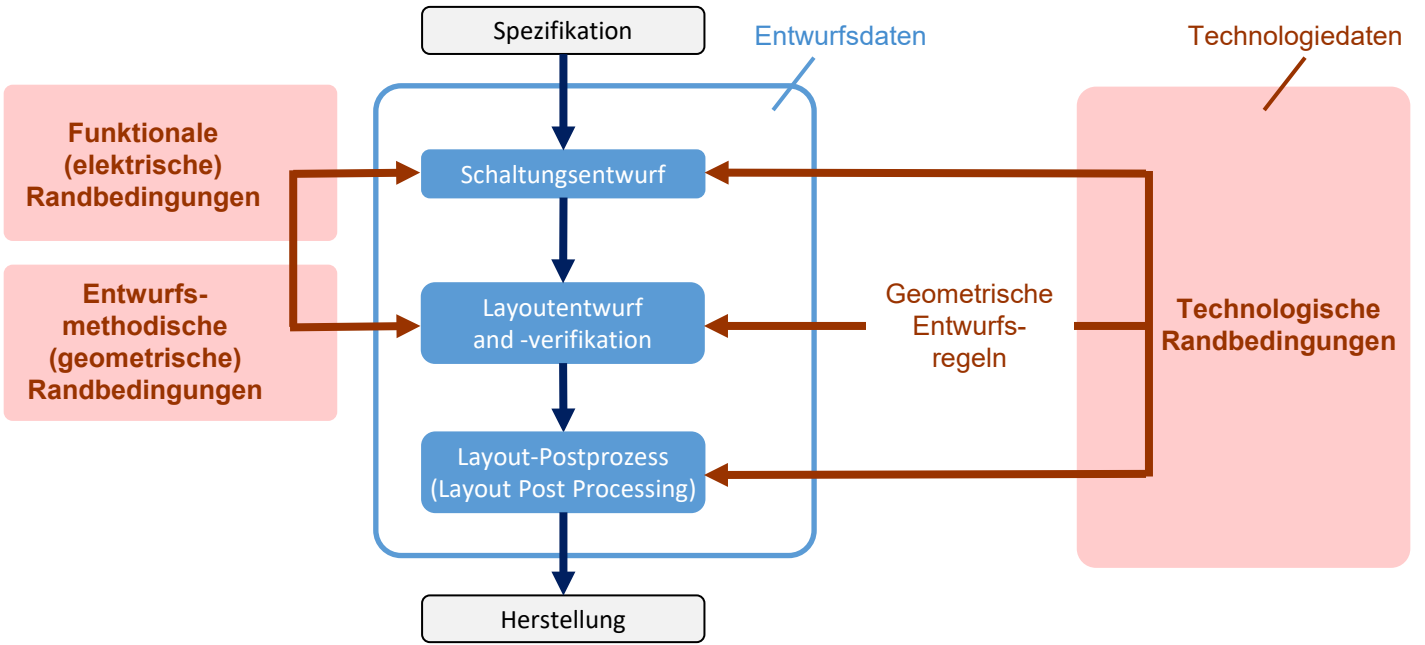


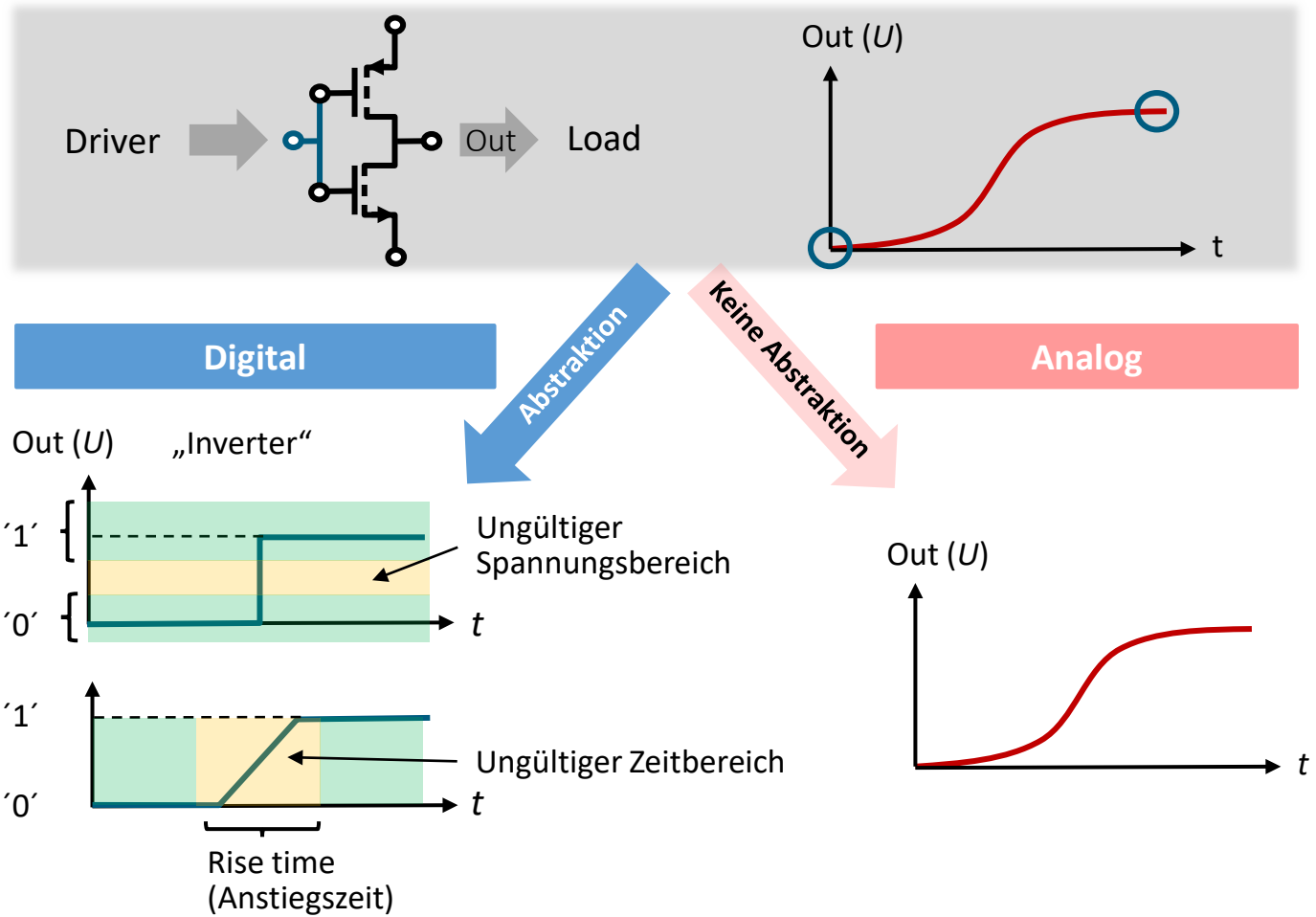


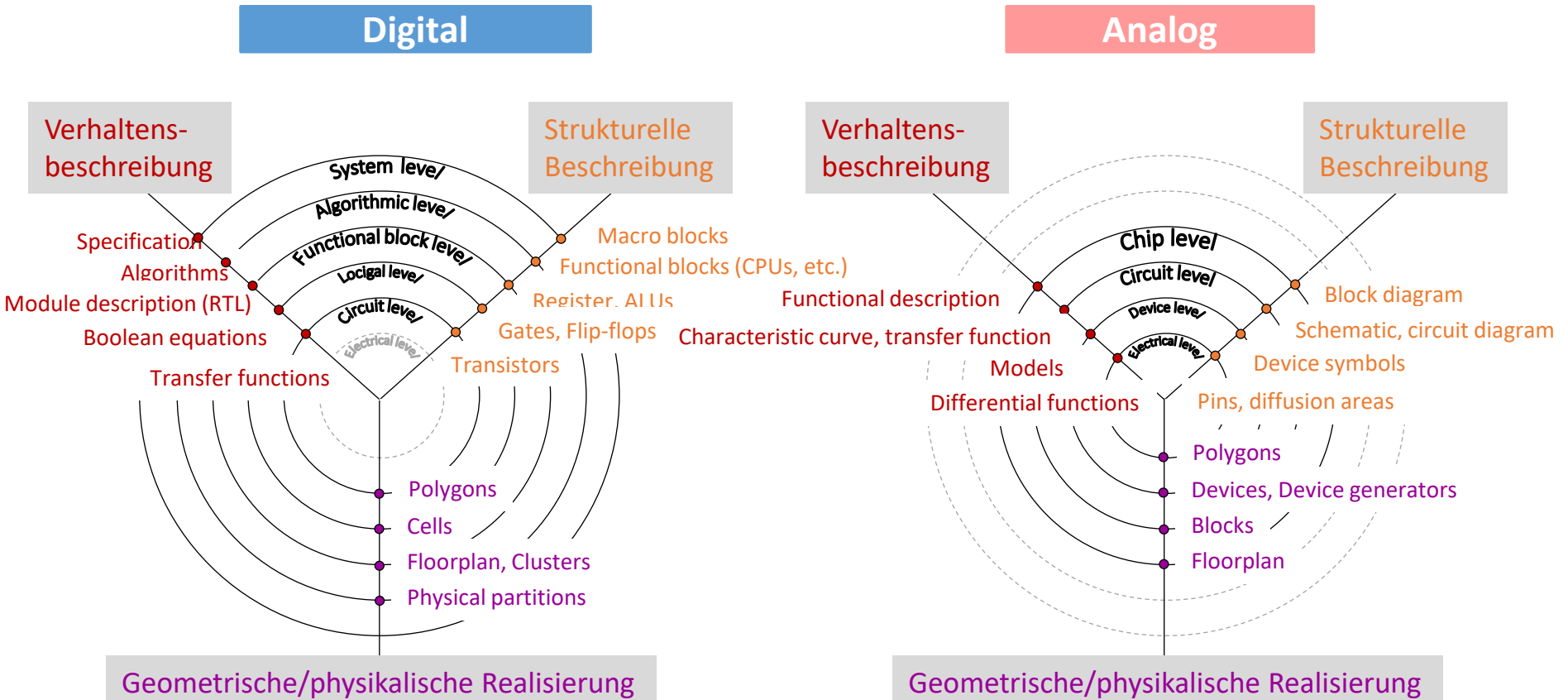
Entwurfsstil	Entwurfskosten	Kosten der Maske	Fertigungs-kosten	Leistung	Wirtschaftliches Volumen
Kunden-spezifisch	Hoch	Hoch	Low	Hoch	Hoch
Standardzelle	Niedrig	Hoch	Mittel	Mittel	Mittlerer Bereich
Makrozelle	Hoch (Niedrig bei Wiederverwendung)	Hoch	Niedrig	Hoch	Mittlerer Bereich
Gate-Array	Niedrig	Mittel	Hoch	Niedrig	Niedrig
FPGA	Sehr niedrig	Keine	Hoch	Niedrig	Niedrig

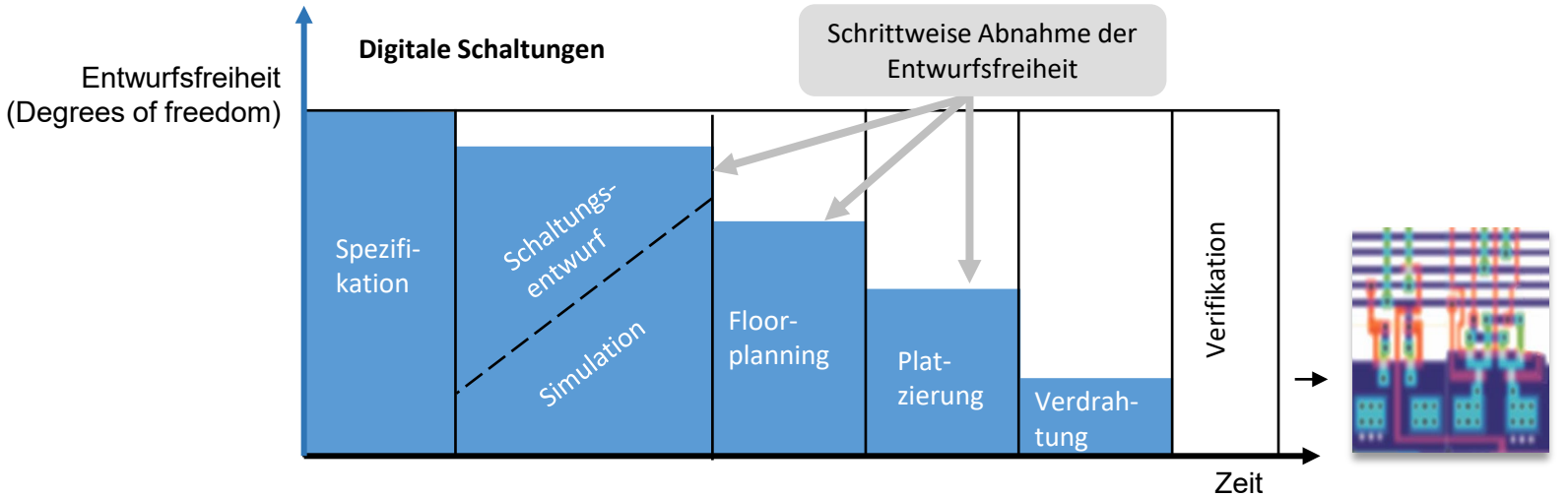


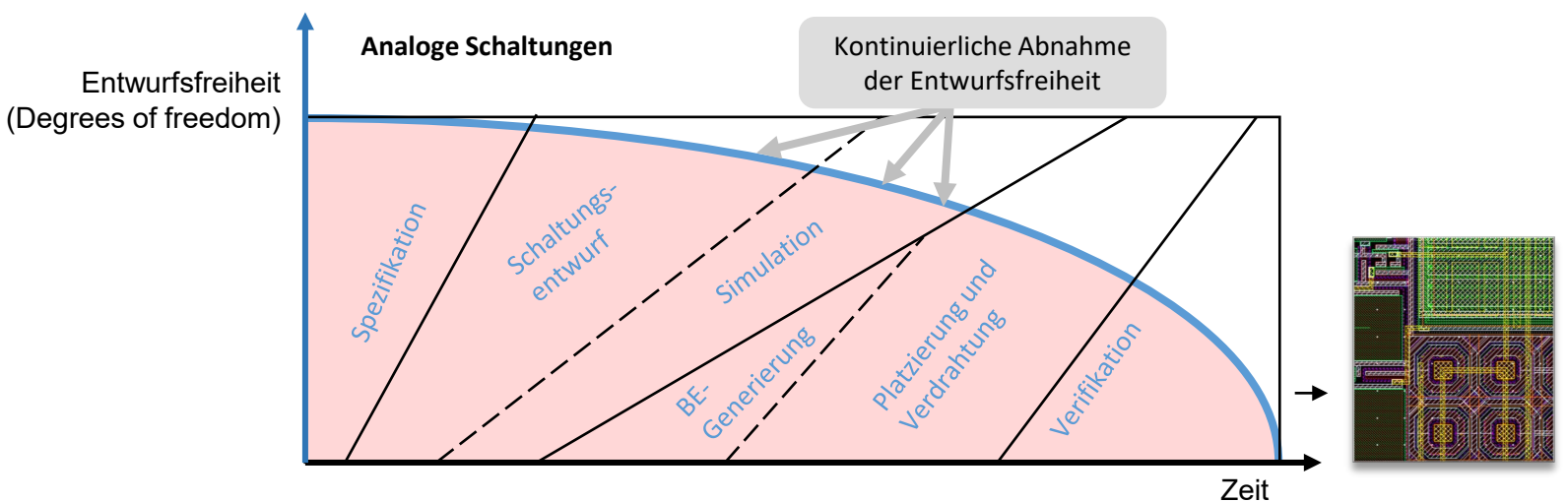


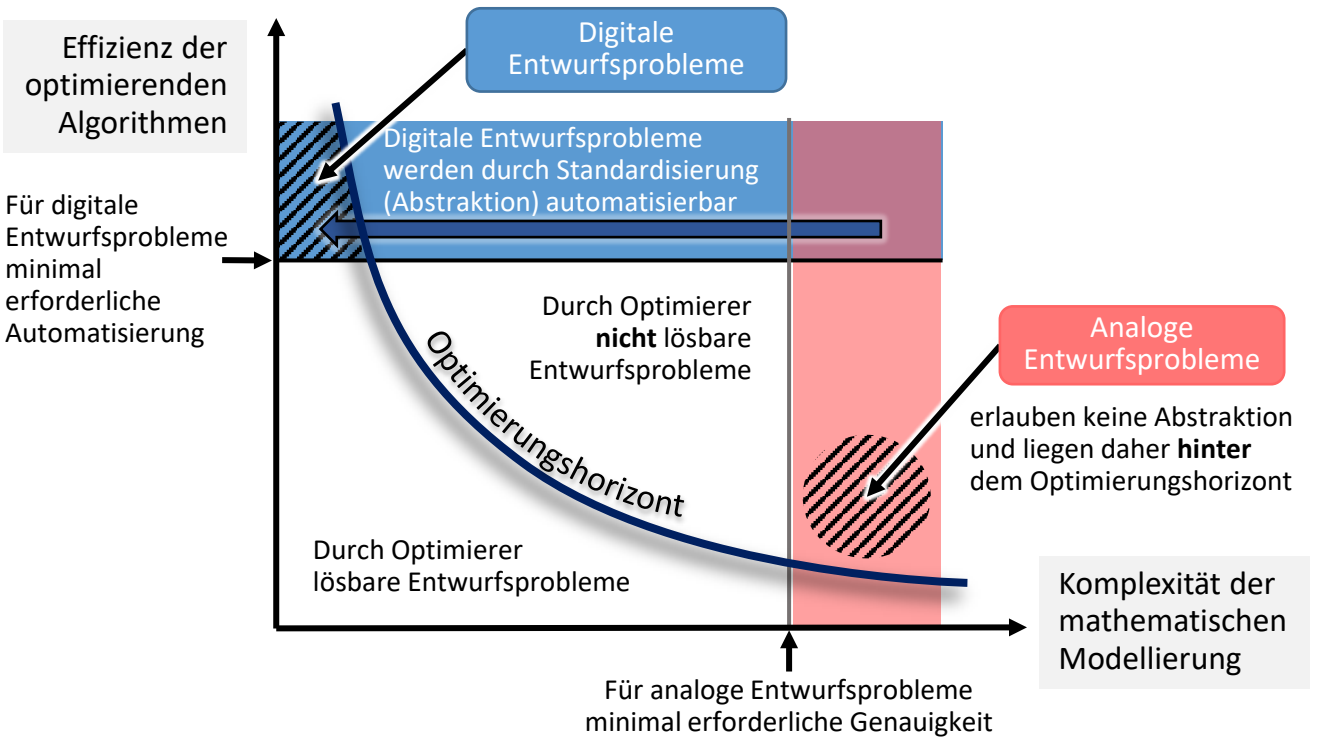




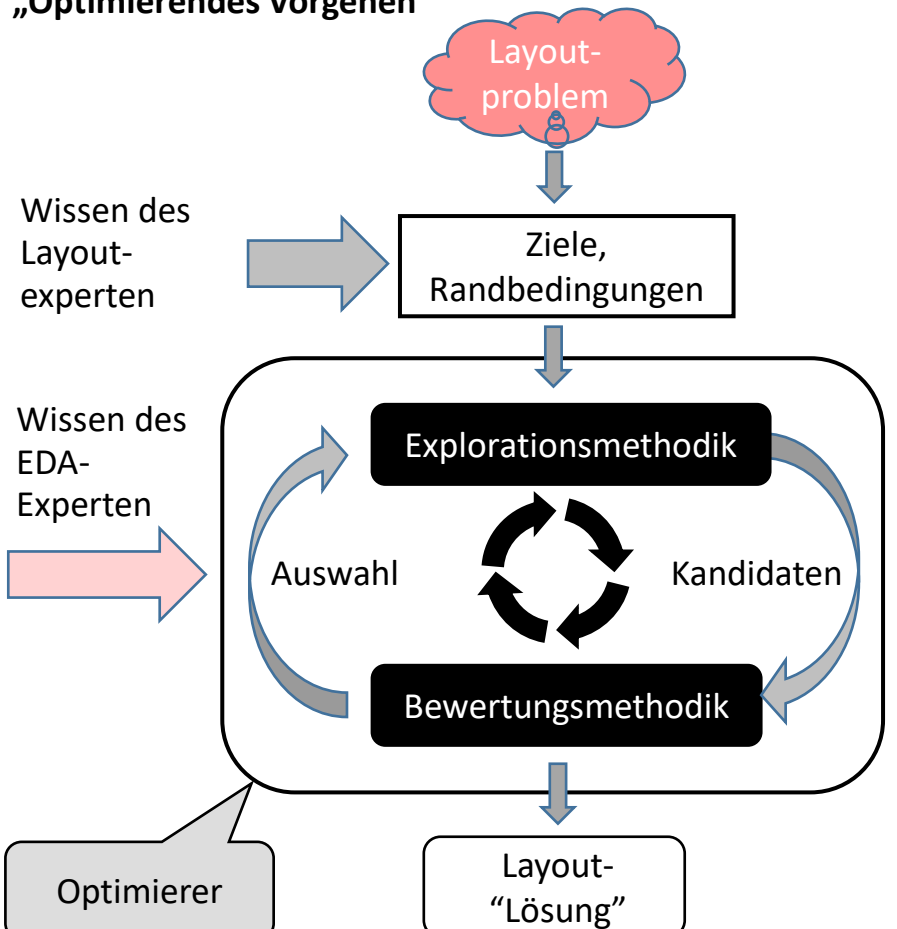




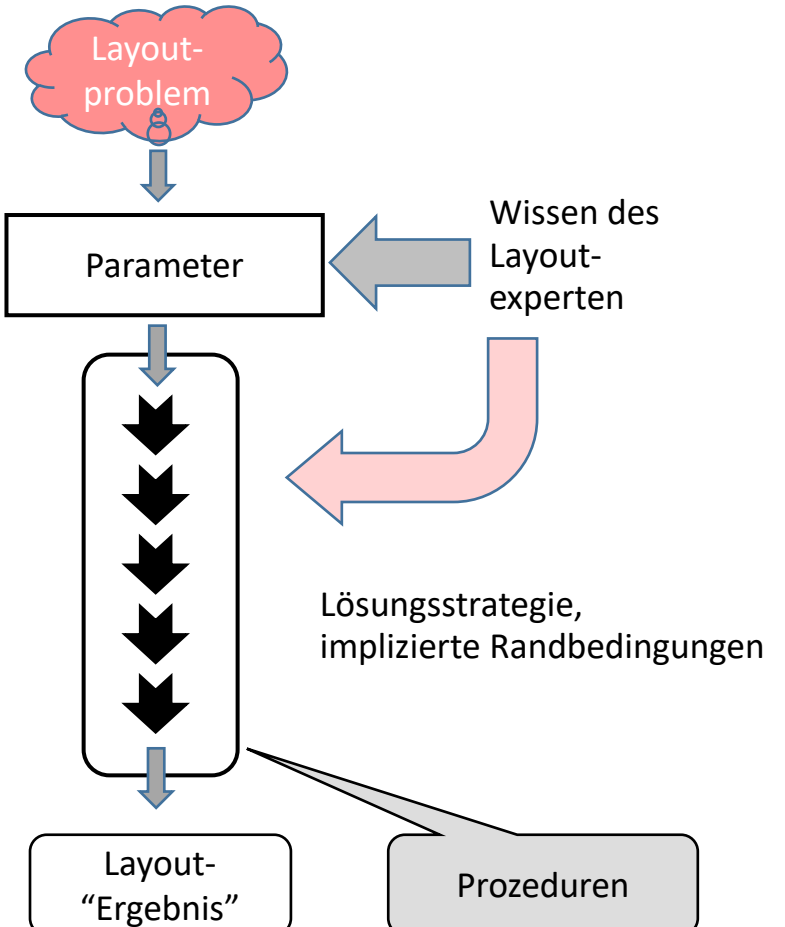




Top-down-Entwurfsstil
„Optimierendes Vorgehen“

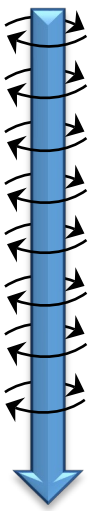


Bottom-up-Entwurfsstil „Prozedurales Vorgehen“



Synthese-Schritte

Logiksynthese
Partitionierung
Floorplanning
Power-Verdrahtung
Globale Platzierung
Detaillierte Platzierung
Clock-Tree-Synthese
Globalverdrahtung
Feinverdrahtung
Timing Closure



Analyse- bzw. Verifikations-Schritte

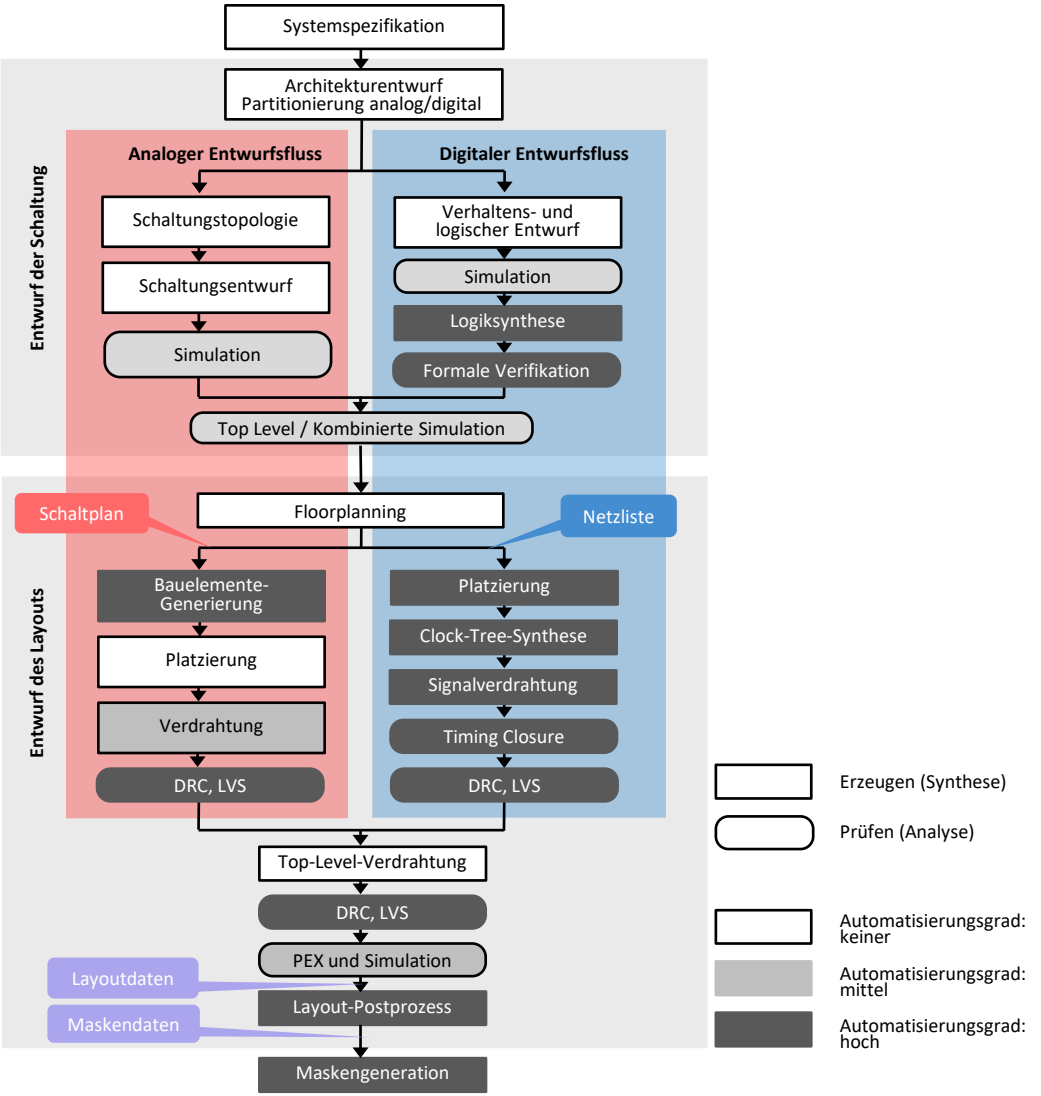
Formale Verifikation

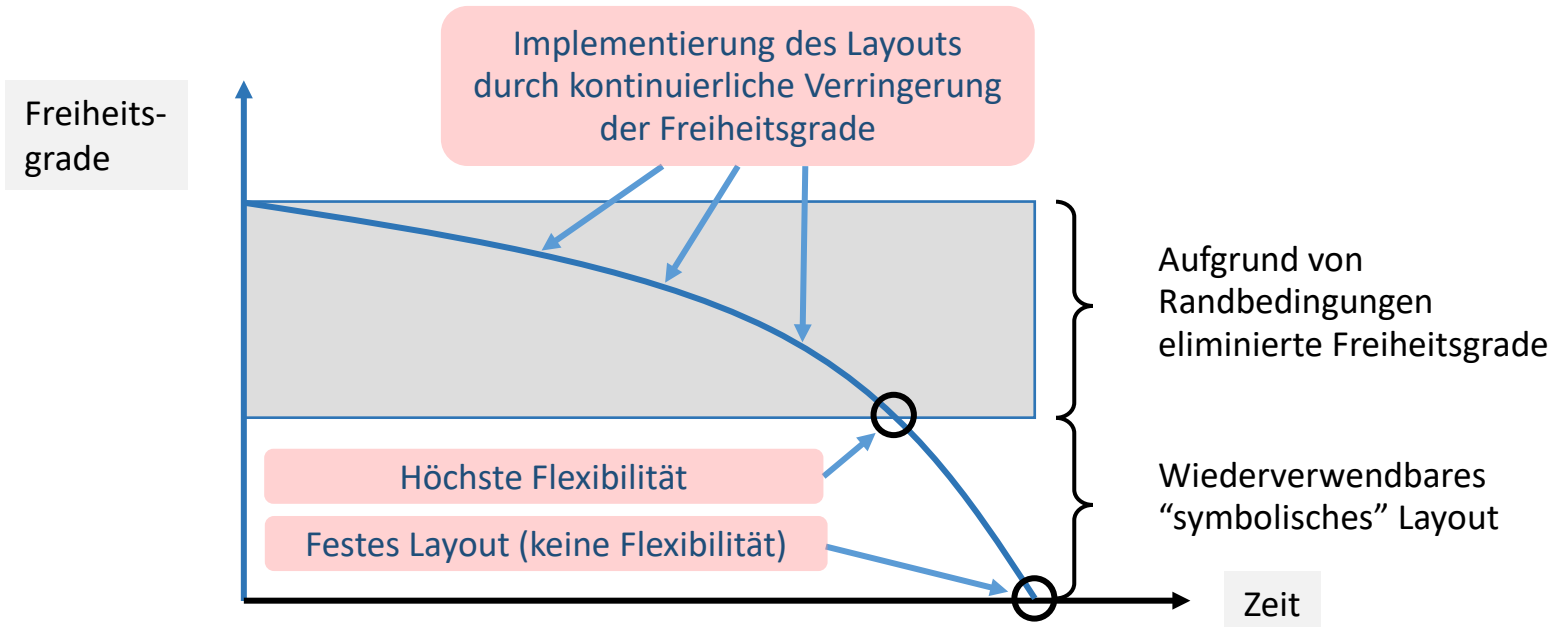
Globales Timing

Vorhersage der Verdrahtbarkeit

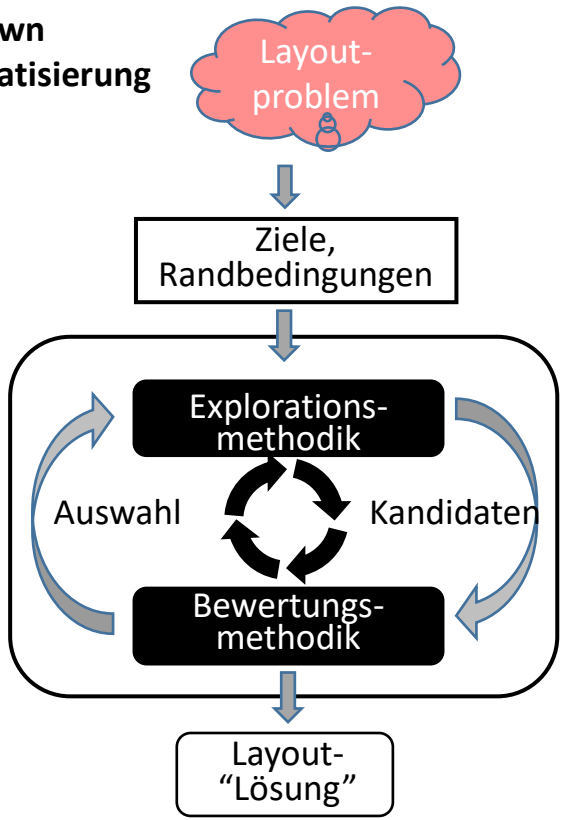
Timing

Parasitenextraktion
Sign-off DRC
Sign-off Timing
Sign-off Spice Simulation





Top-down Automatisierung



Bottom-up Automatisierung