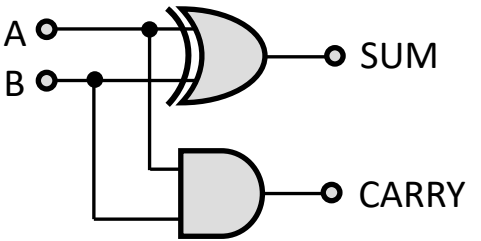
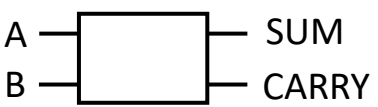
Kapitel 5 - Layoutentwurf in Schritten: Von der Netzliste bis zum Layout-Postprozess

Halbaddierer (Half adder)

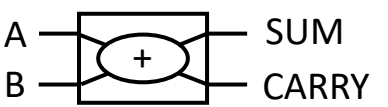


Schnittstellen-beschreibung

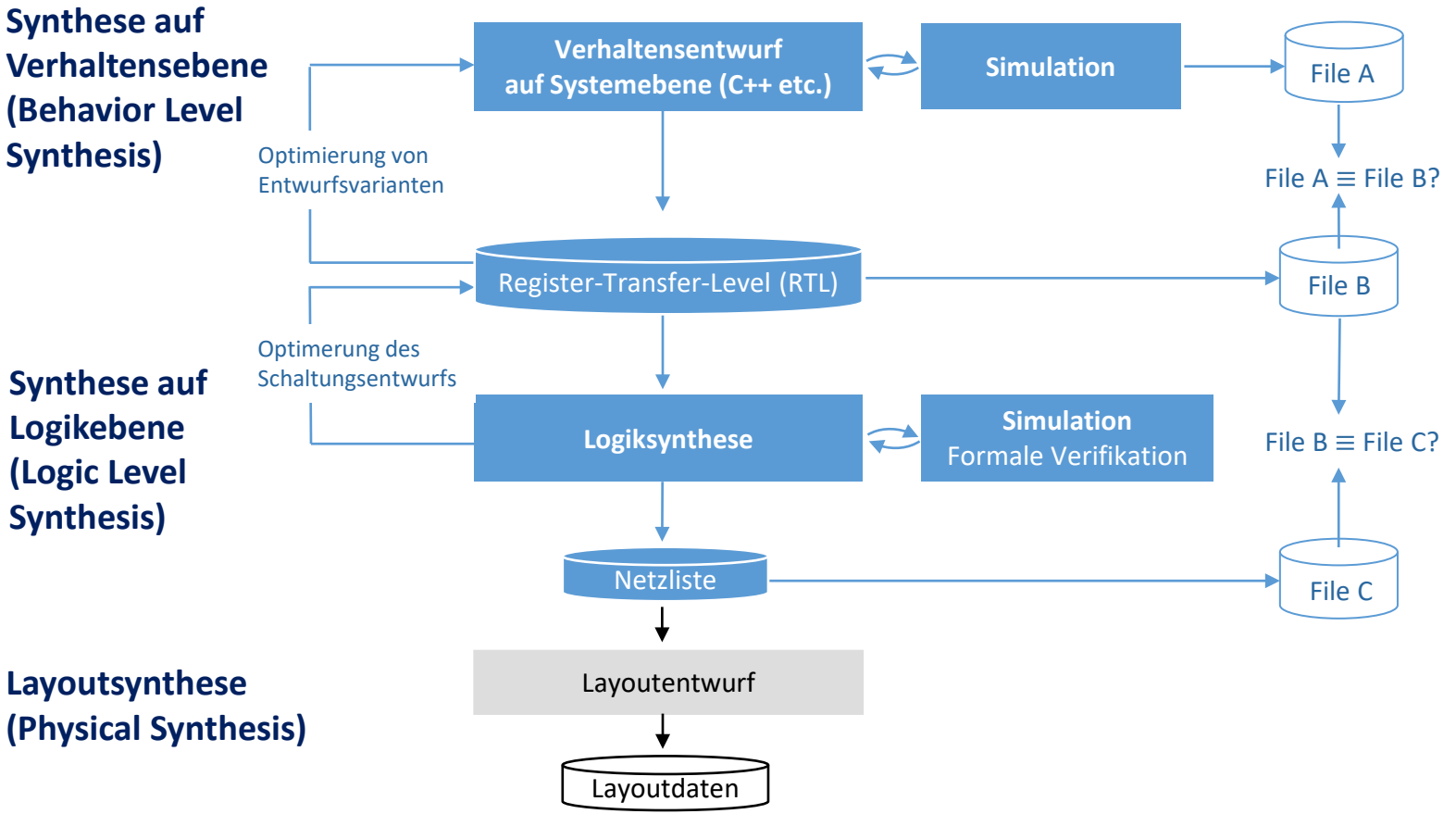



```
entity HALFADDER is
  port(A, B           : in bit;
       SUM, CARRY: out bit);
end entity HALFADDER;
```

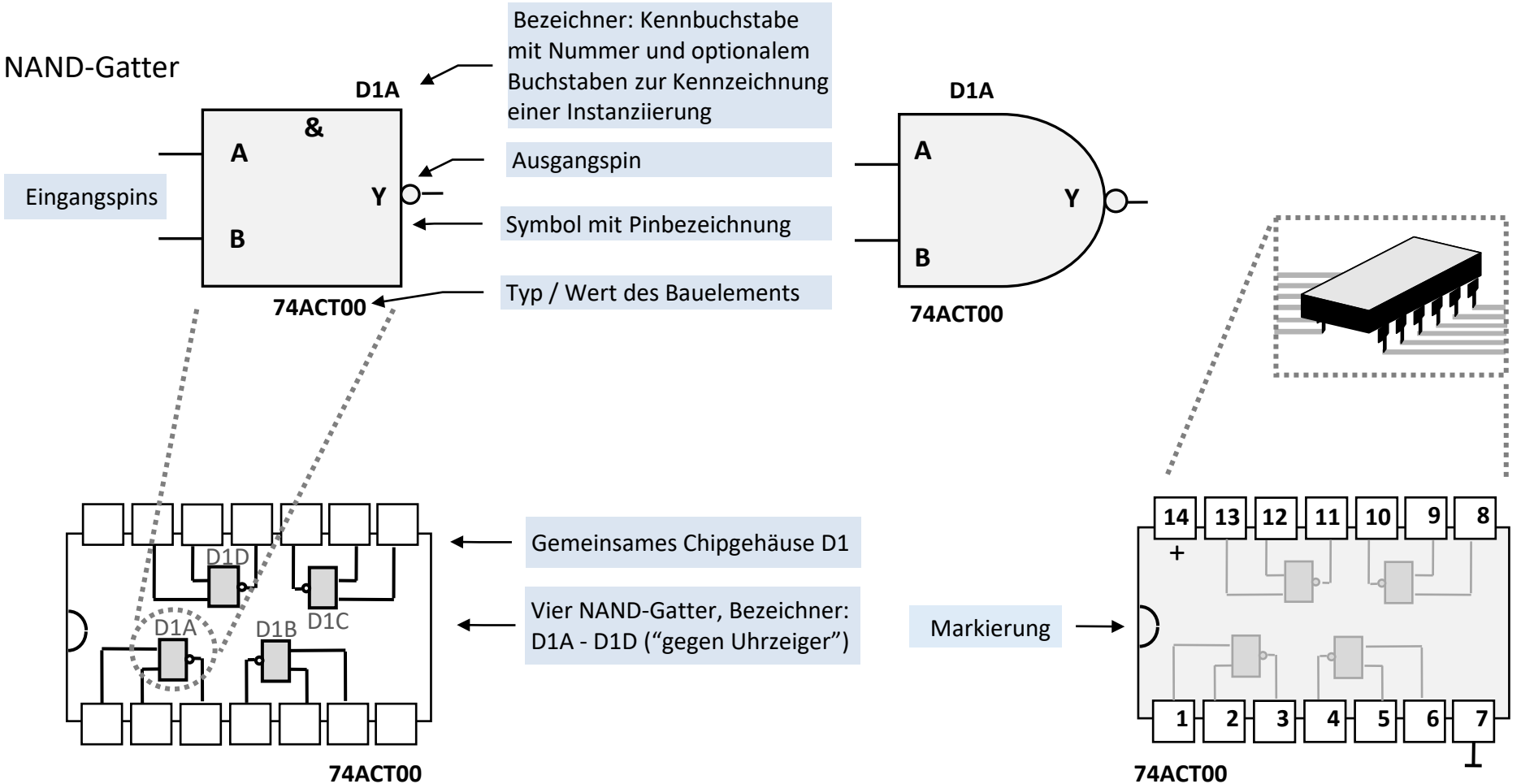
Aufbau und Implementierung

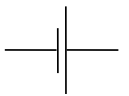
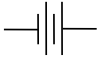
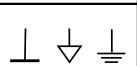
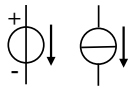
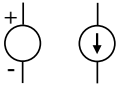
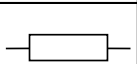
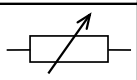
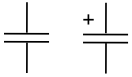
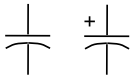


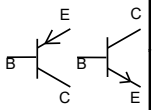
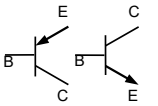
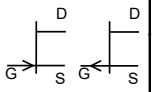
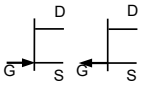
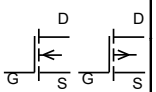
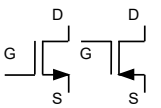
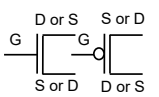
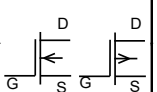
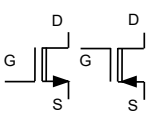
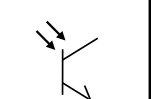
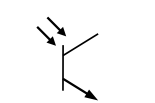

```
architecture RTL of HALFADDER is
begin
      SUM   <= A xor B;
      CARRY <= A and B;
end architecture RTL;
```

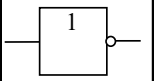
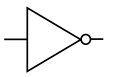
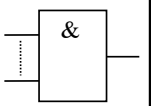
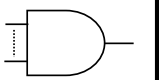
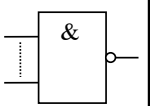
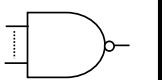
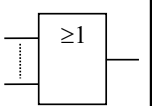
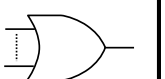
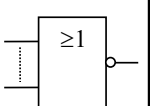
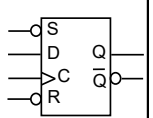


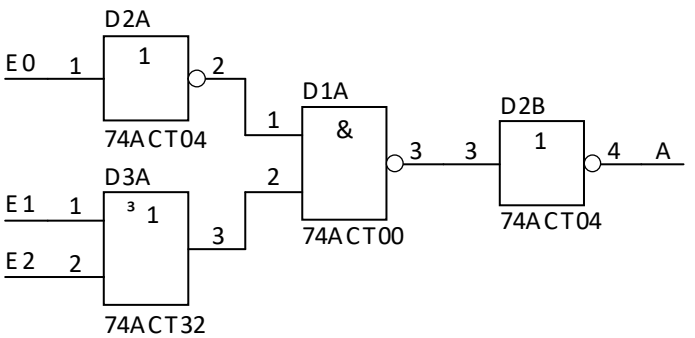
NAND-Gatter

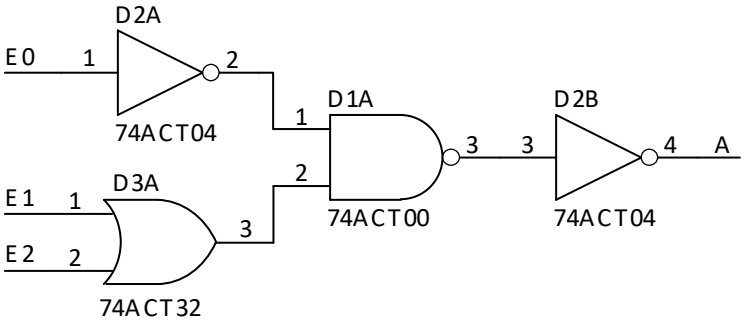


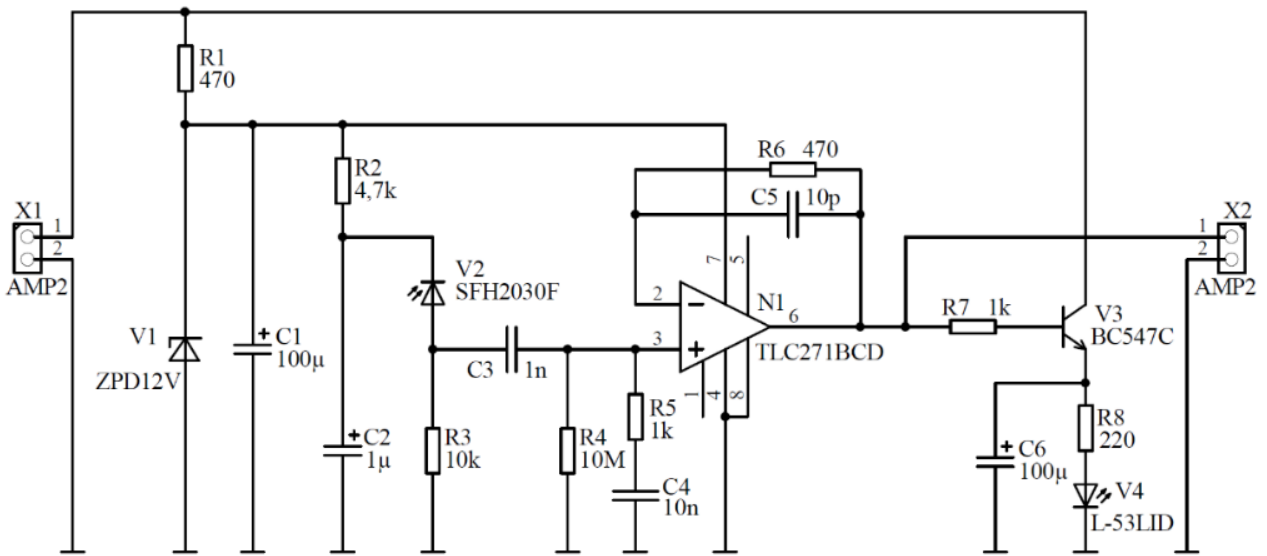
DIN/IEEE/IEC Symbol	Beschreibung	Alternatives/ ANSI-Symbol
	Primary cell, secondary cell, storage battery The longer line represents the positive pole, the shorter one the negative pole.	
	Ground symbols	
	DC voltage source DC current source	
	Resistor	
	Resistor, adjustable	
	Capacitor Polarized capacitor	
	Inductor, coil, winding, choke (without core)	
	Semiconductor diode; (triangle = anode, bar = cathode)	
	Light emitting diode (LED) Photo-diode	

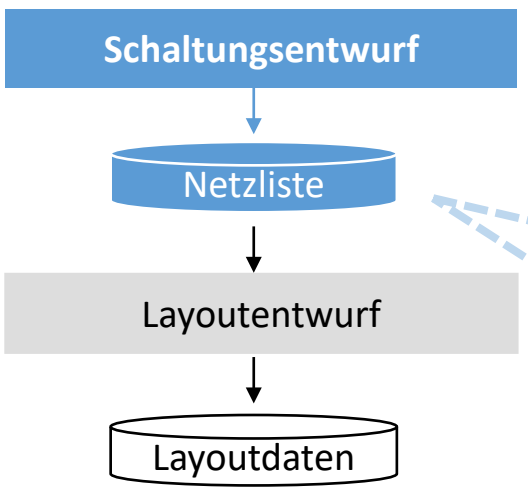
DIN/IEEE/IEC Symbol	Beschreibung	Alternatives/ ANSI-Symbol
	pnp- npn- transistor	
	n-channel p-channel Junction FET	
	n-channel p-channel Enhancement MOSFET	
	n-channel p-channel (n-MOS) (p-MOS) Enhancement MOSFET (digital representation)	
	n-channel p-channel Depletion MOSFET	
	Photo transistor (npn model)	

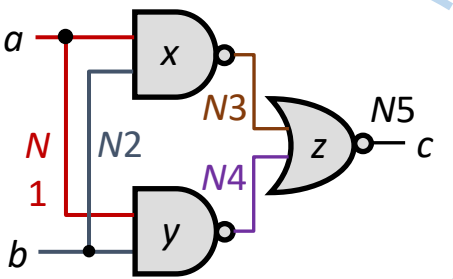
DIN/IEEE/IEC Symbol	Beschreibung	Alternatives/ ANSI-Symbol
	Inverter	
	AND gate	
	NAND (AND with negated output)	
	OR gate	
	NOR (OR with negated output)	
	D-Flipflop	
	Operational amplifier	









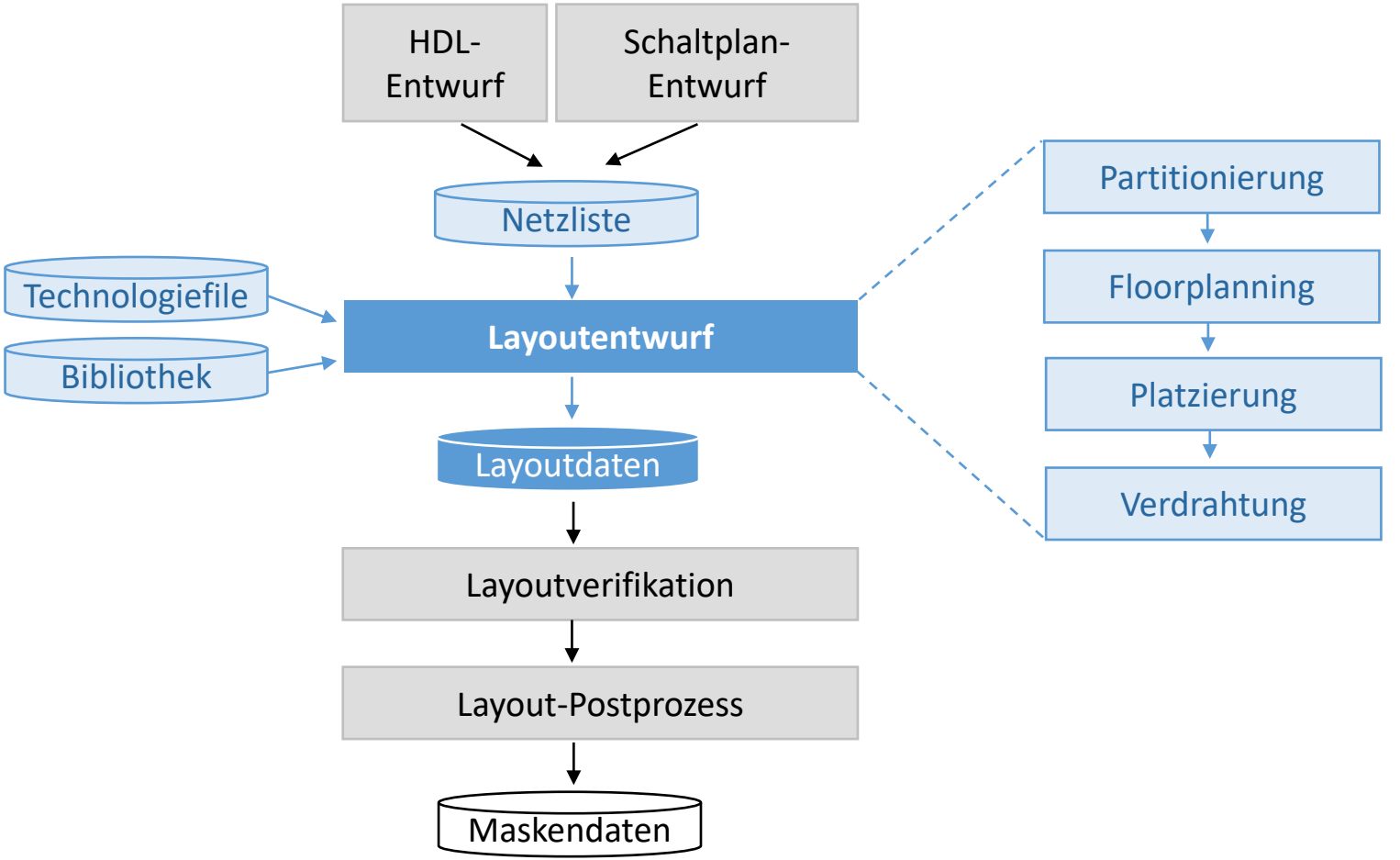


Netz-orientierte Netzliste

(*N*1: *a*, *x*.IN1, *y*.IN1)
(*N*2: *b*, *x*.IN2, *y*.IN2)
(*N*3: *x*.OUT, *z*.IN1)
(*N*4: *y*.OUT, *z*.IN2)
(*N*5: *z*.OUT, *c*)

Pin-orientierte Netliste

(*a*: *N*1)
(*b*: *N*2)
(*c*: *N*5)
(*x*: IN1 *N*1, IN2 *N*2, OUT *N*3)
(*y*: IN1 *N*1, IN2 *N*2, OUT *N*4)
(*z*: IN1 *N*3, IN2 *N*4, OUT *N*5)



Systemebene

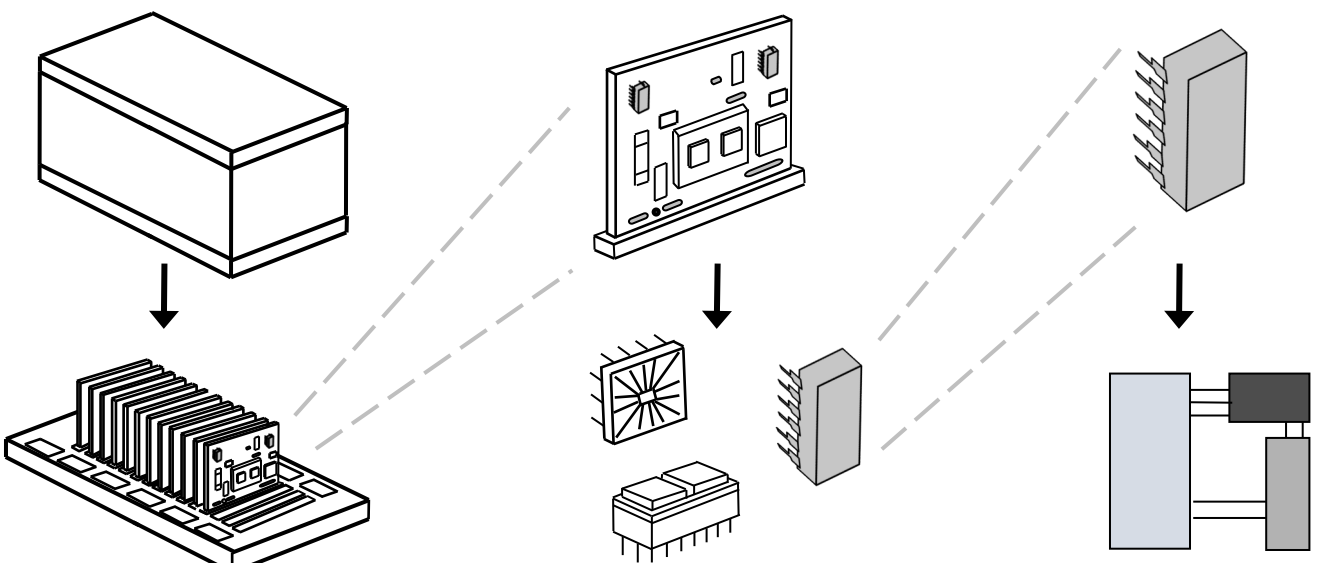
Jedes Subsystem (Leiterplatte) kann unabhängig entworfen und gefertigt werden

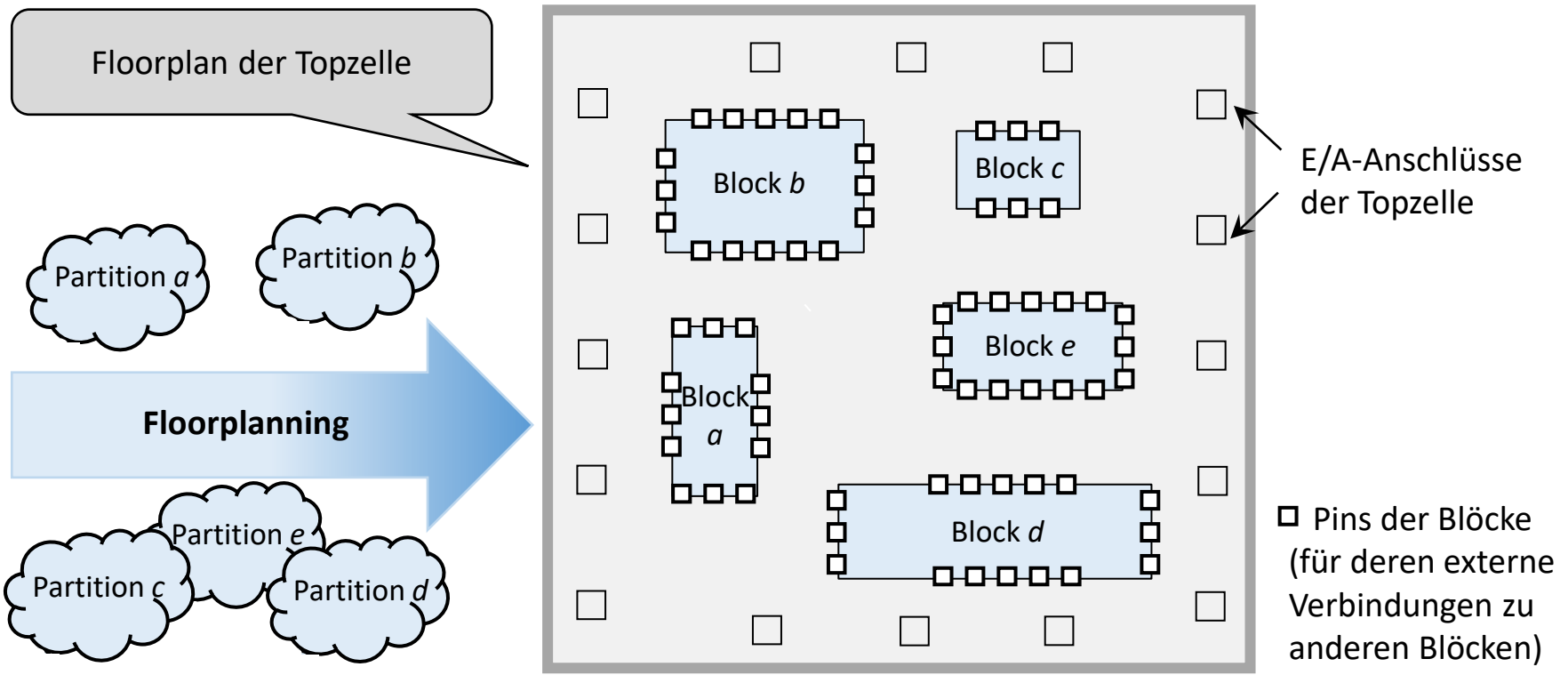
Leiterplattenebene

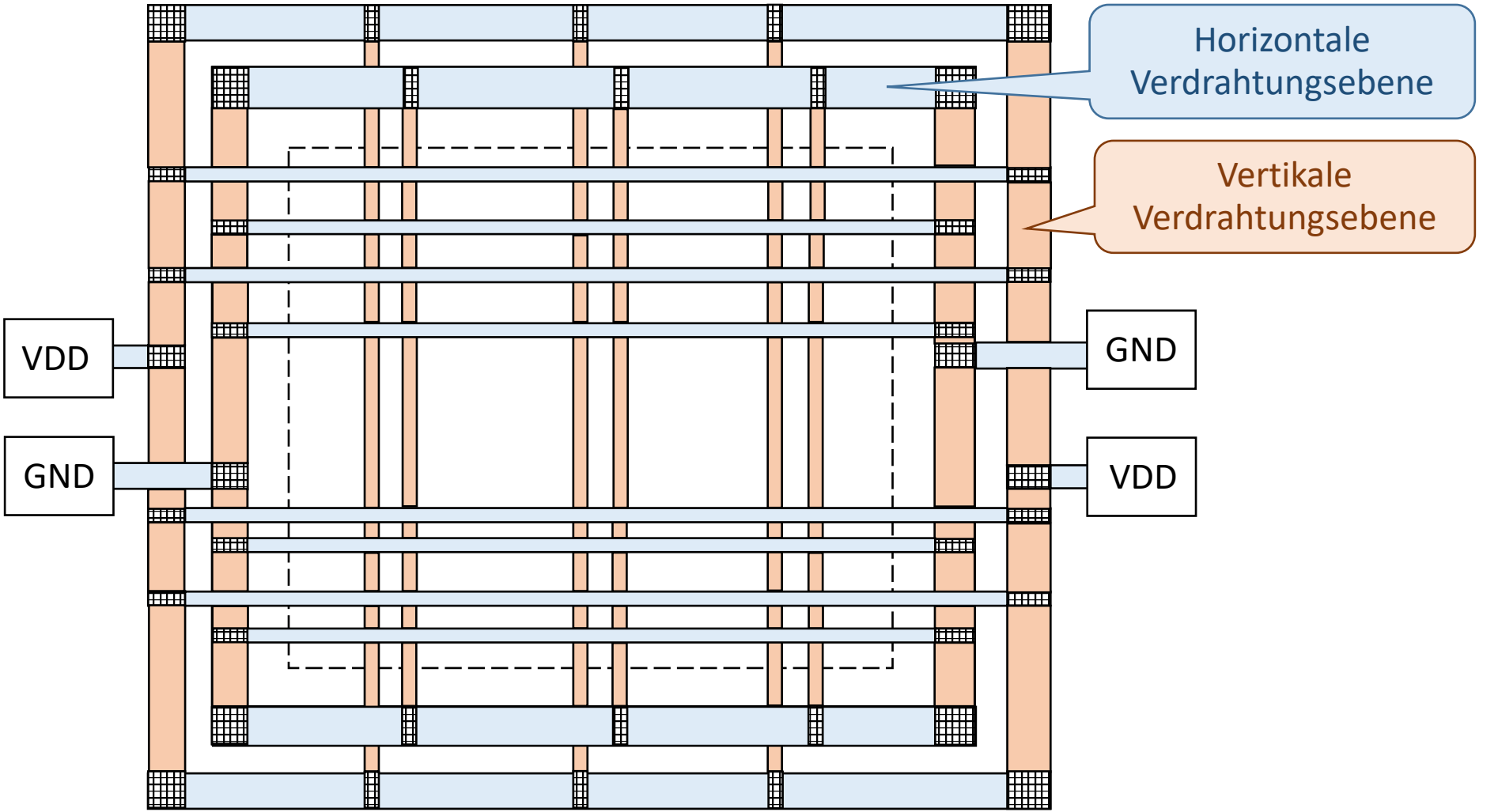
Ermittlung von Teilschaltungen auf einer Leiterplatte, die als IC/MCM realisierbar sind

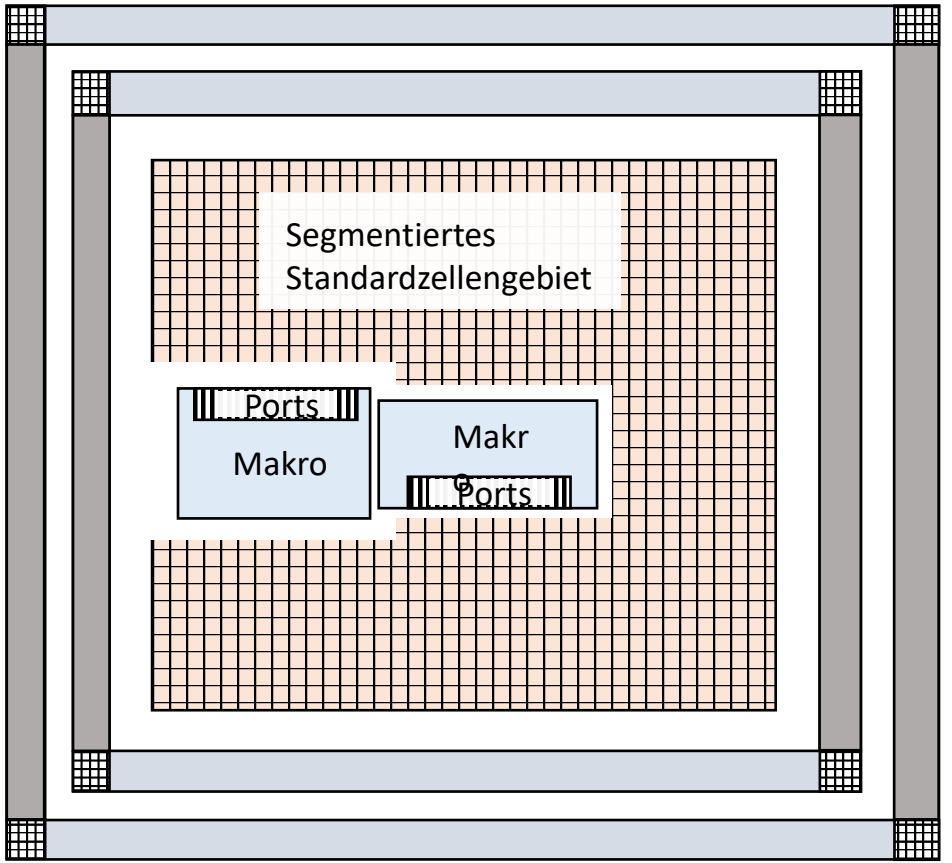
IC-Ebene

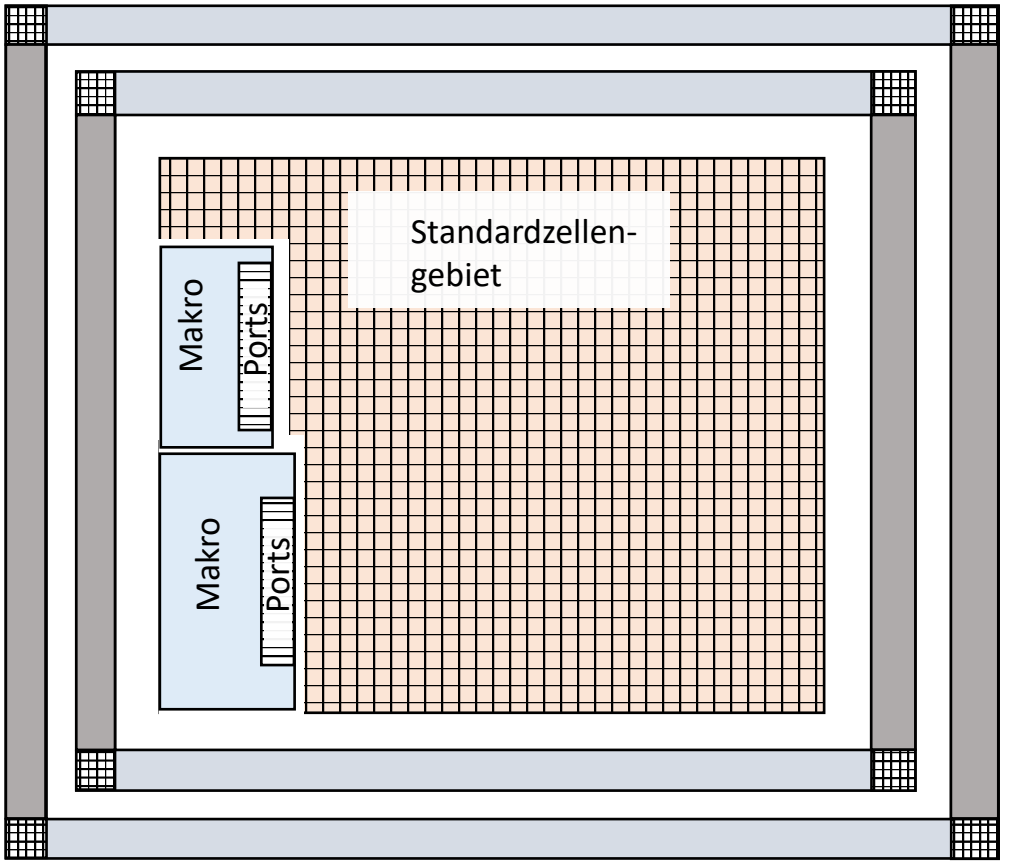
IC-Schaltungen werden aus Komplexitätsgründen oft in Blöcke aufgeteilt, um sie unabhängig voneinander zu entwerfen

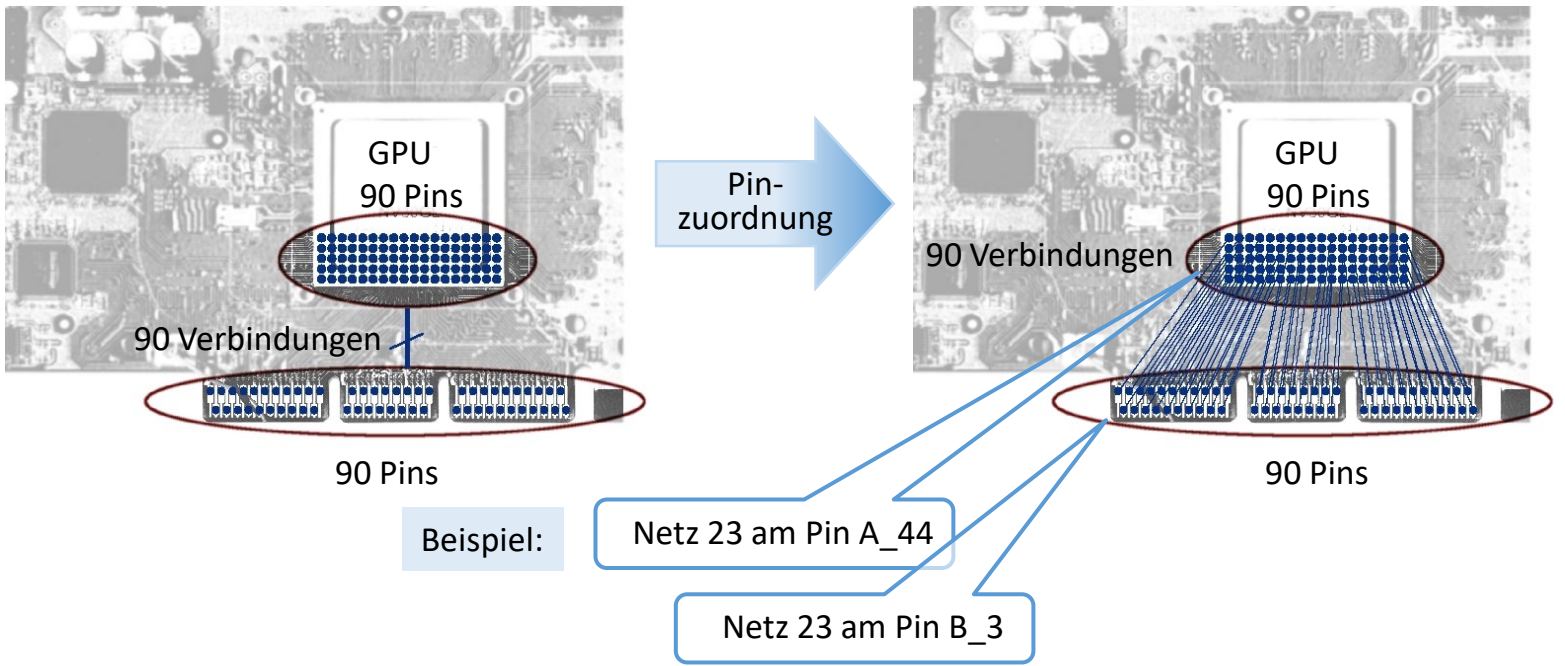


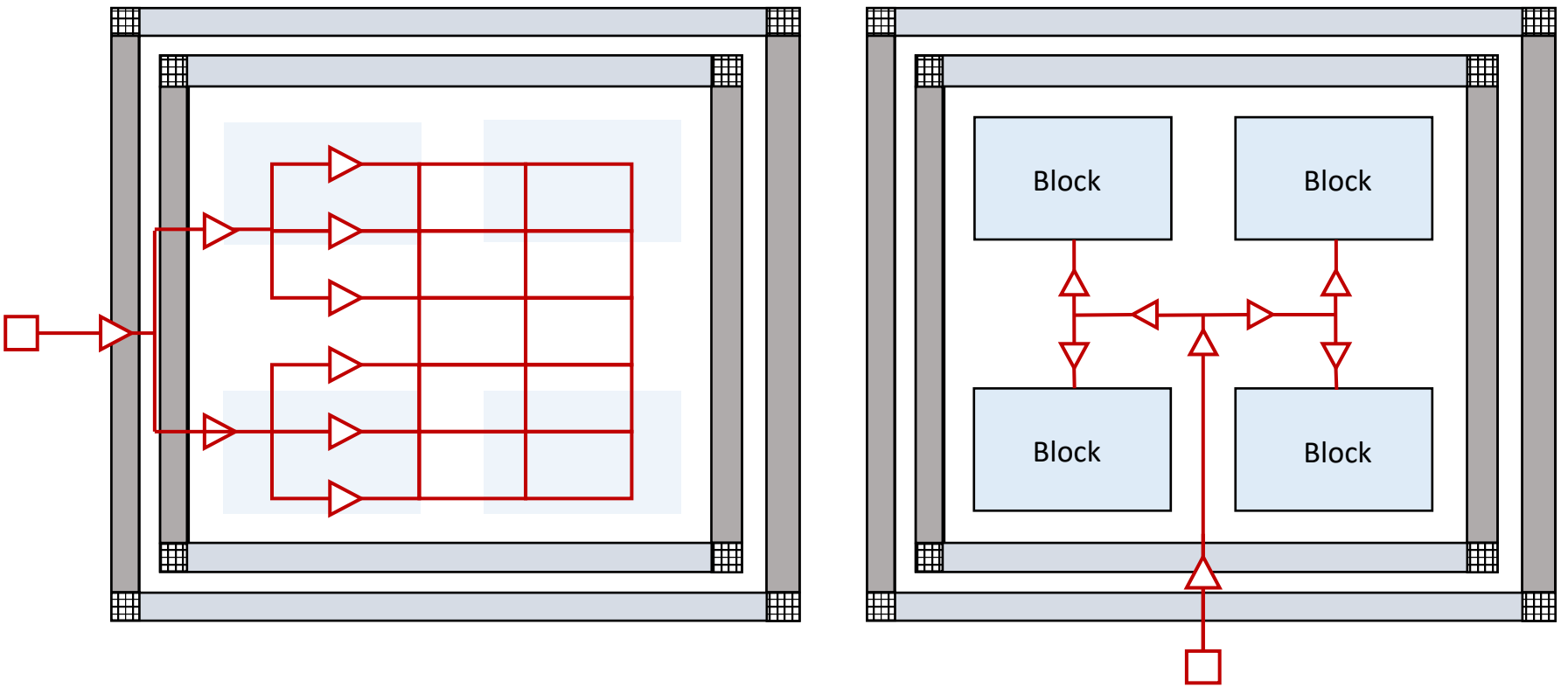


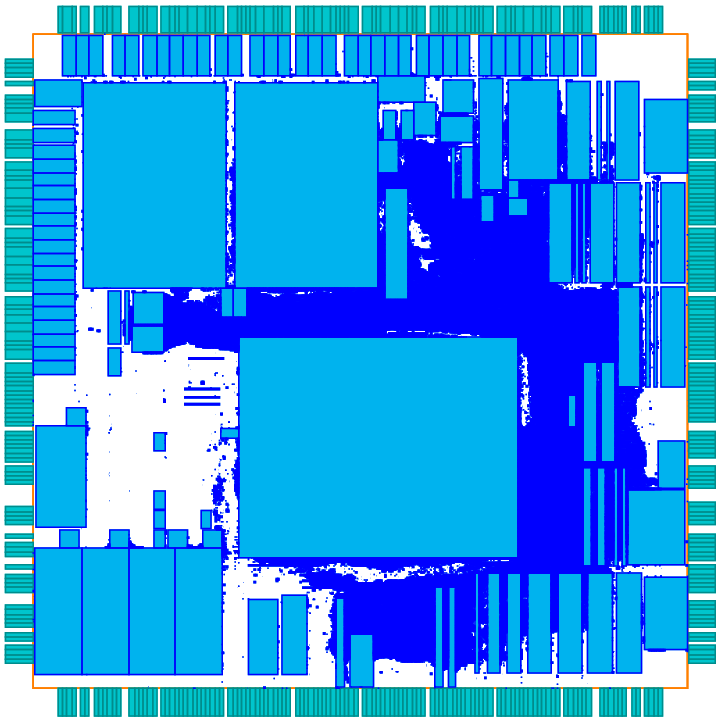


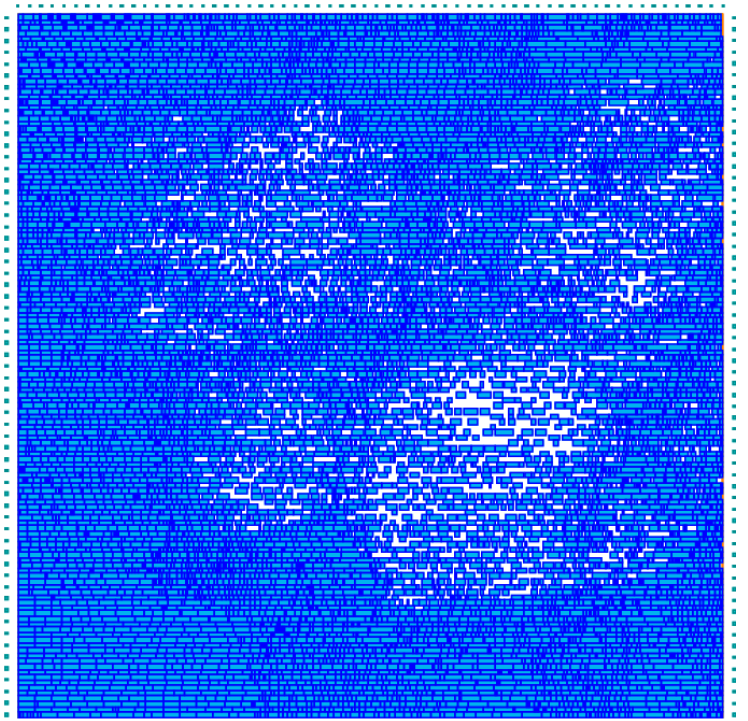


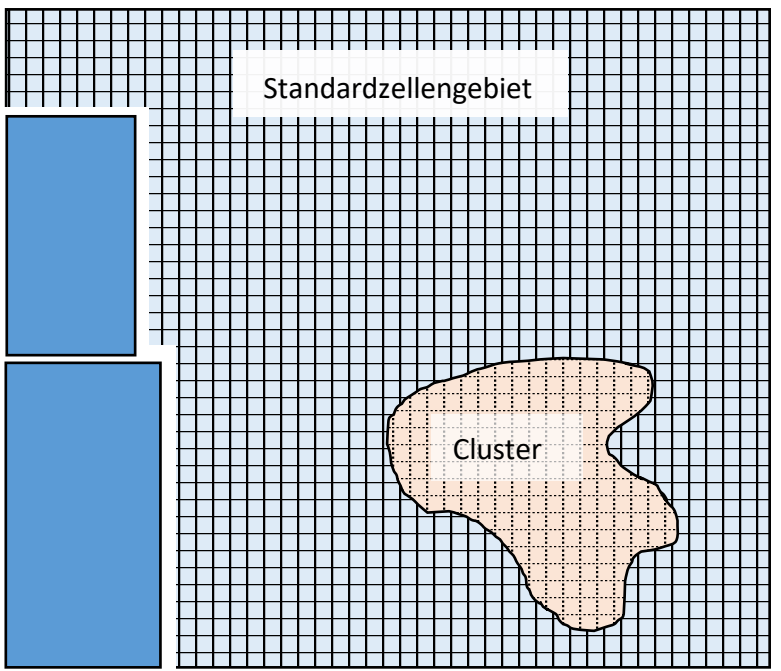


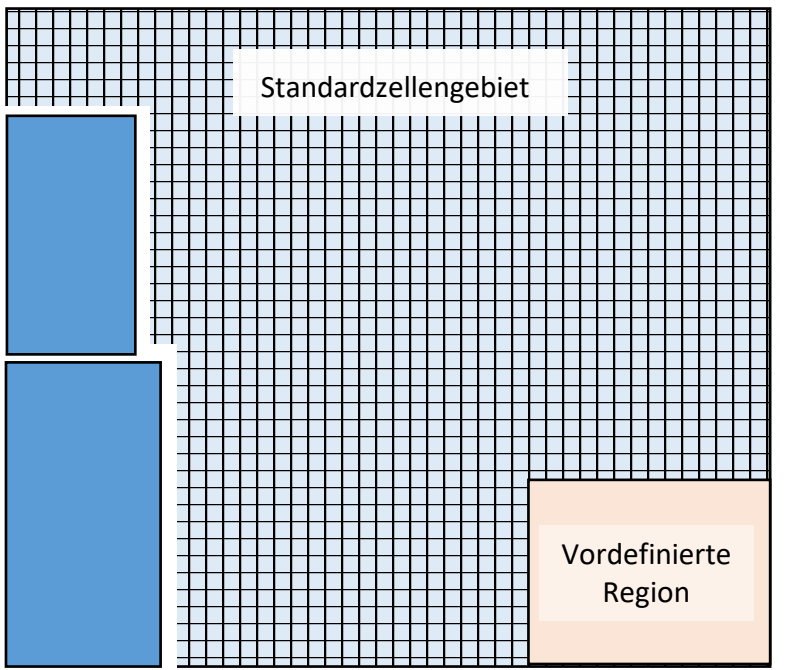


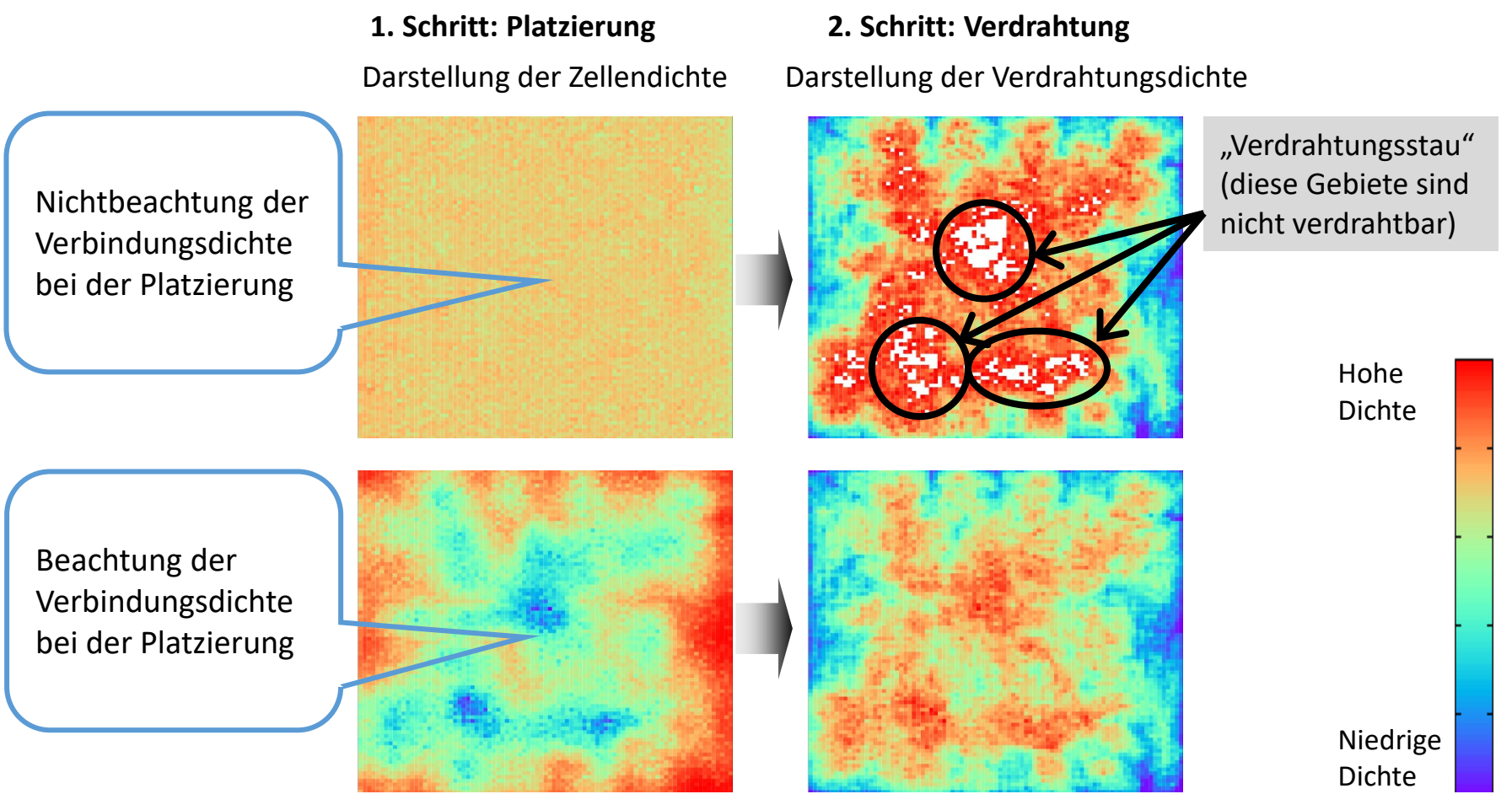


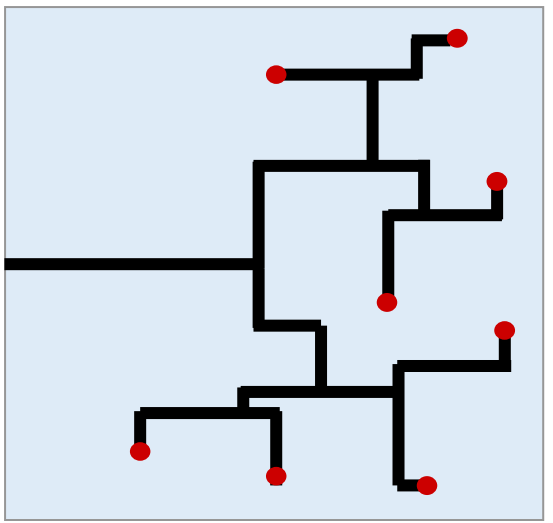




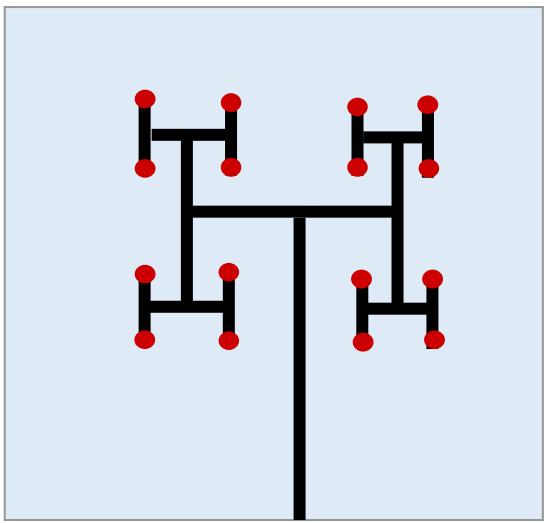




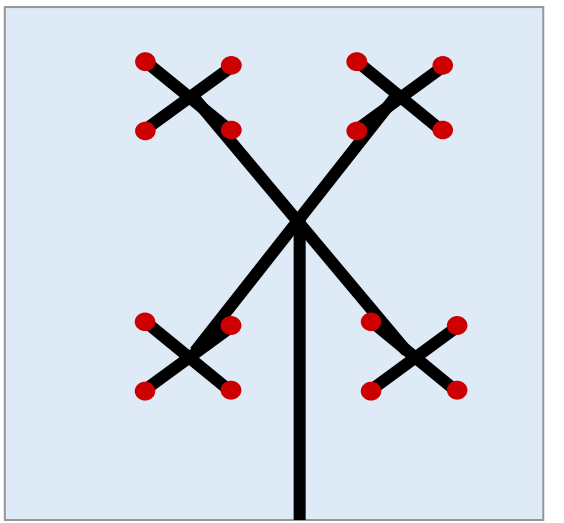




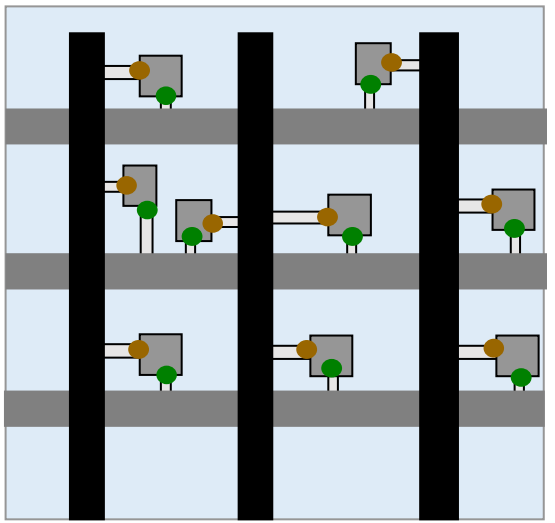
Ausgleichende Baumstruktur
(Balanced tree)



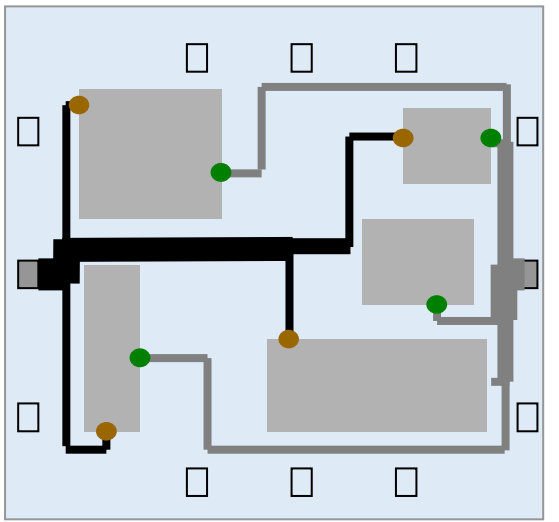
H-Baum
(H tree)



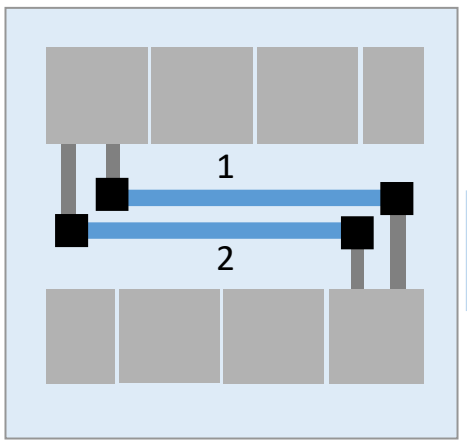
X-Baum
(X tree)



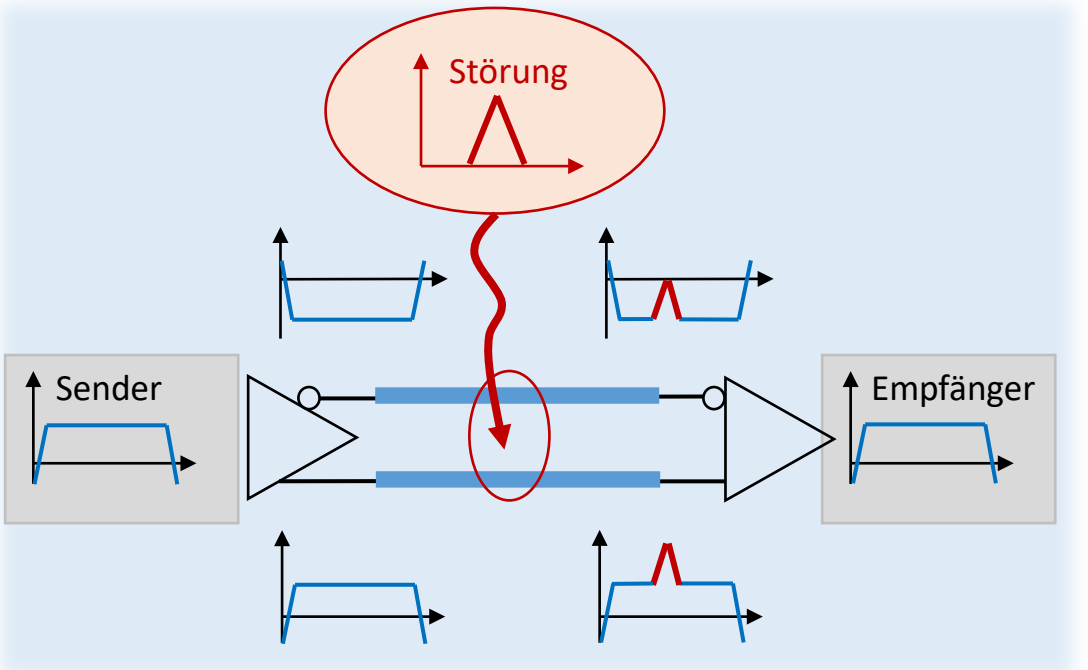
Versorgungsgitter
(Power mesh)



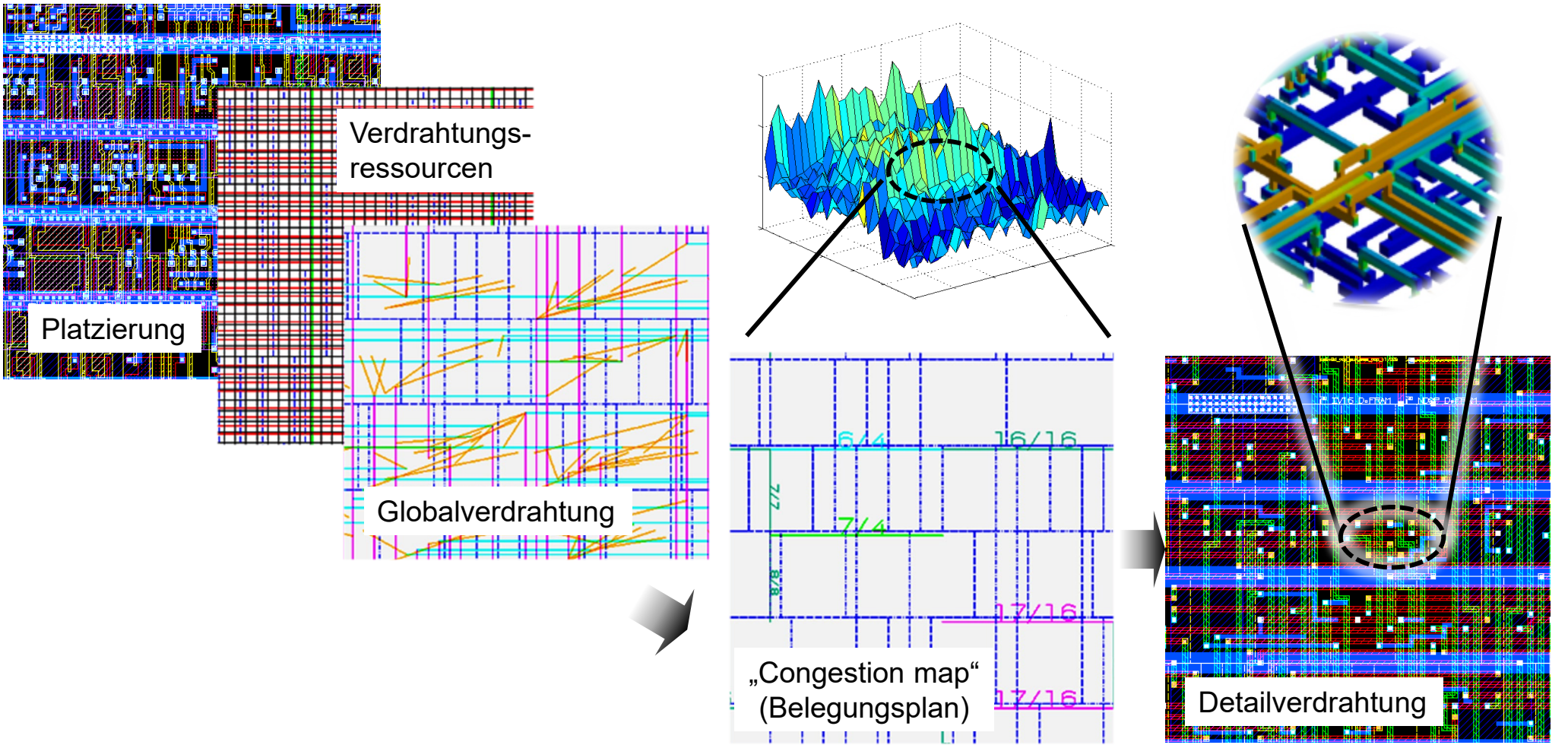
Versorgungsbaum
(Power tree)

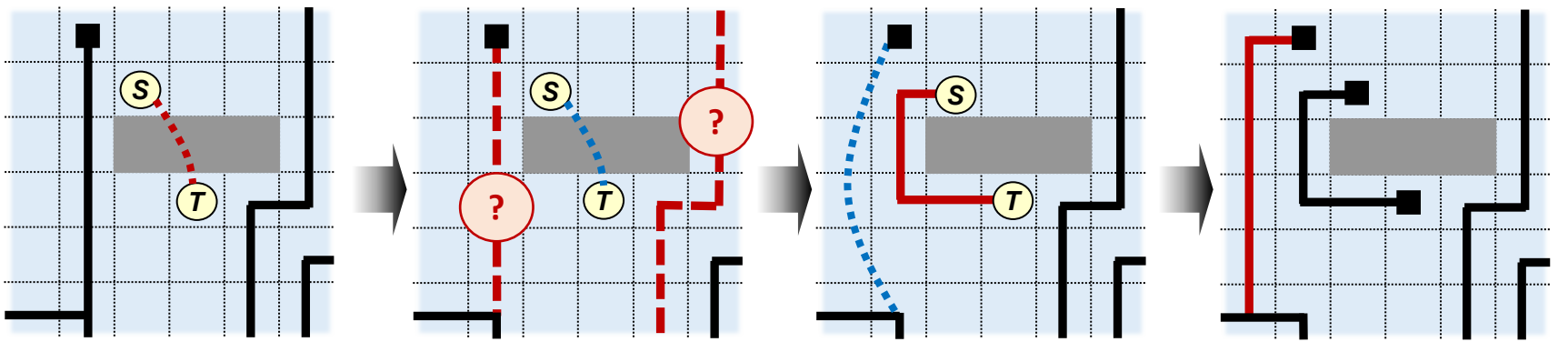


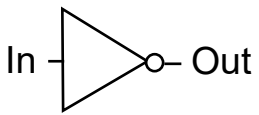
Differenzielle Signalübertragung

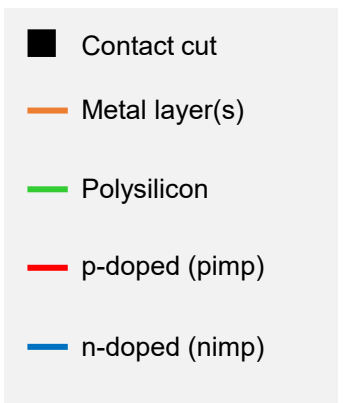


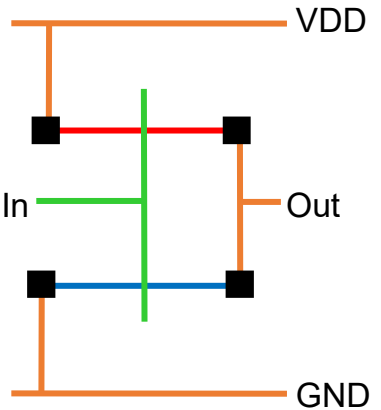
Symmetrische Signalführung
$(R_1, C_1) = (R_2, C_2)$



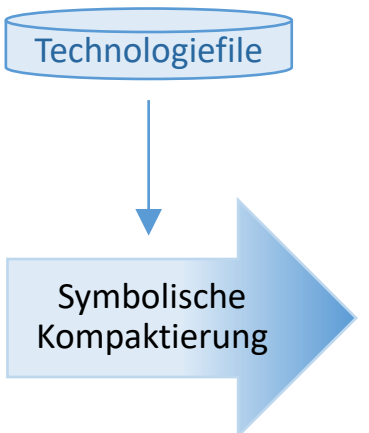


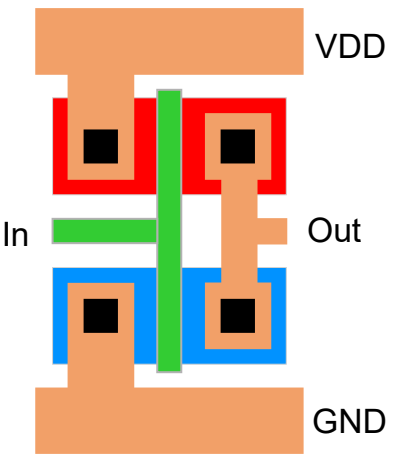




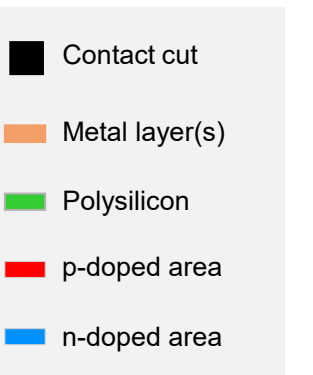


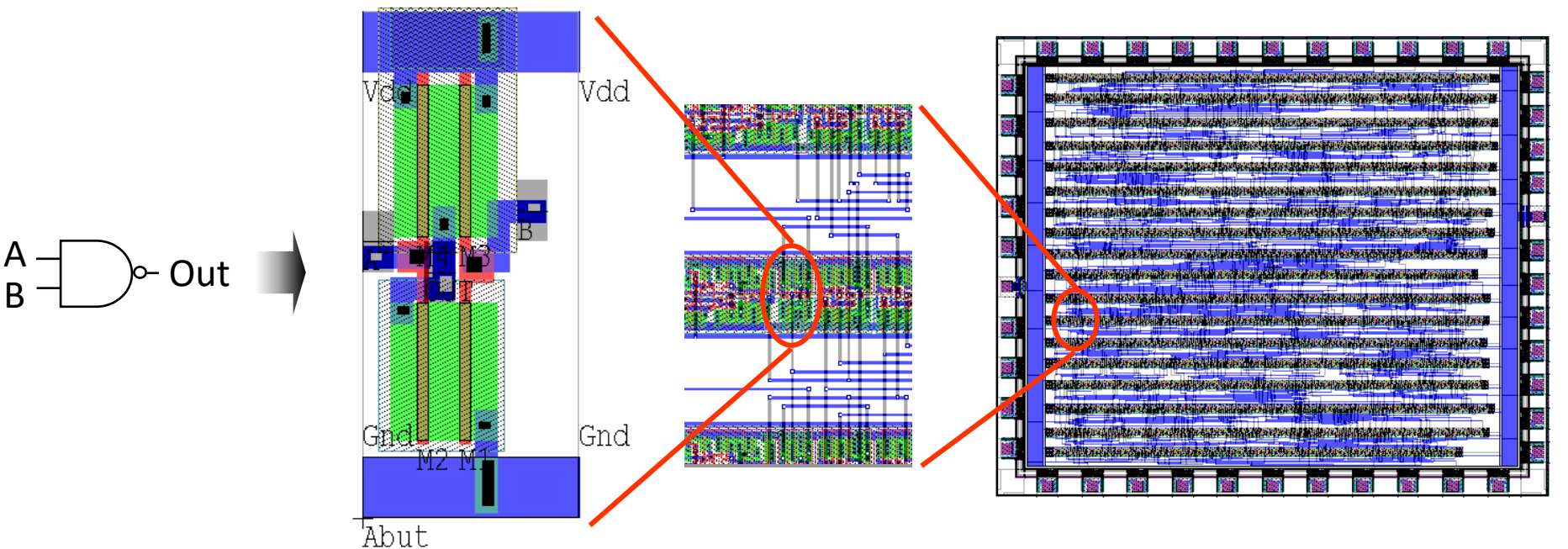
Stickdiagramm
(Technologie-unabhängig)

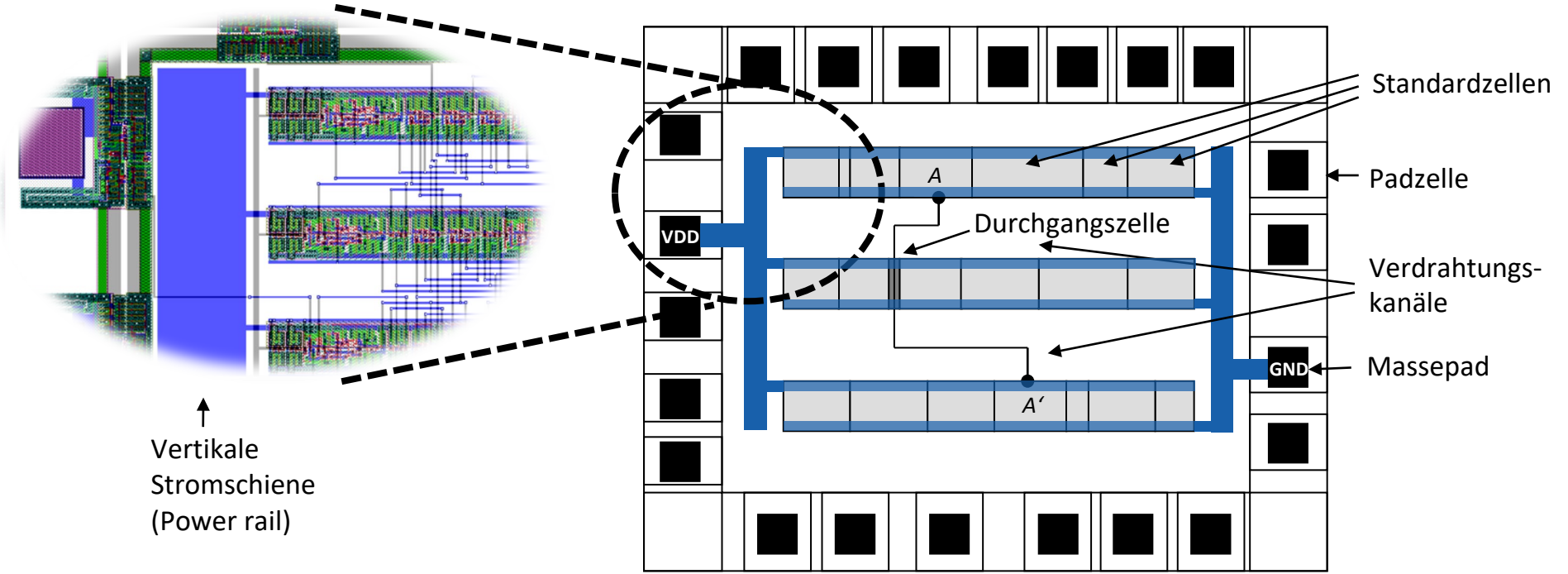


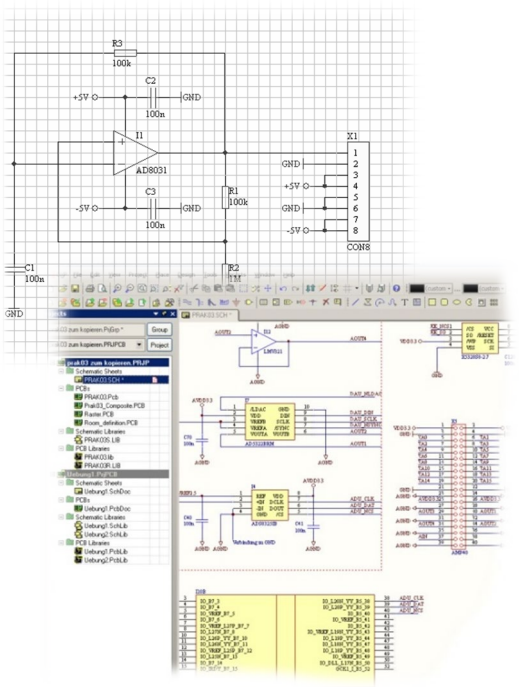


Maskenlayout
(Technologie-konform)

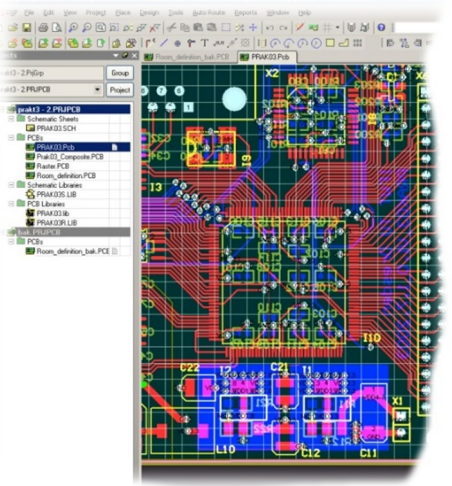




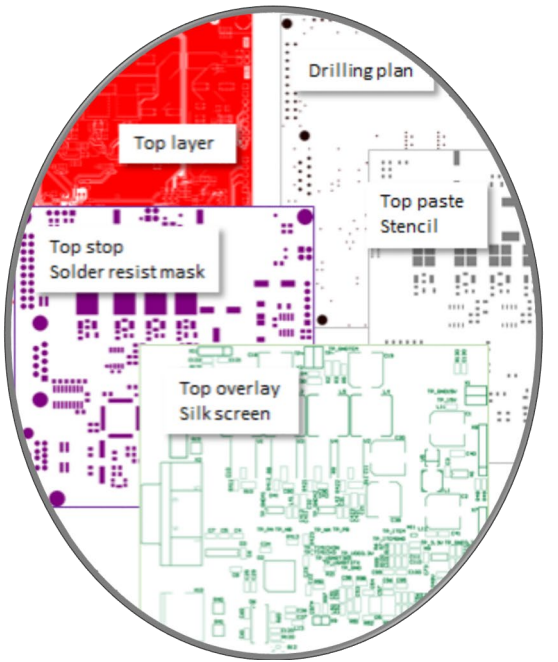




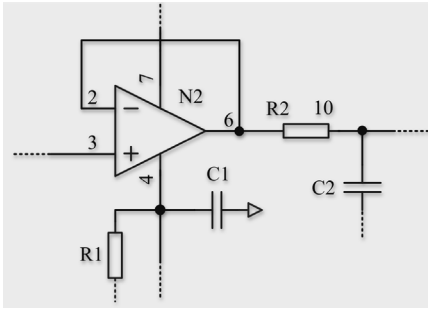
Schaltplaneingabe

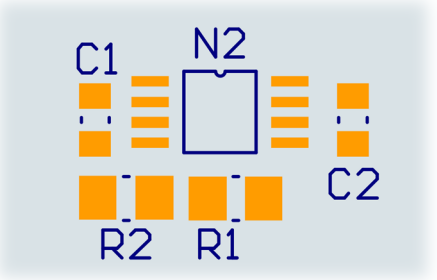


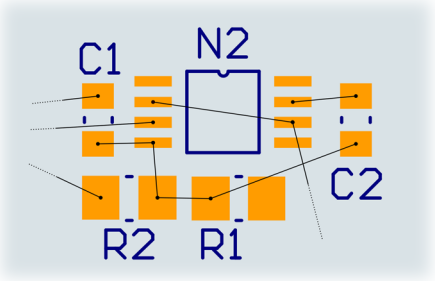
PCB-Layoutentwurf

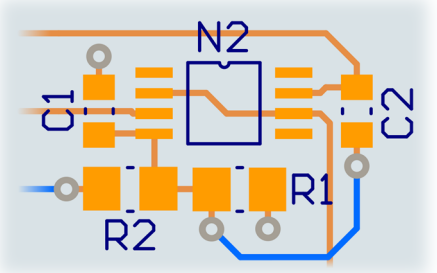


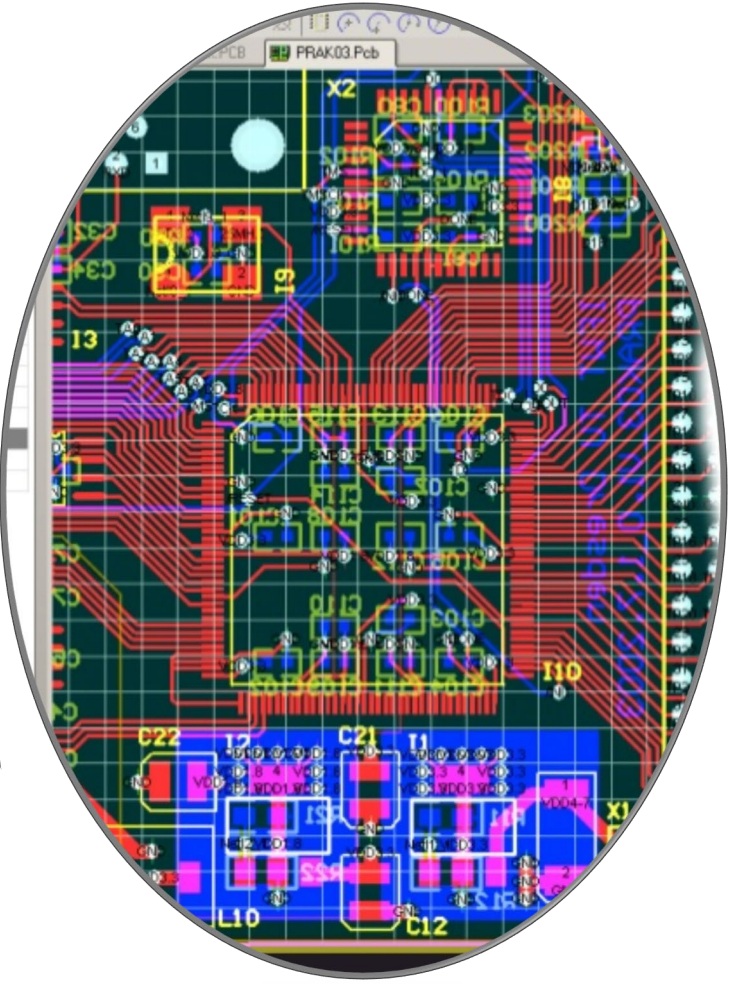
Erstellung von Fertigungsdaten



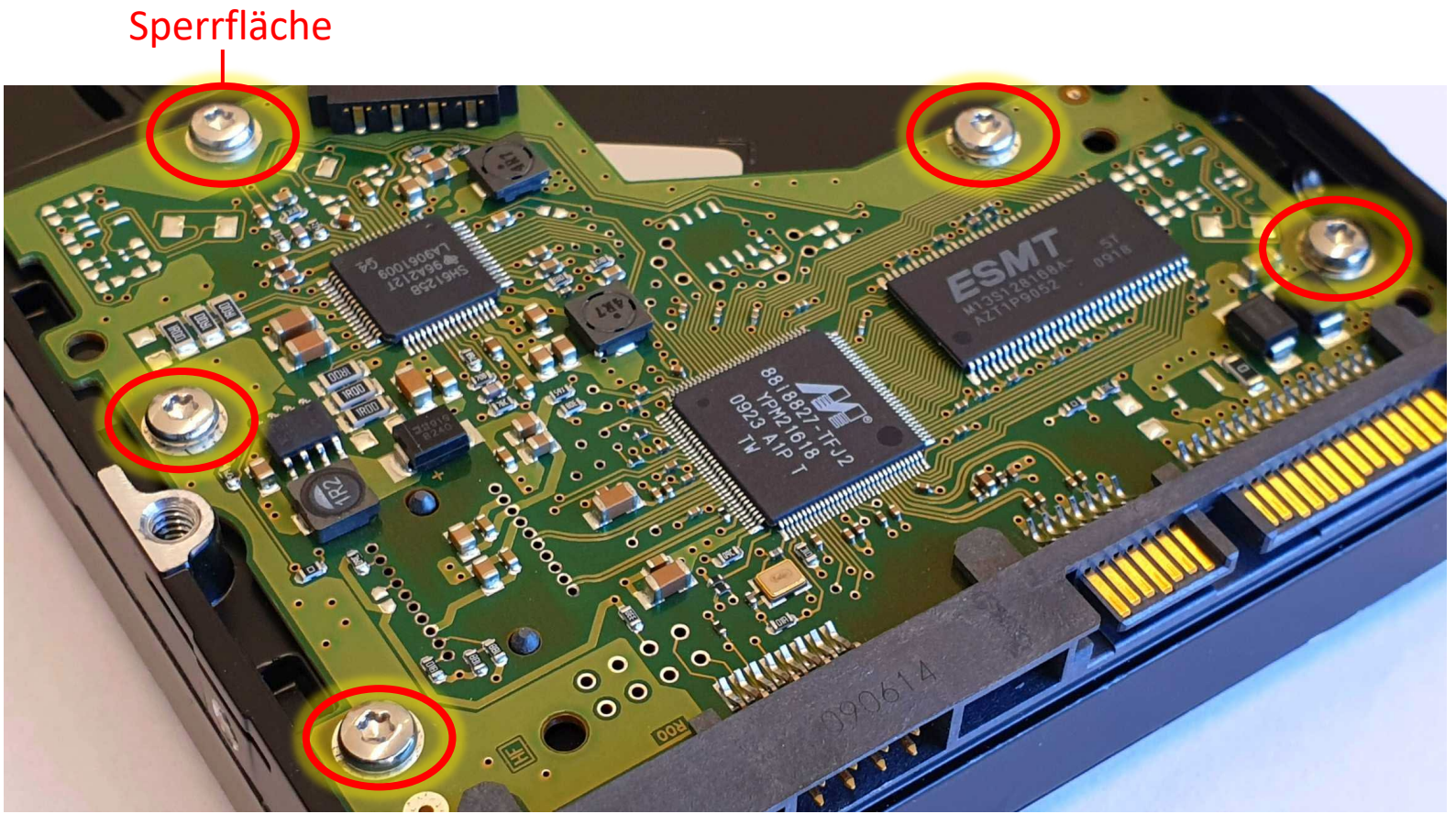


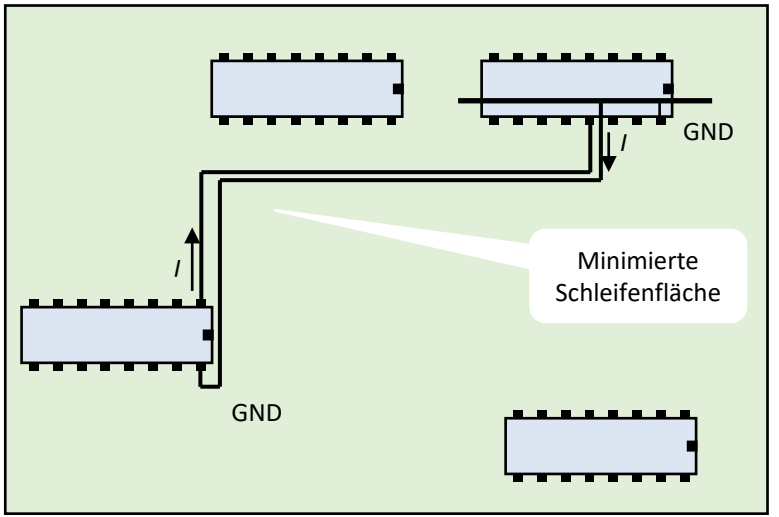


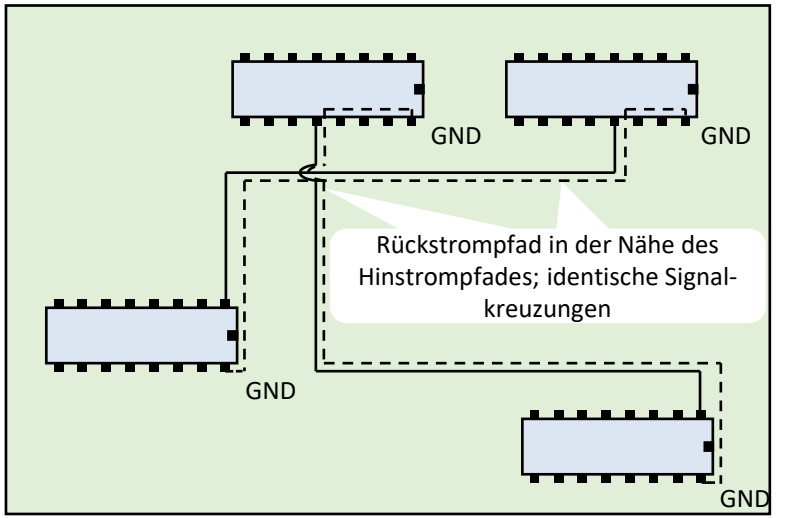


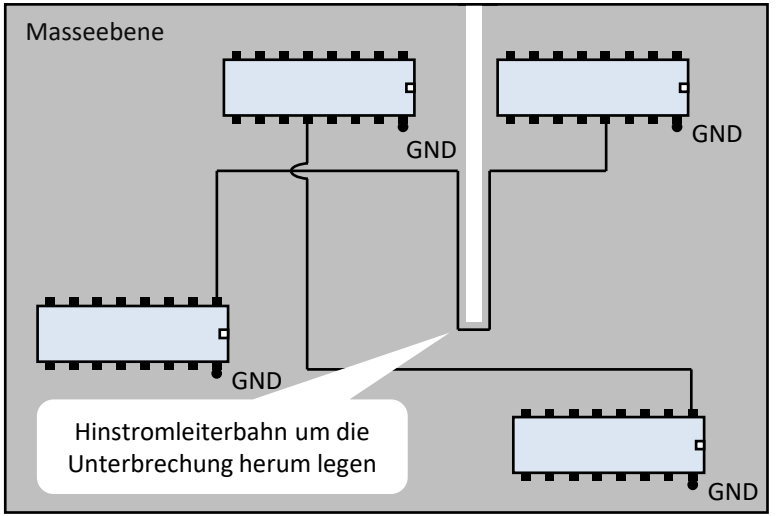


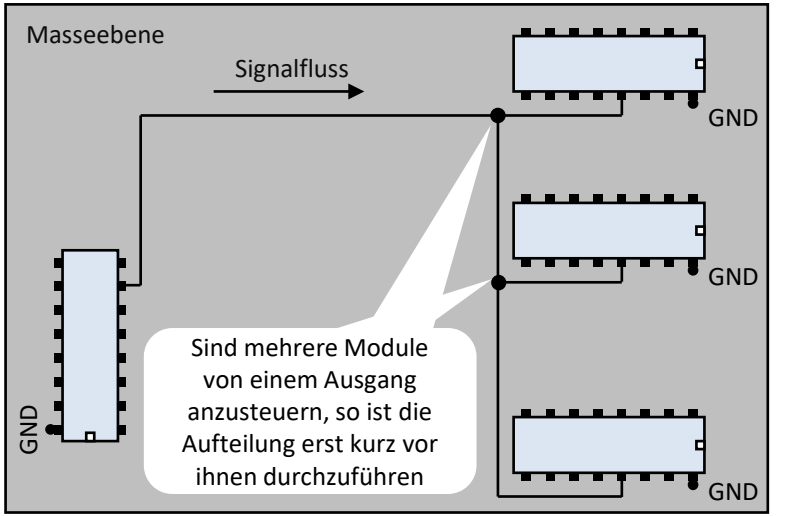
PCB-Layout

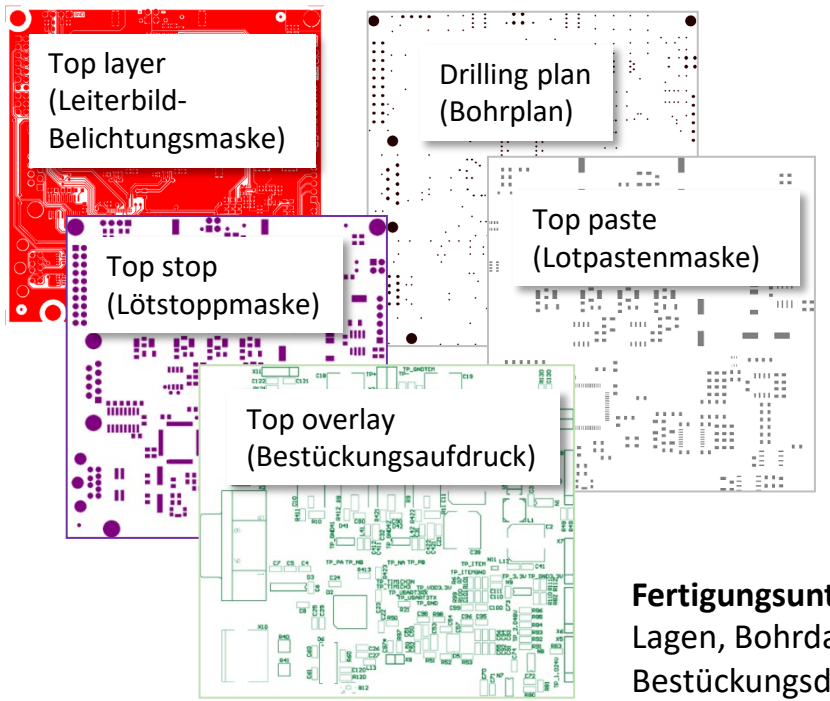




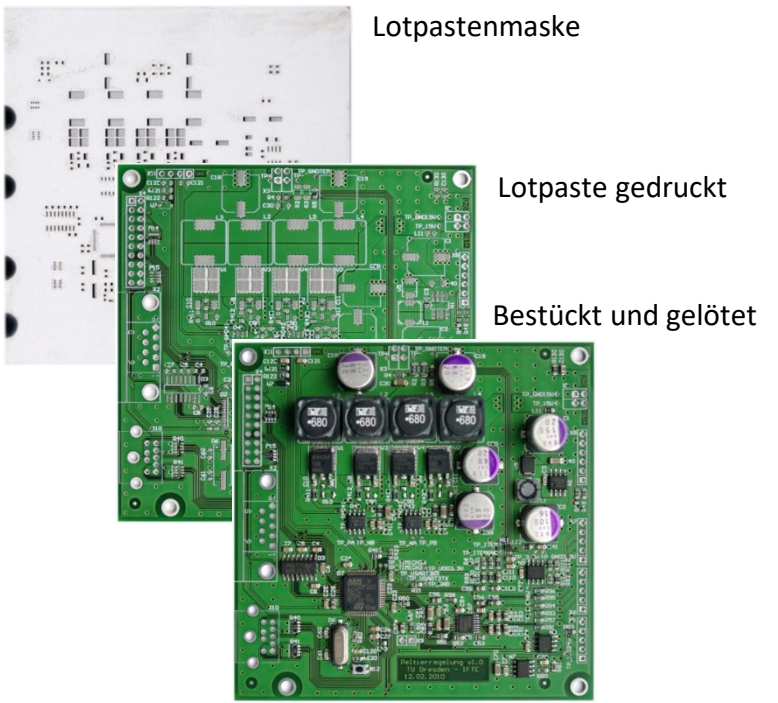


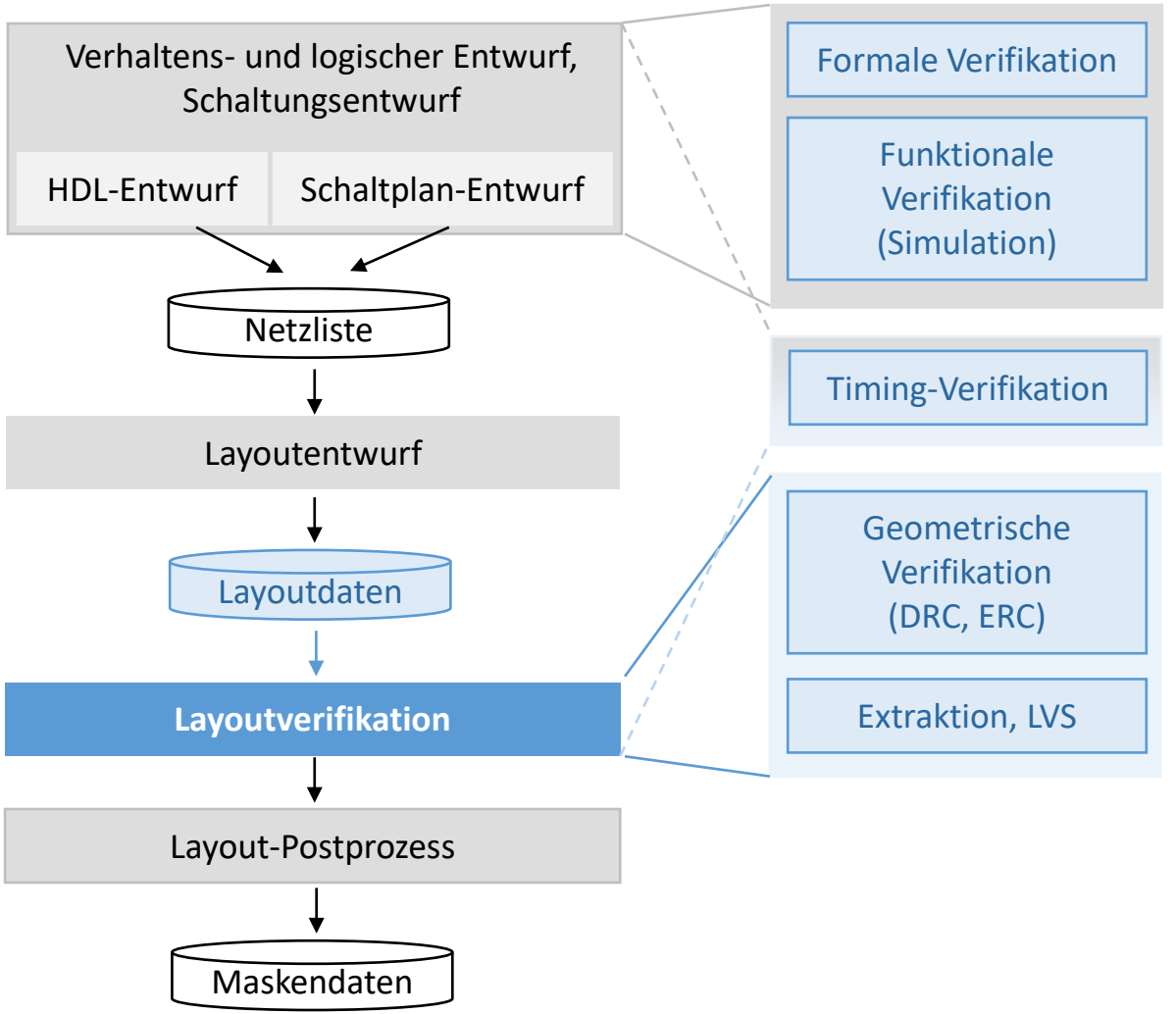


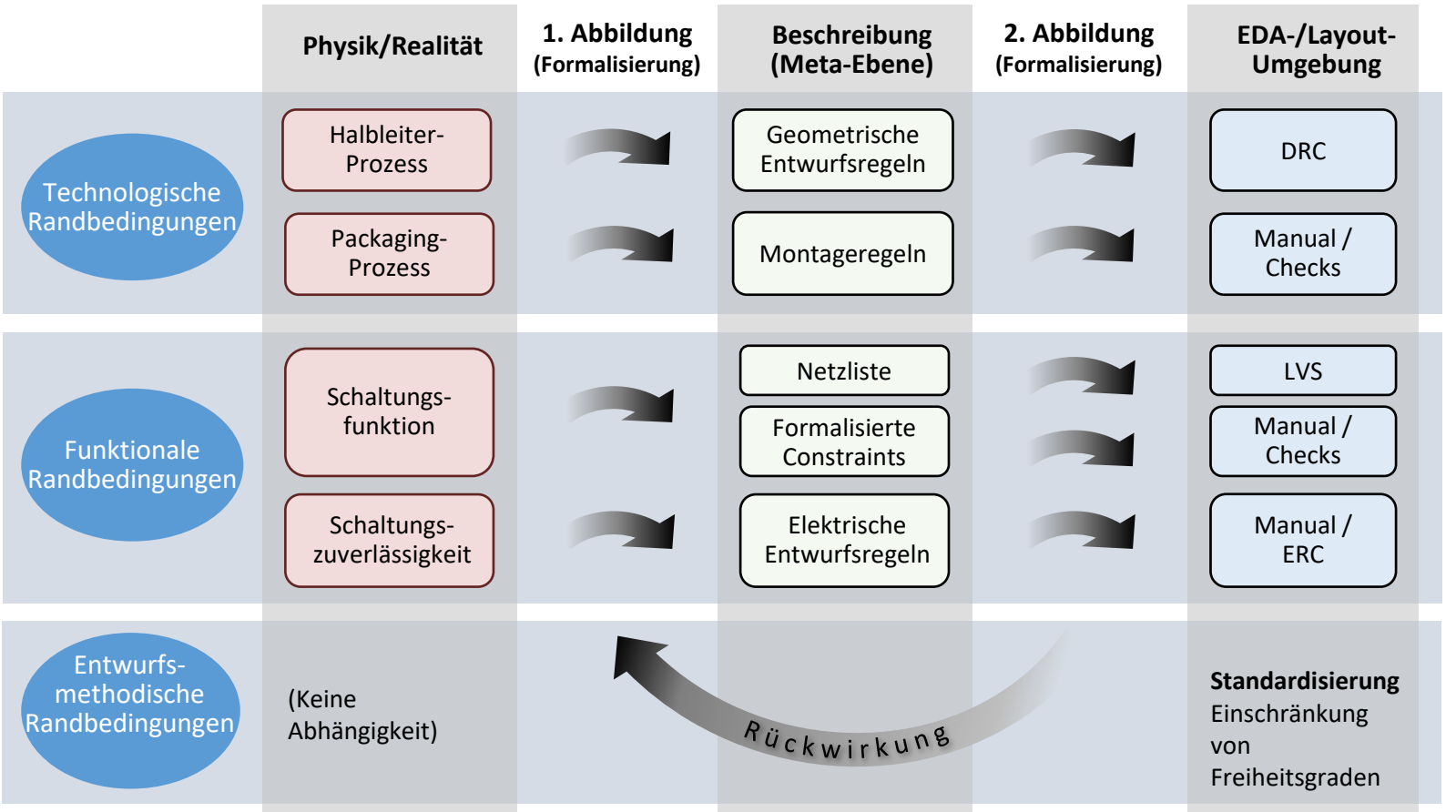




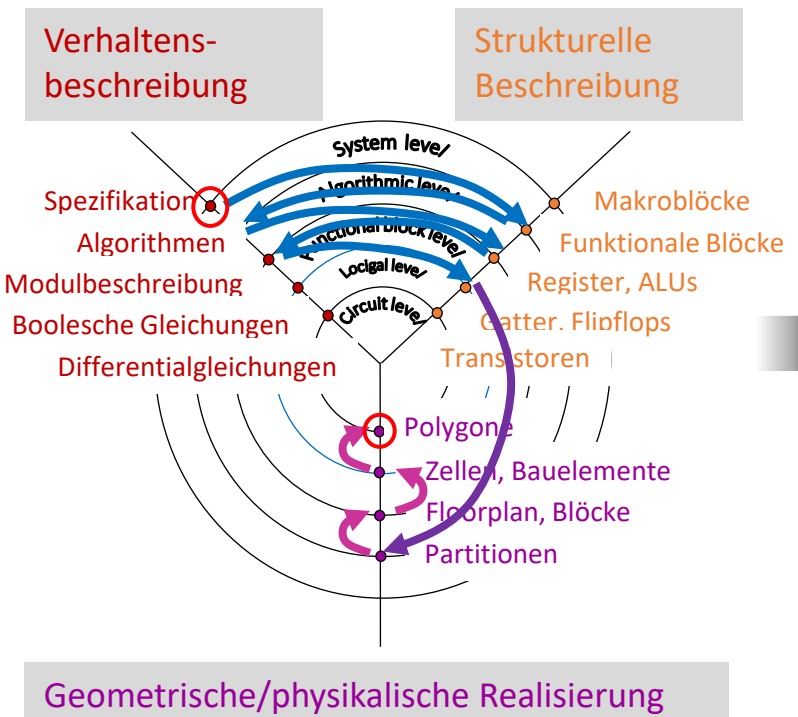
Fertigungsunterlagen
Lagen, Bohrdaten,
Bestückungsdaten

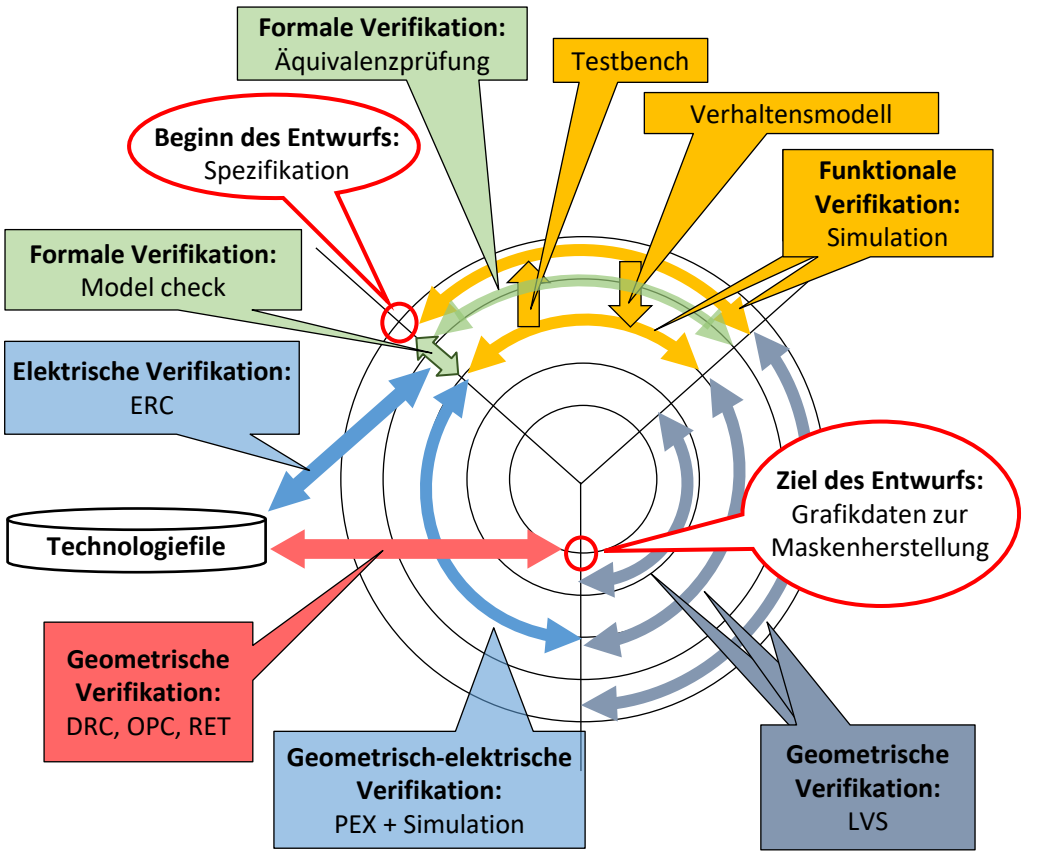


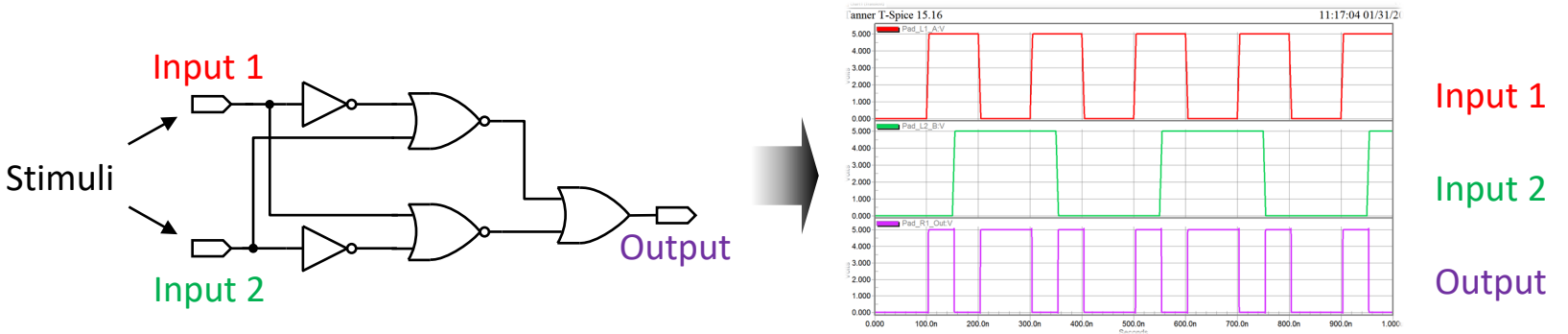


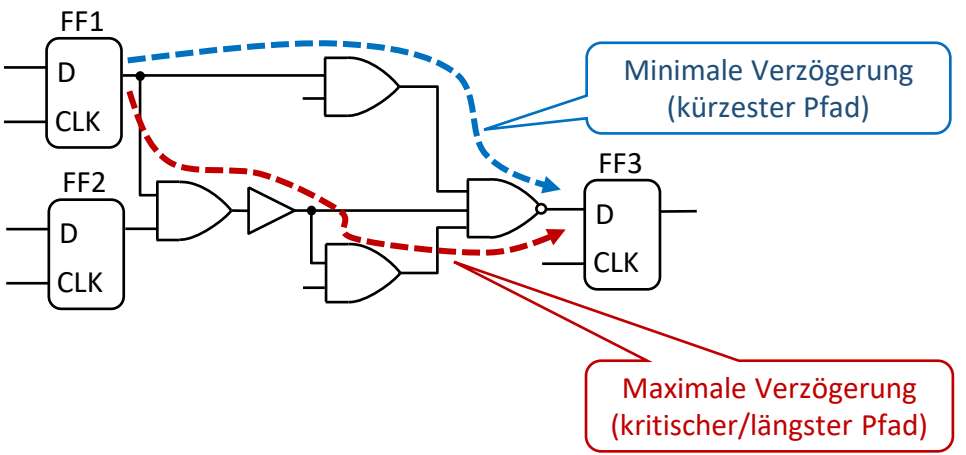


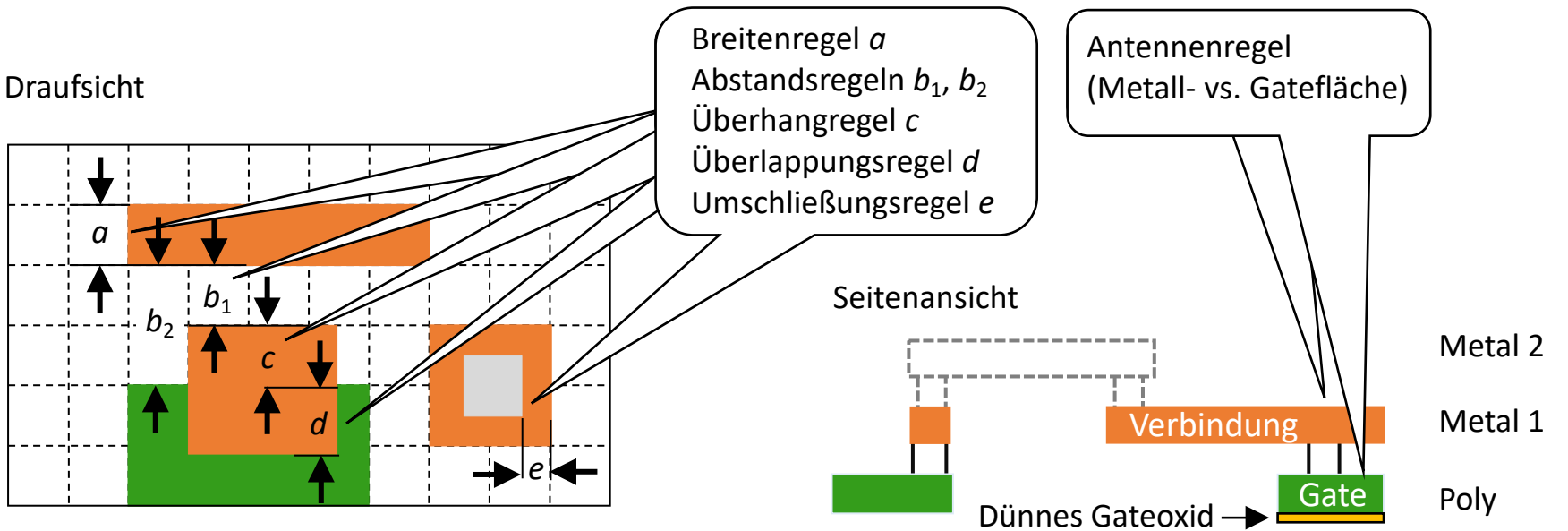
Prüfung	Was wird geprüft?	Wie wird geprüft?	Typ
Modellprüfung (Model check)	Logisches Merkmal (Vermutung ist wahr?)	Mathematische Modelle	Formale Verifikation
Äquivalenzprüfung	Logische Gleichwertigkeit von zwei Beschreibungen	Mathematische Modelle	Formale Verifikation
Simulation	Schaltungsverhalten vs. Spezifikation	Virtuelles Experiment (Stimuli und Kennlinie)	Funktionale Verifikation
DRC (OPC, RET)	Layout vs. technologische Randbedingungen (Herstellbarkeit)	Geometrische Entwurfsregeln	Geometrische Verifikation
LVS	Layout vs. Schaltplan	Netzlistenextraktion aus dem Layout, regelbasiert	Geometrische Verifikation
PEX (plus Simulation)	Auswirkungen von Parasiten auf das Schaltungsverhalten	Parameterextraktion aus dem Layout, regelbasiert; gefolgt von Simulation	Geometrische und funktionale Verifikation
ERC	Layout vs. elektrische Prozessgrenzen (Zuverlässigkeit)	Extraktion der Konnektivität aus dem Layout, regelbasiert	Geometrische Verifikation
Testen	Eignung hinsichtlich Einsatzzweck	Reales Experiment, Kundenprüfung	Validierung

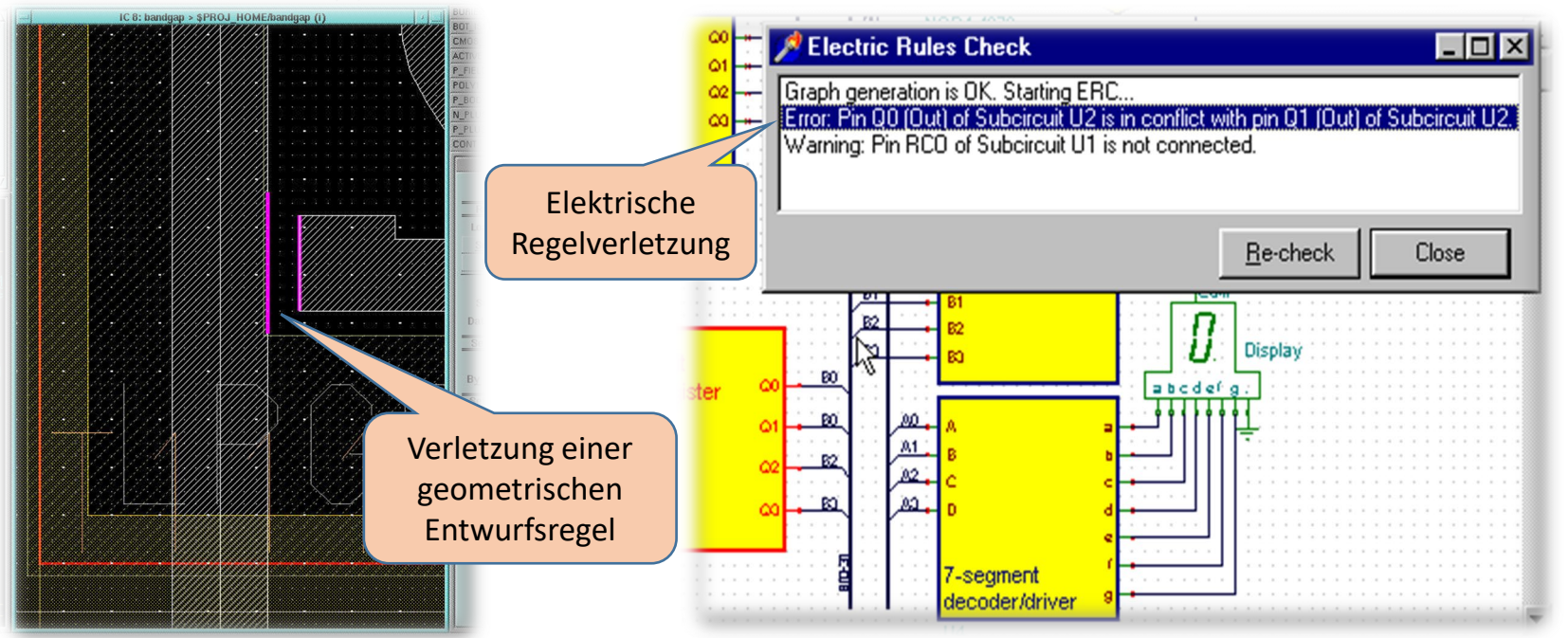


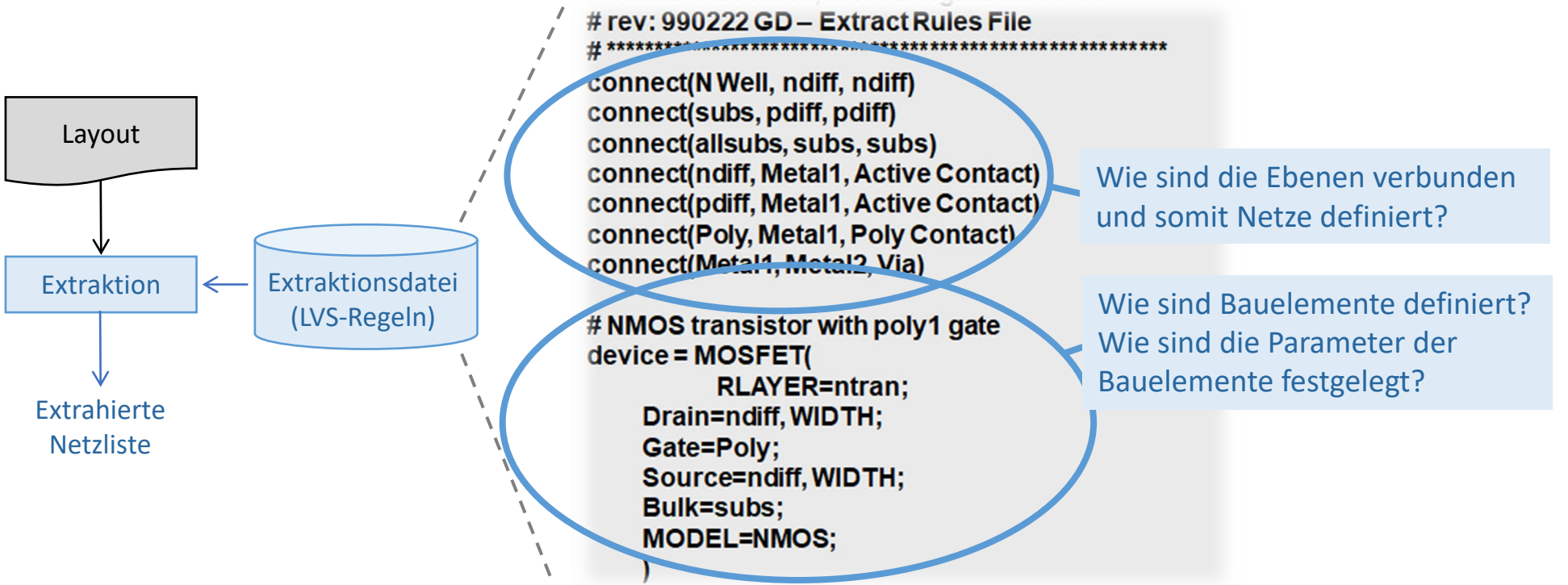


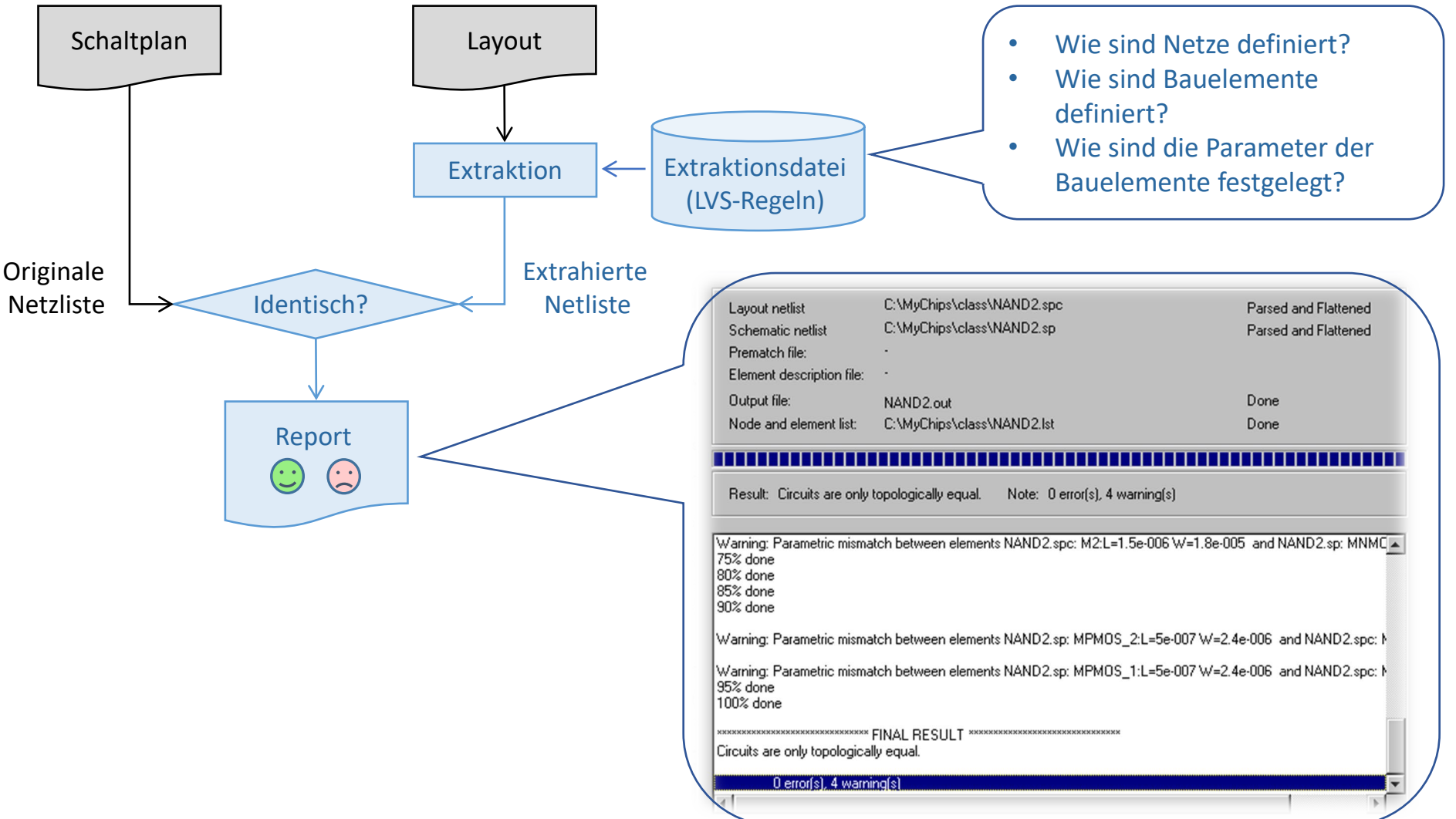


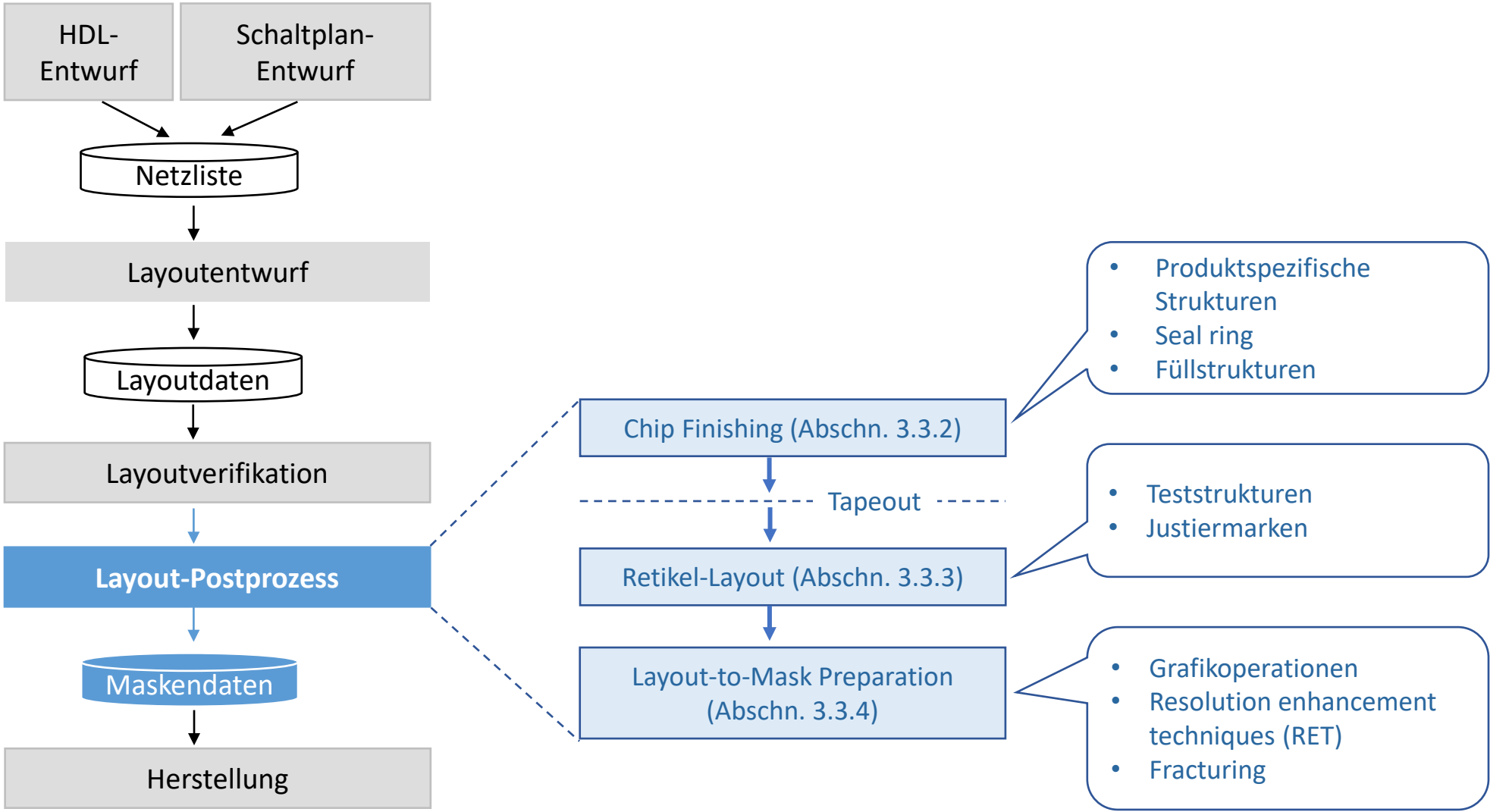


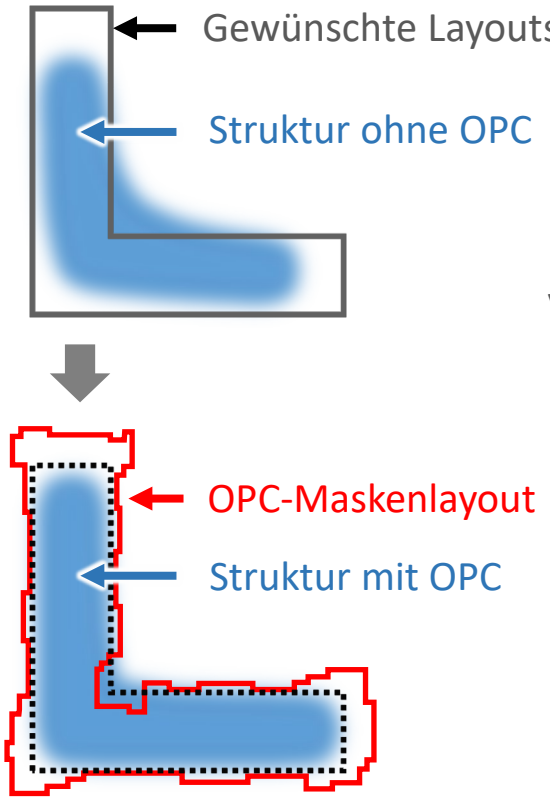




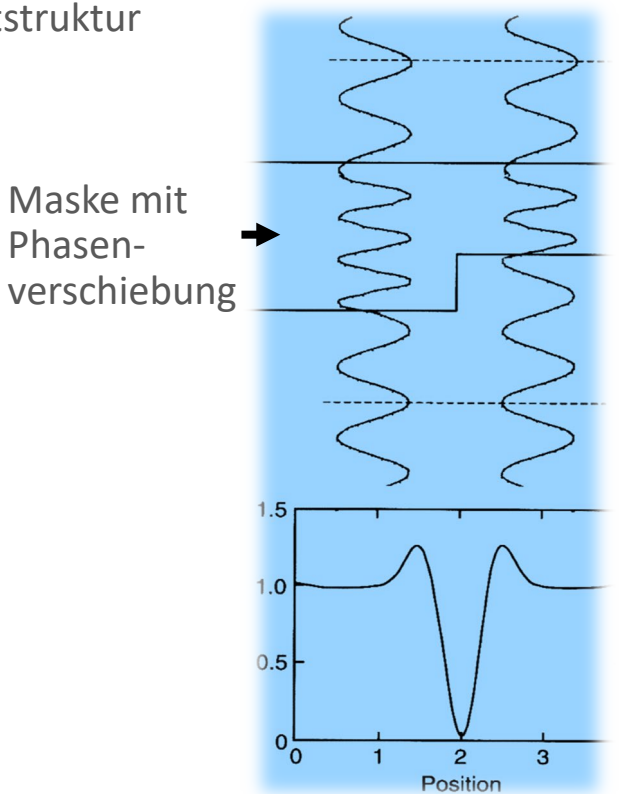




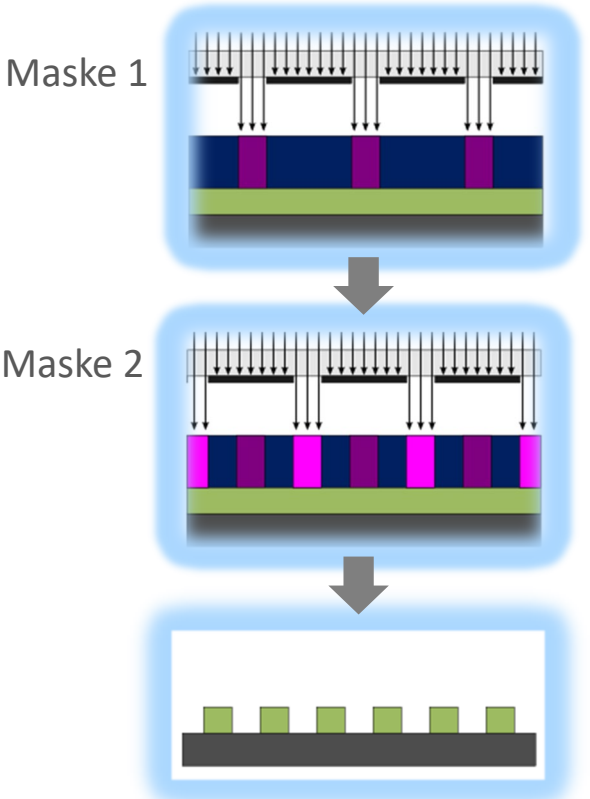




Optical Proximity Correction (OPC)
Nahbereichskorrektur



Phase Shift Mask
Phasenverschiebungsmaske



Double Patterning
Doppelstrukturierung