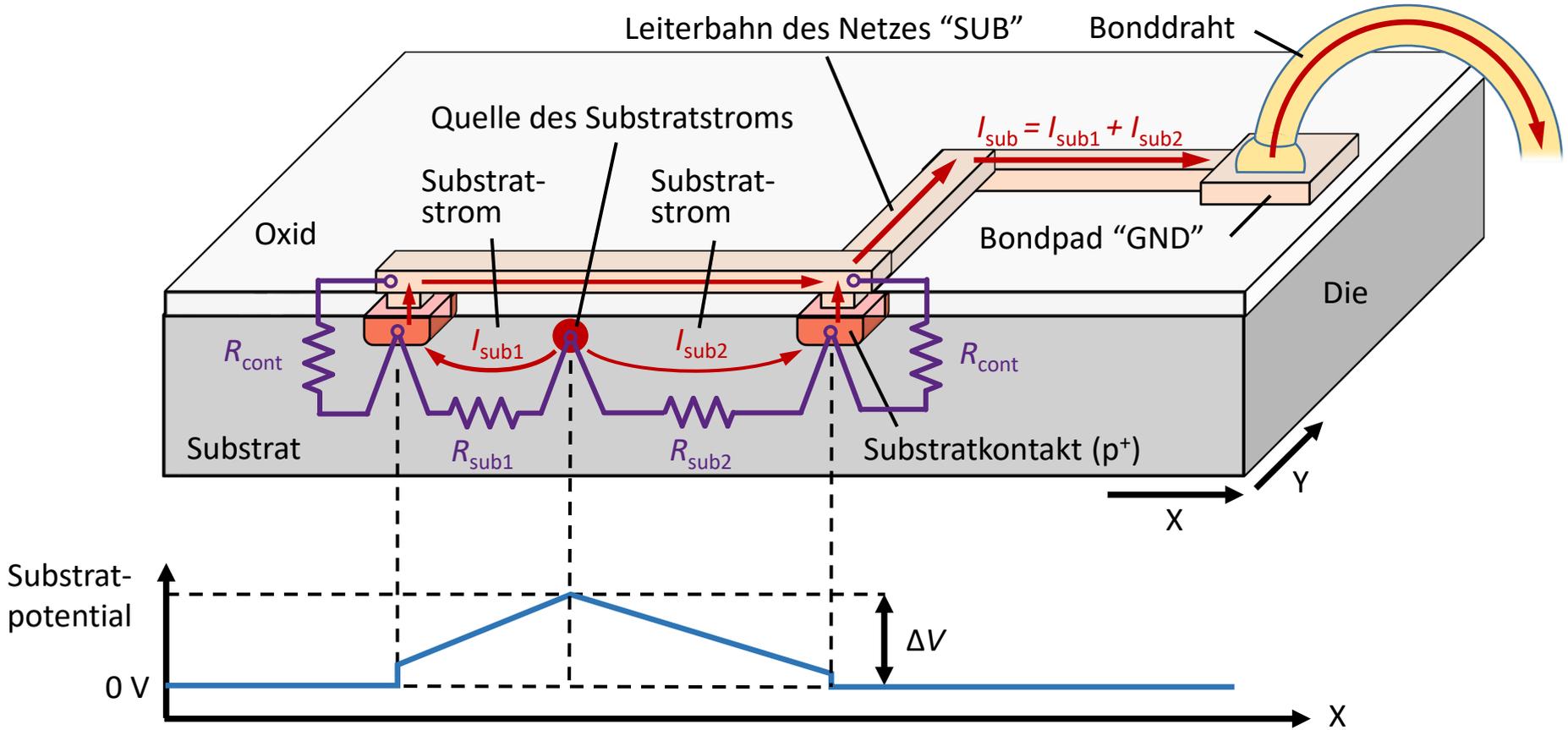
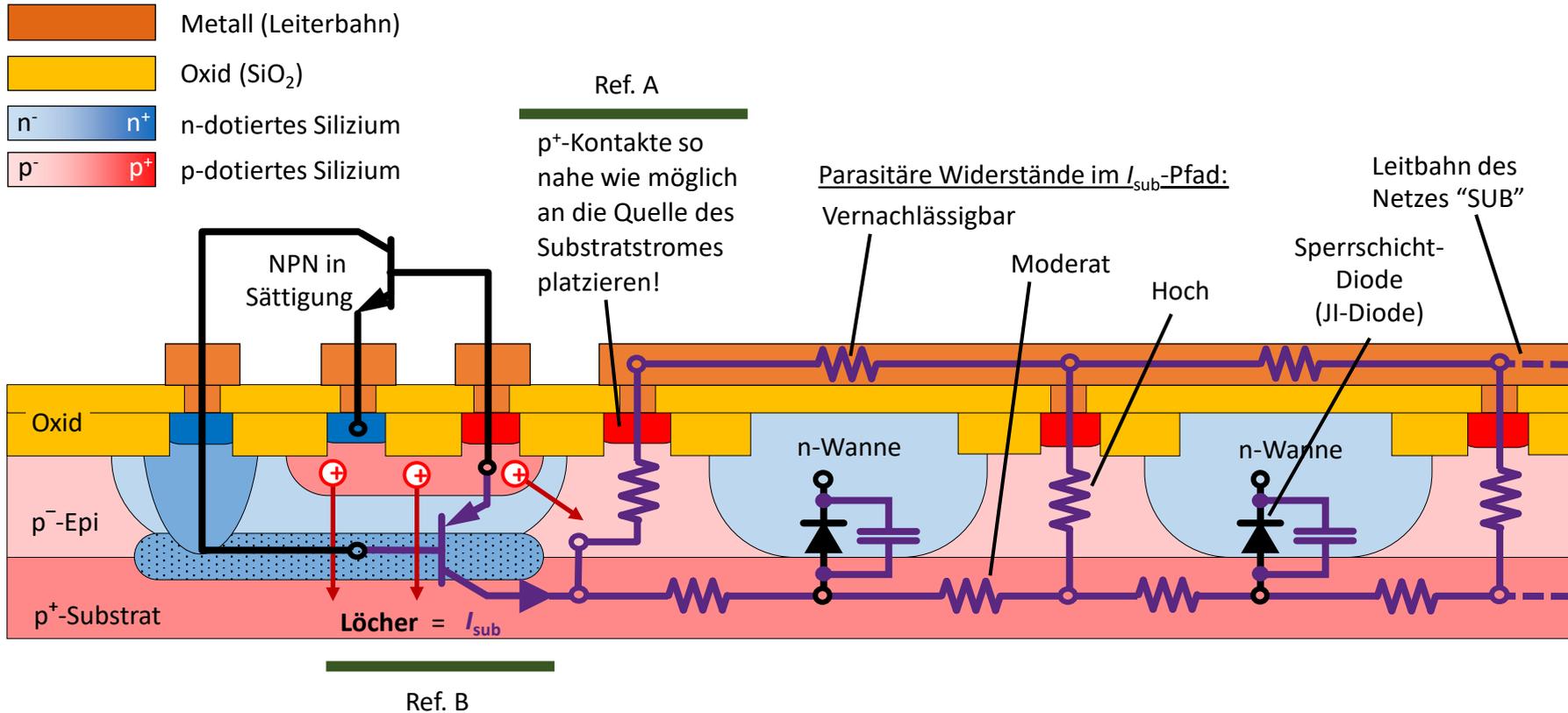
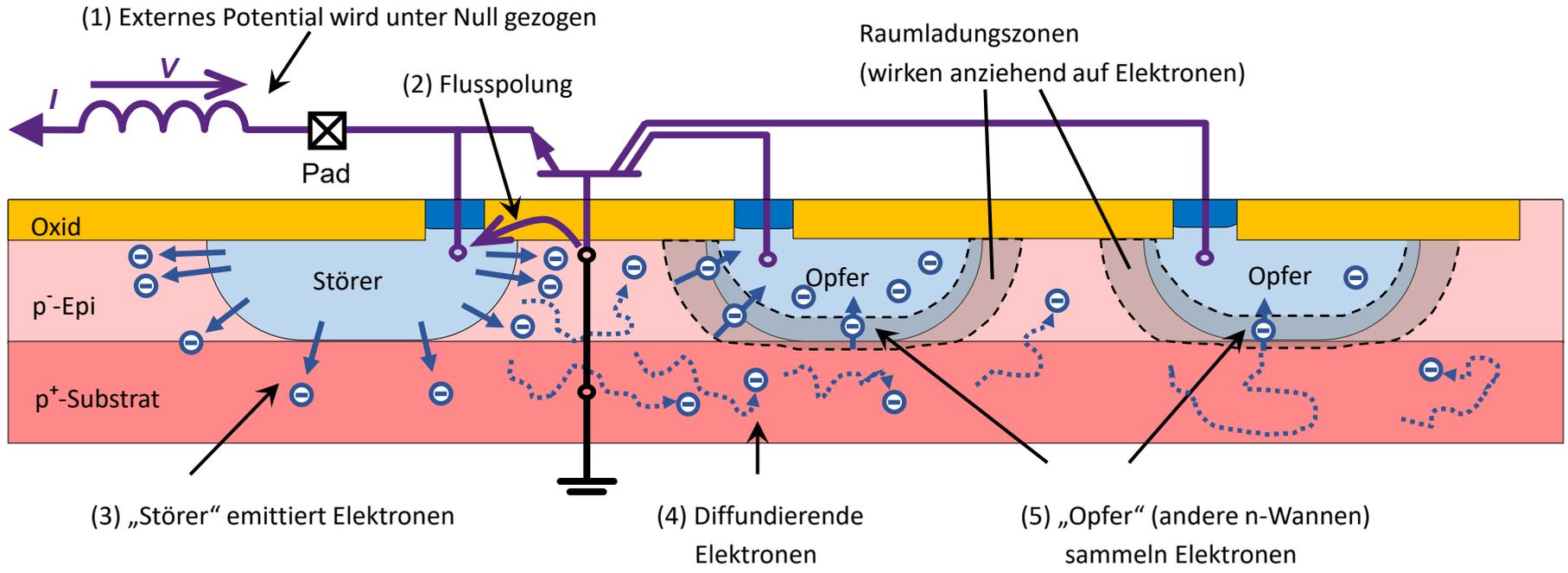


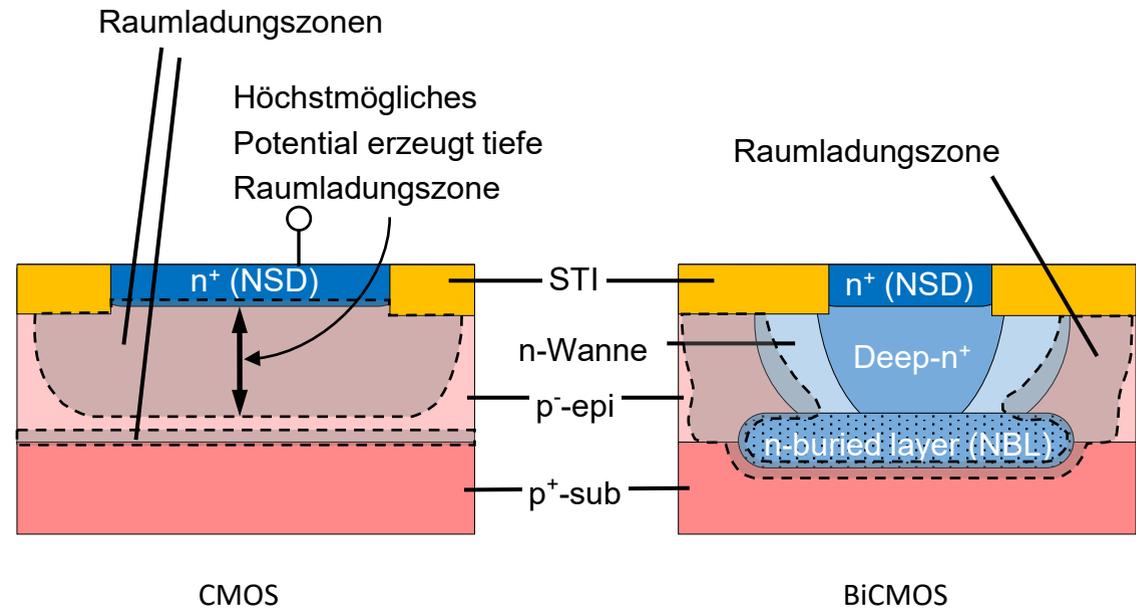
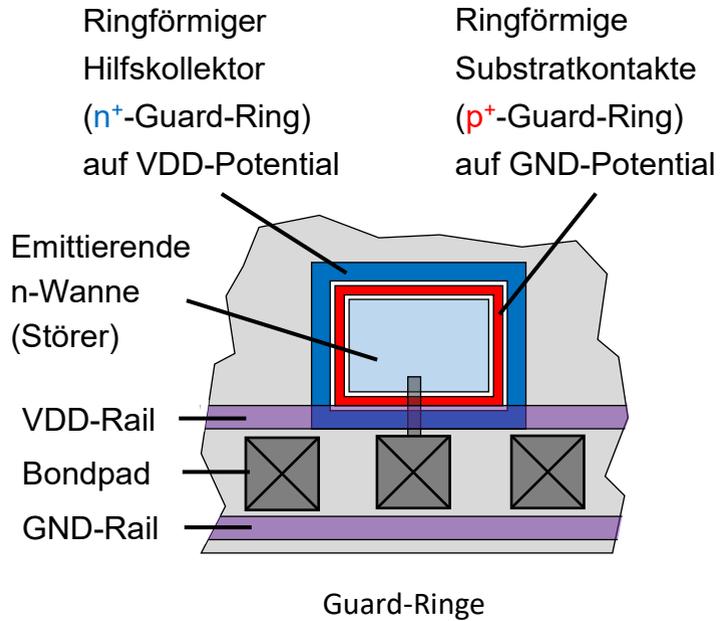
- 7.1 Parasitäre Effekte im Silizium
- 7.2 Oberflächeneffekte
- 7.3 Parasitäre Effekte in der Metallisierung
- 7.4 Schadensmechanismen durch Überspannungen
- 7.5 Migrationseffekte in der Metallisierung



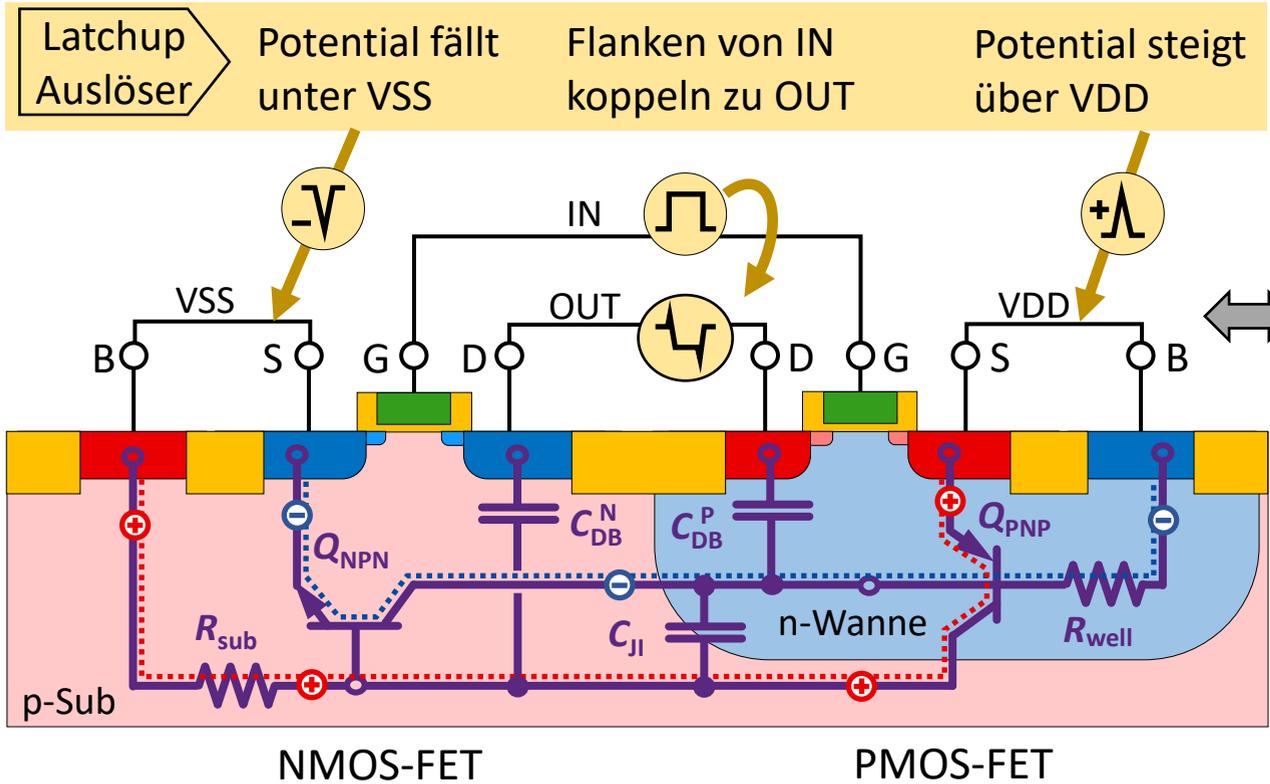




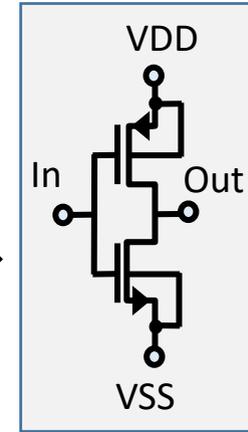




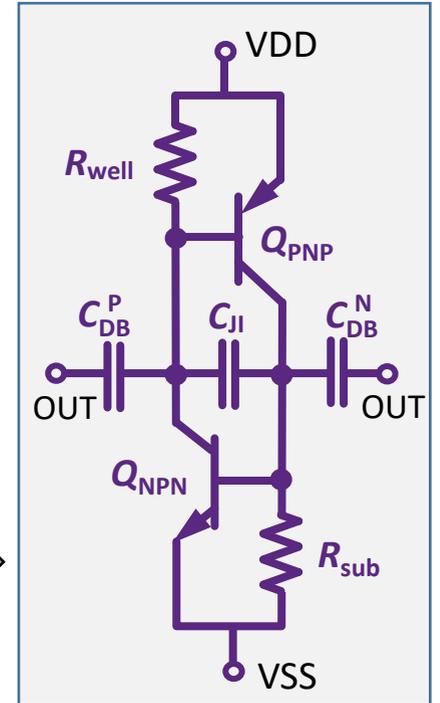
- Poly (Gate)
- Oxid
- n^- n^+ n-dotiertes Silizium
- p^- p^+ p-dotiertes Silizium

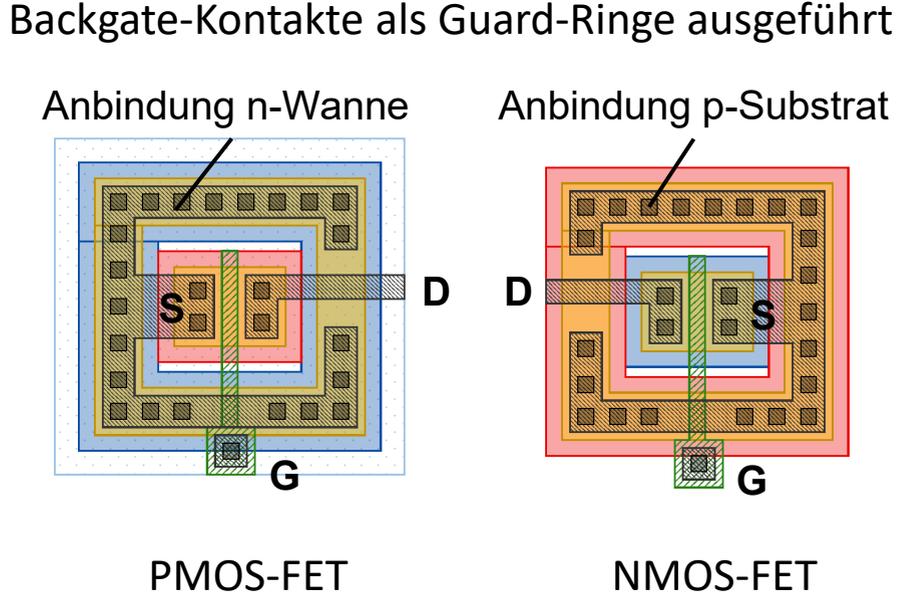
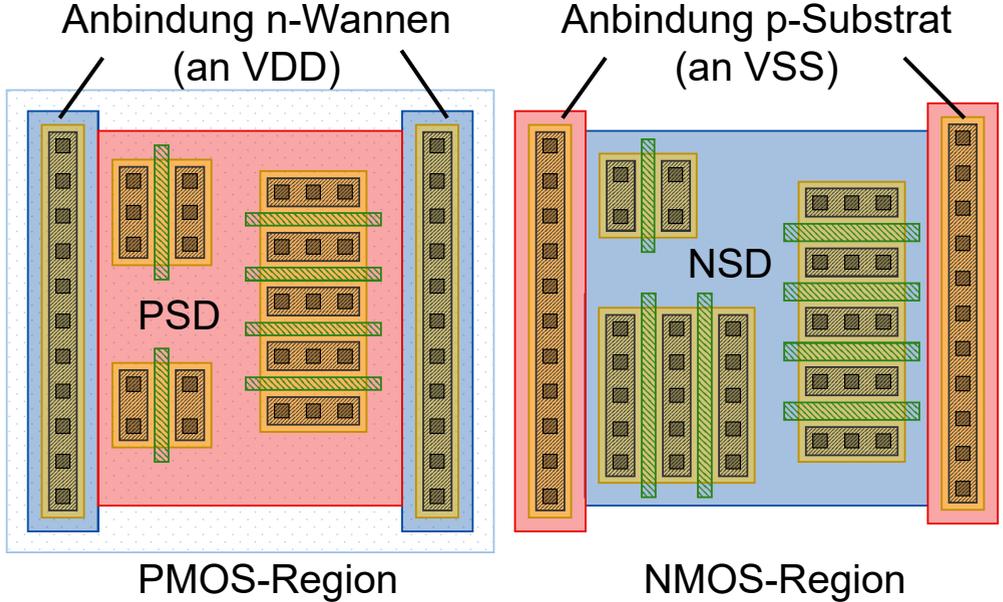
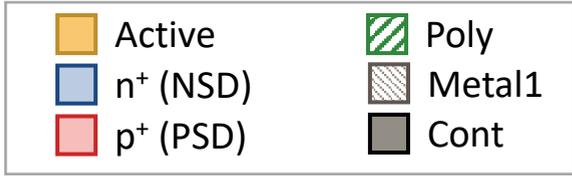


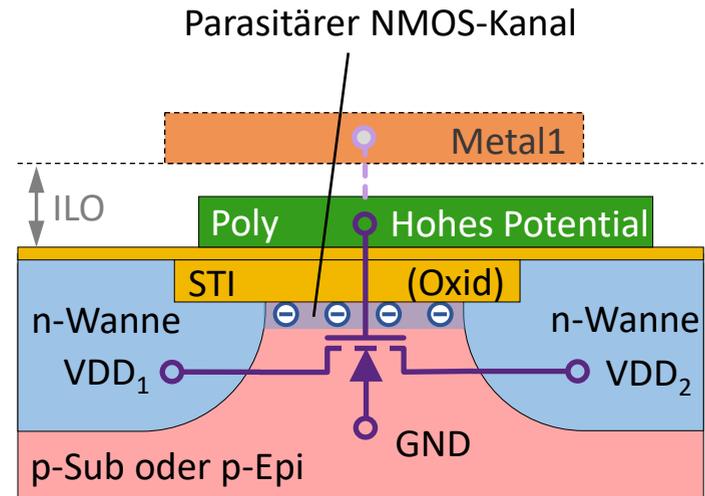
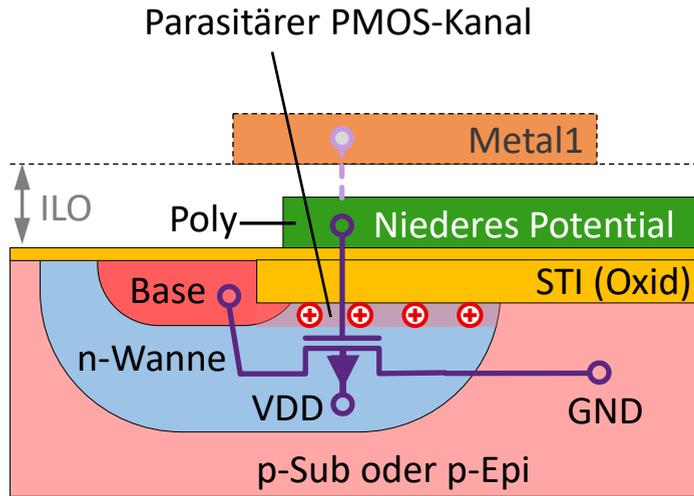
Beabsichtigte Schaltung

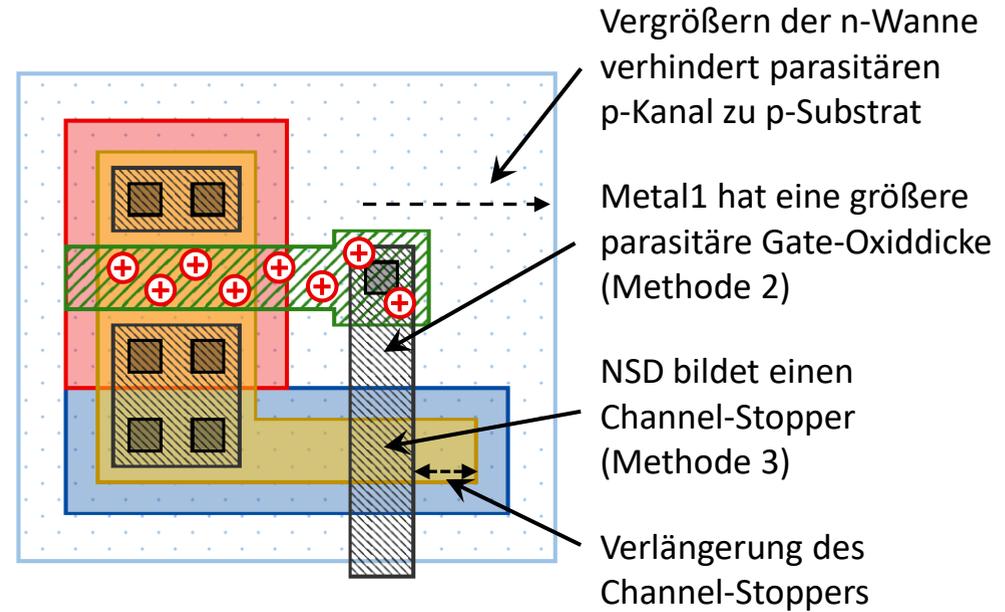
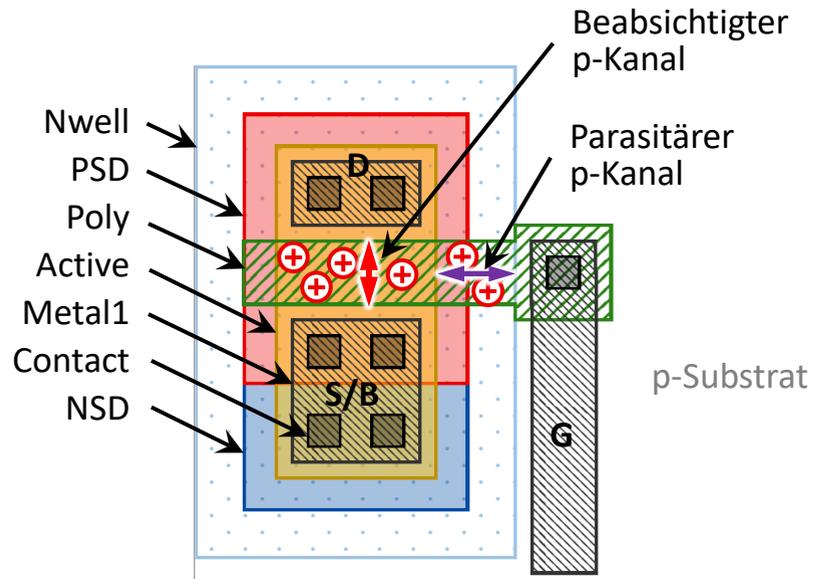


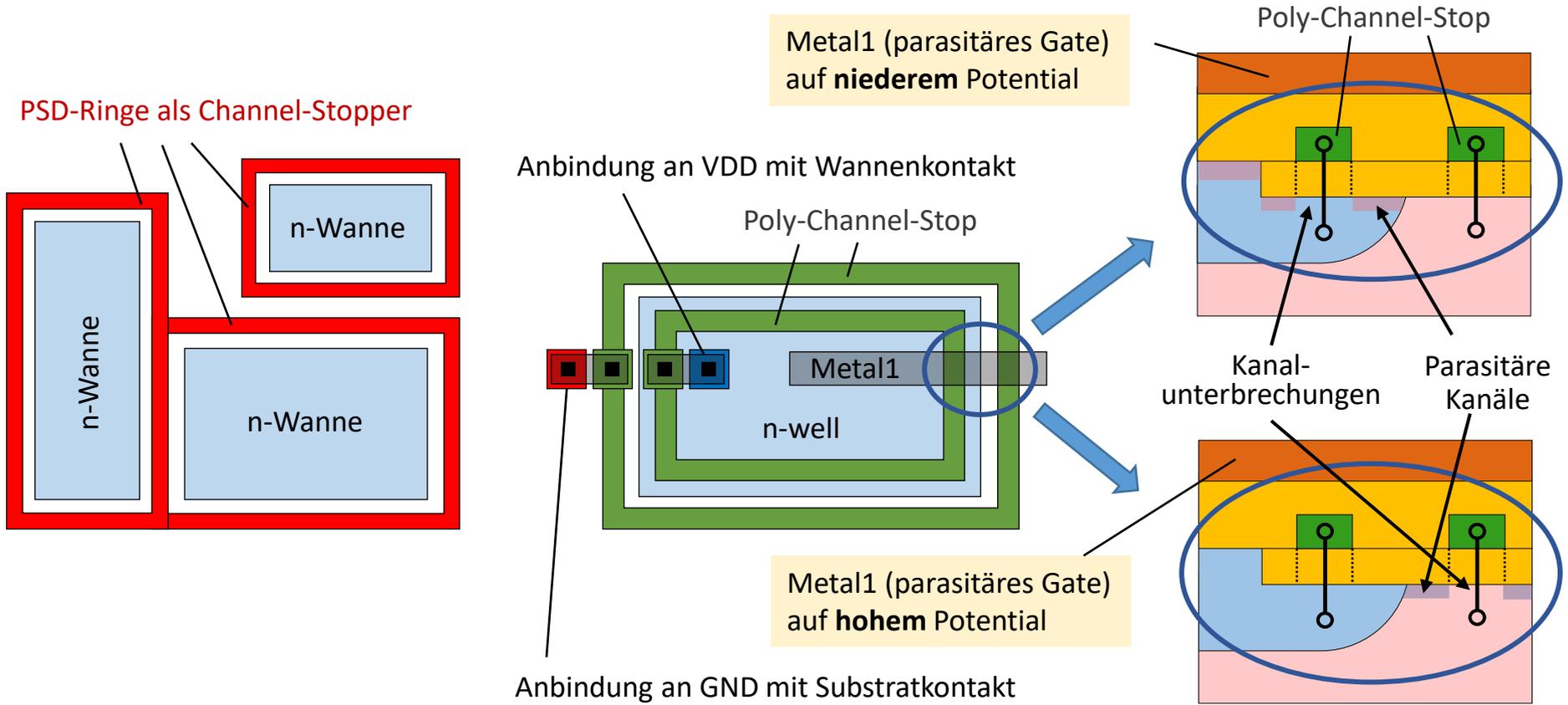
Parasitäre Schaltung

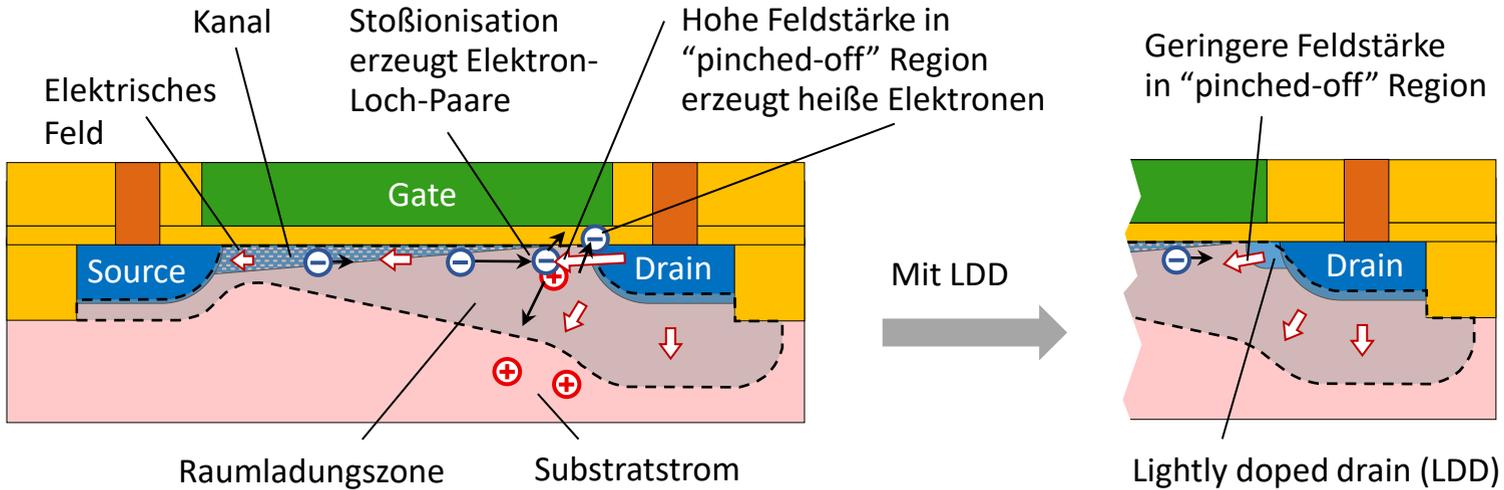


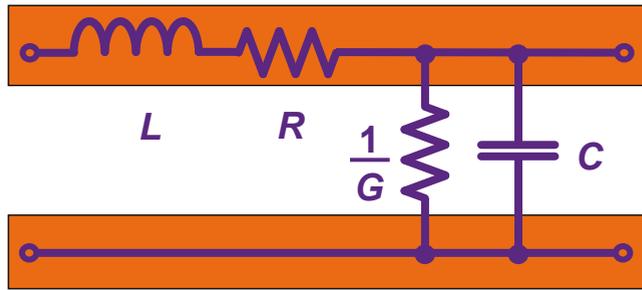




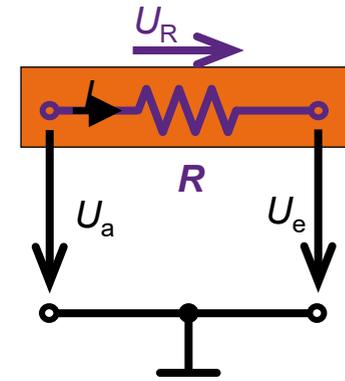
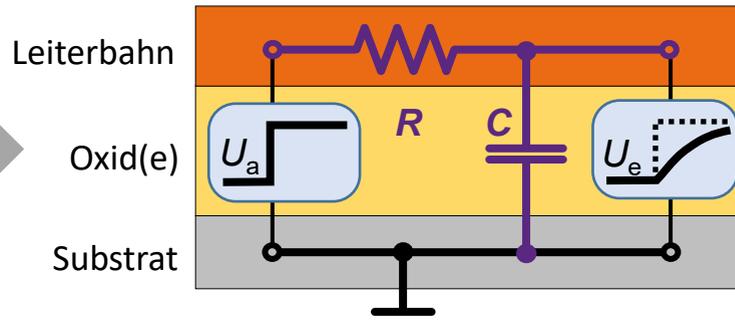


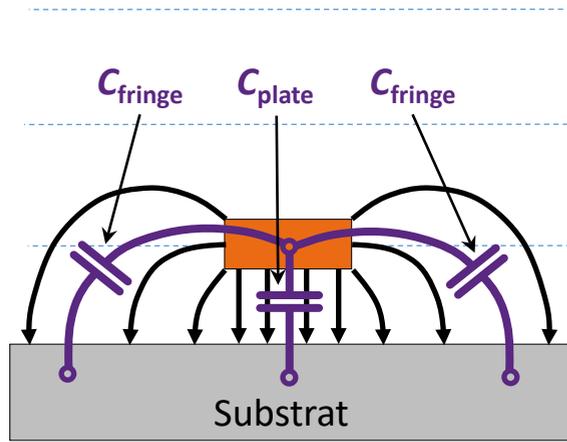




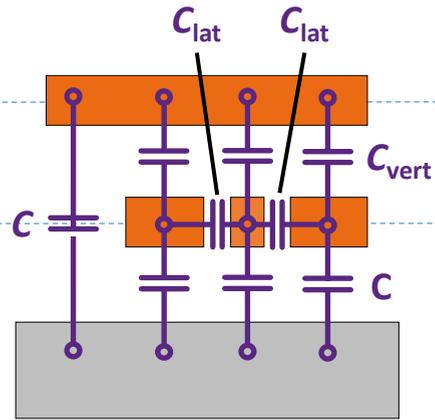


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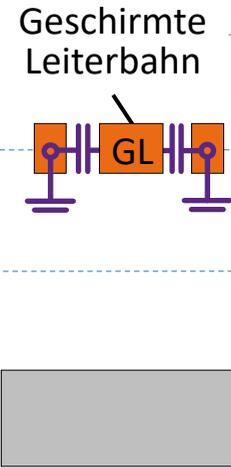




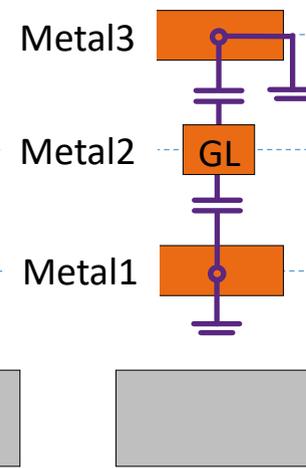
(a)



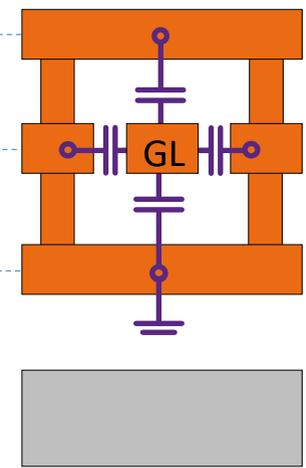
(b)



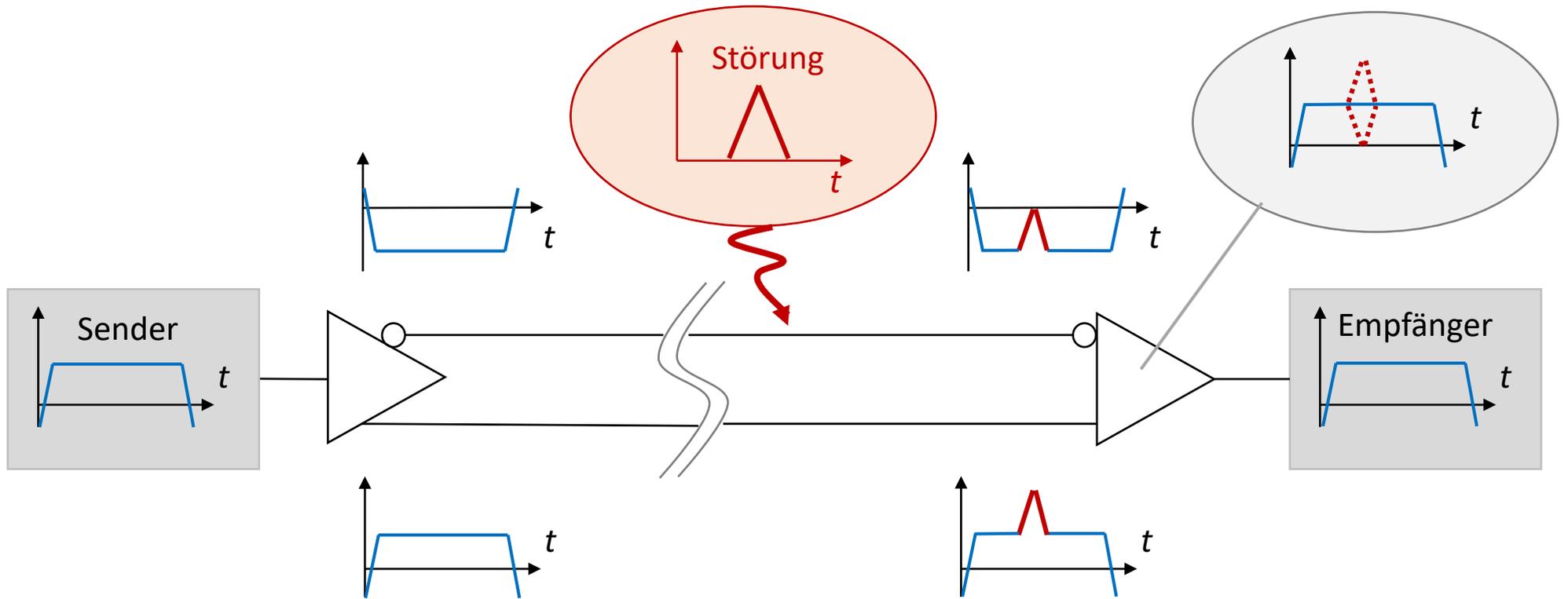
(c)

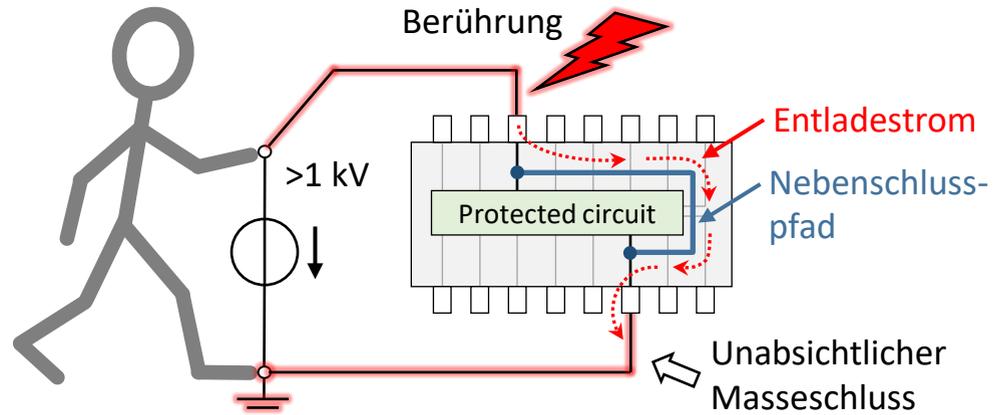
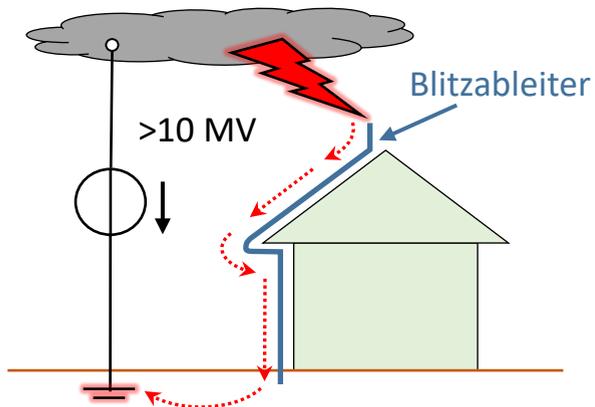


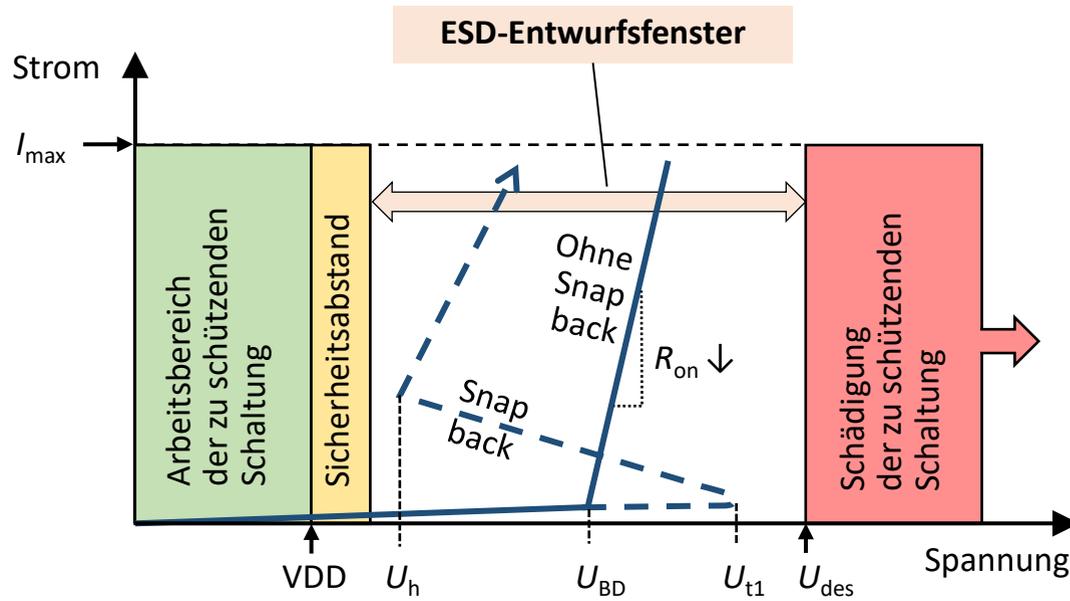
(d)



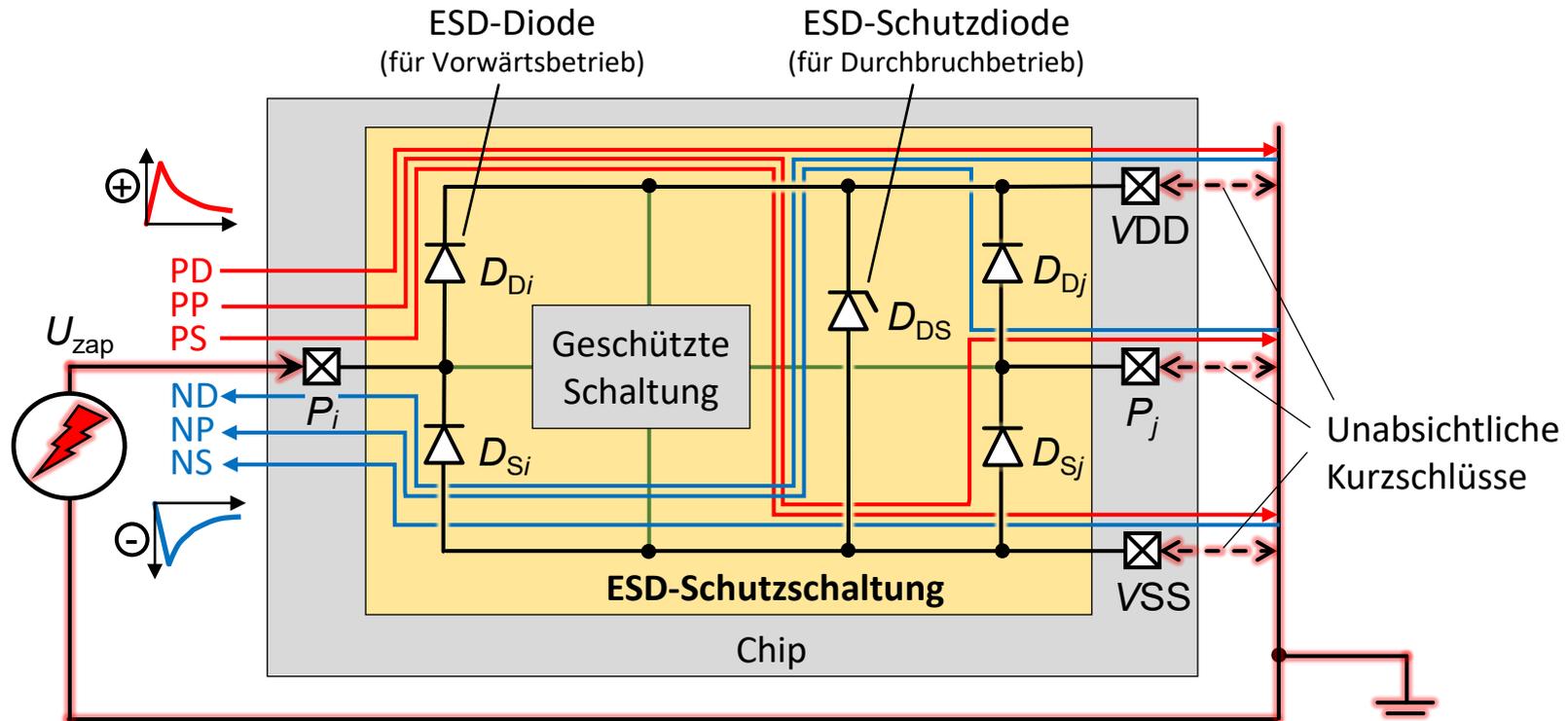
(e)

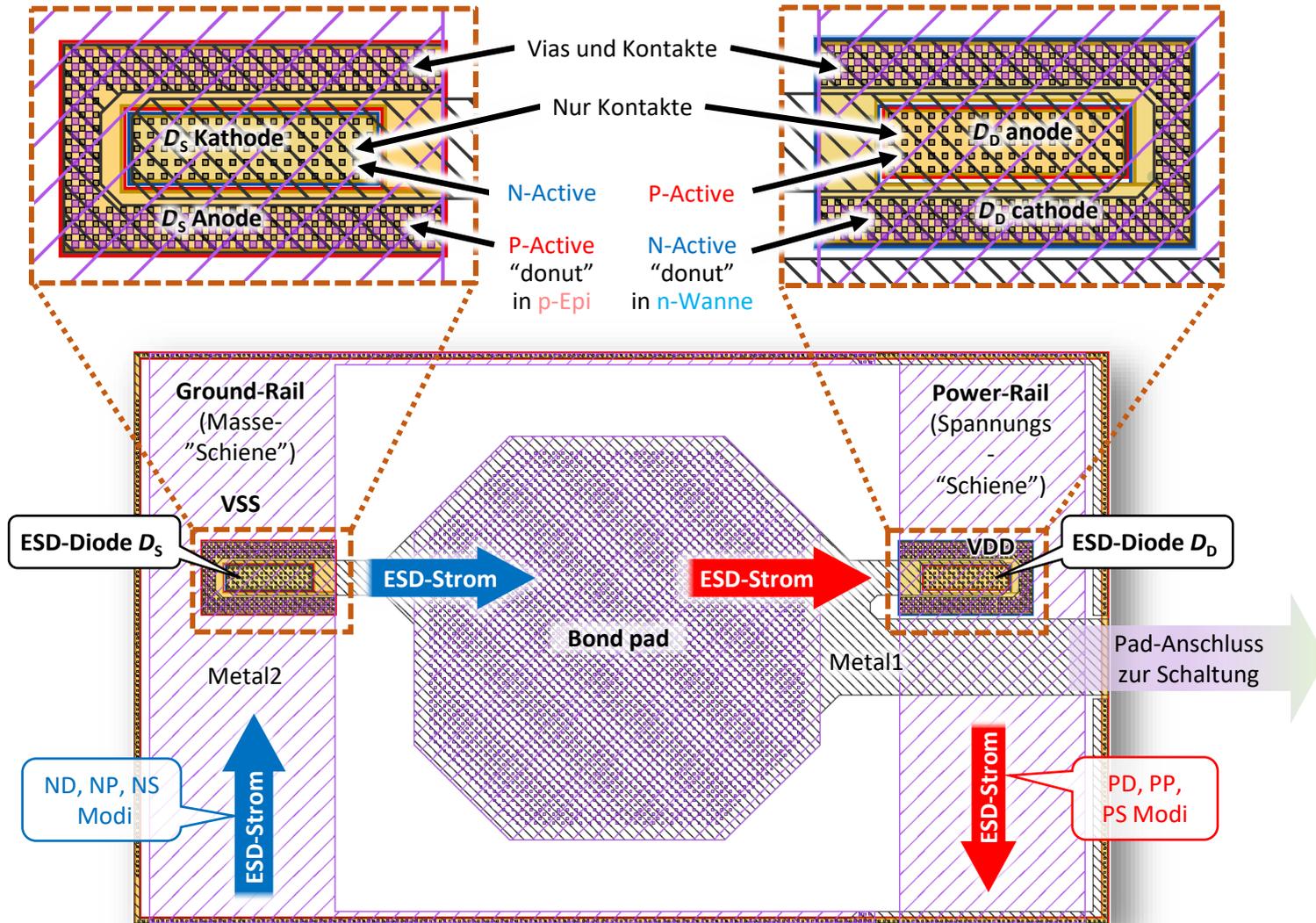


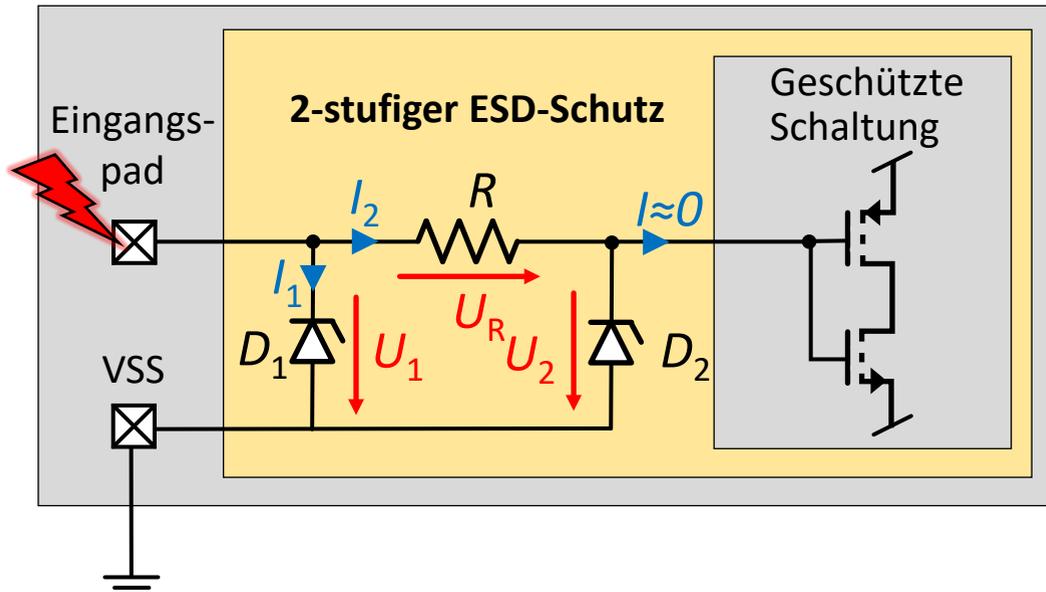




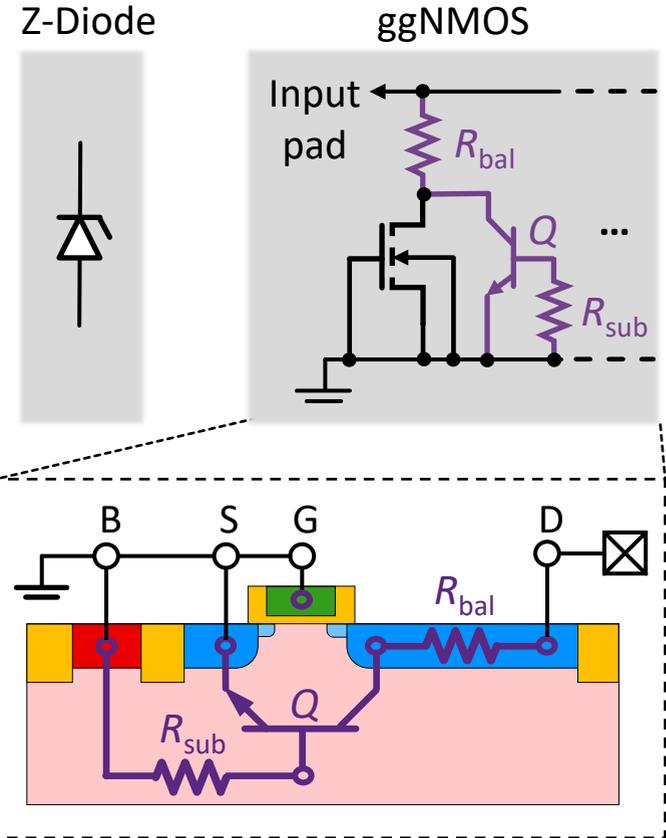
- U_h Haltespannung
- U_{BD} Durchbruchspannung
- U_{t1} Triggerspannung
- U_{des} Zerstörspannung

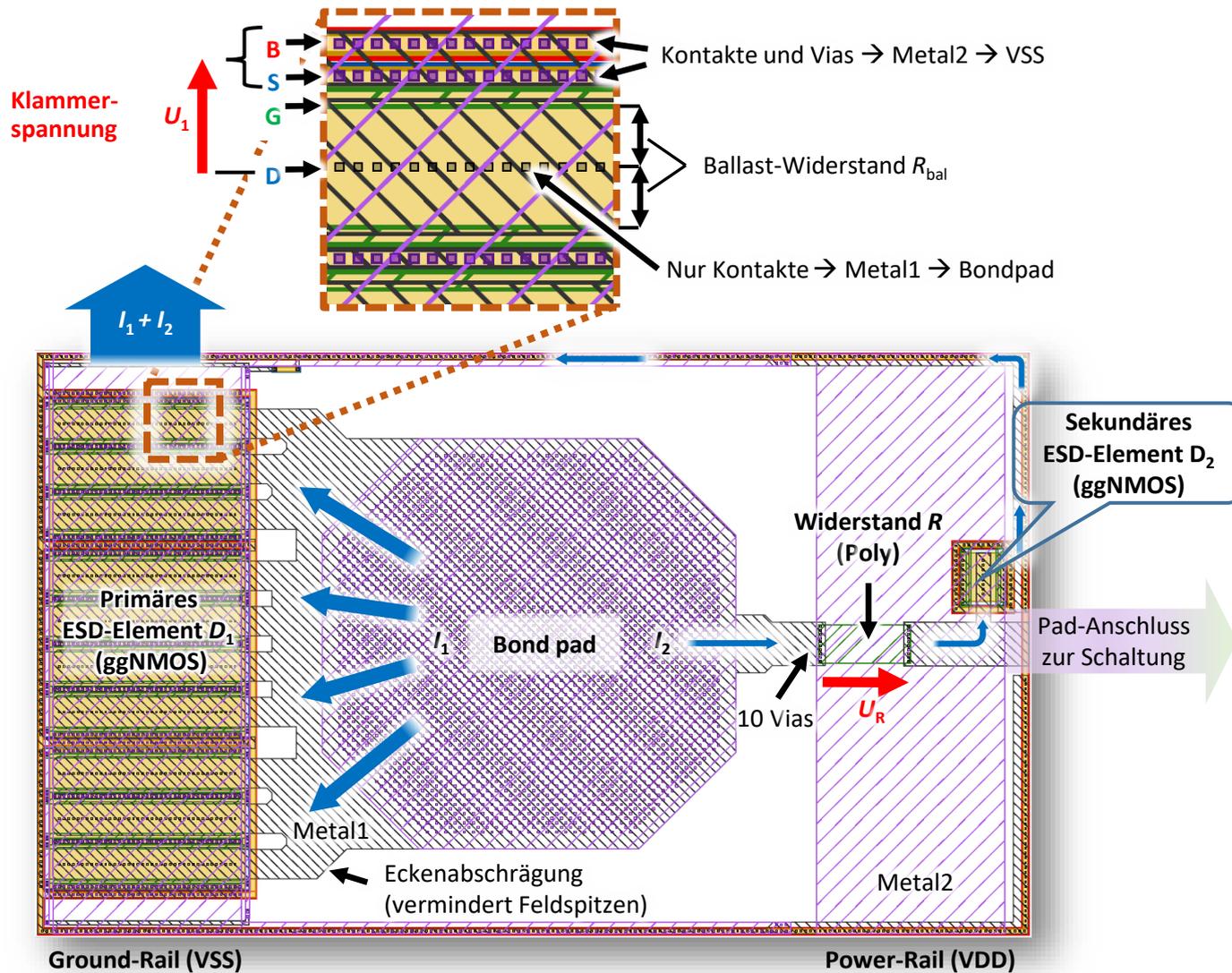


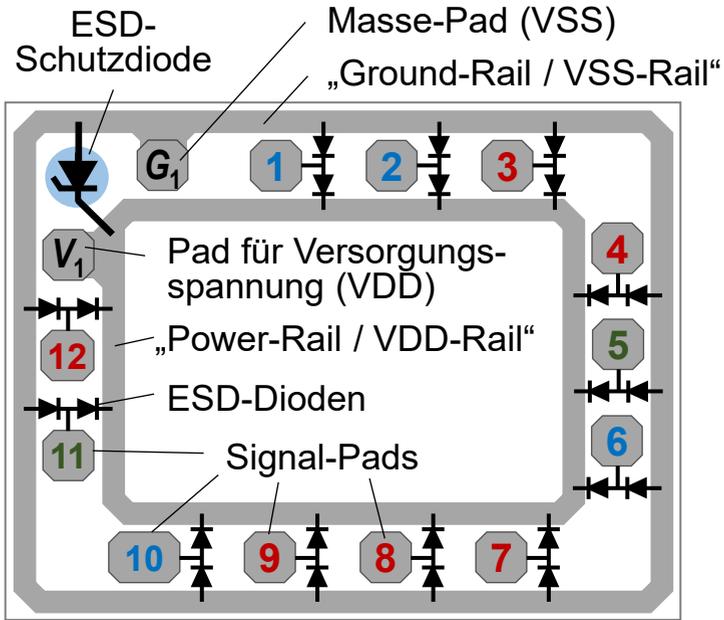




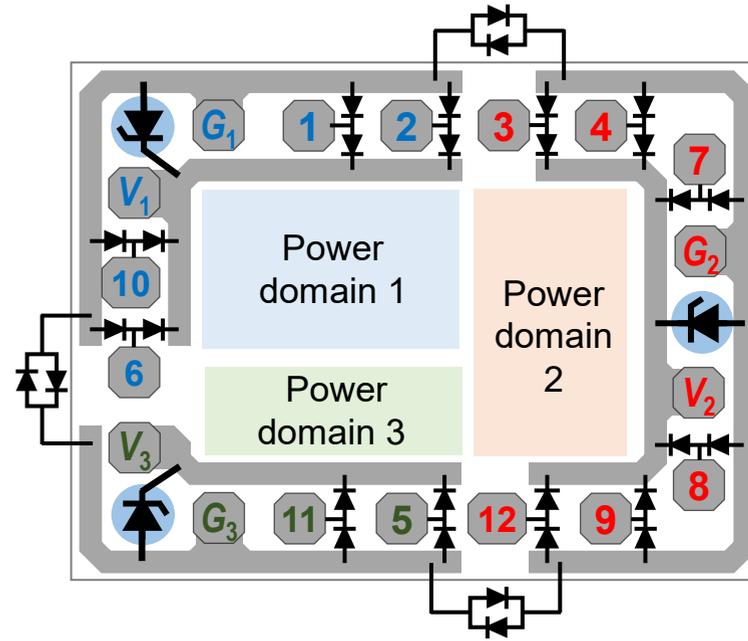
Optionen für die ESD-Elemente D_1 , D_2 :



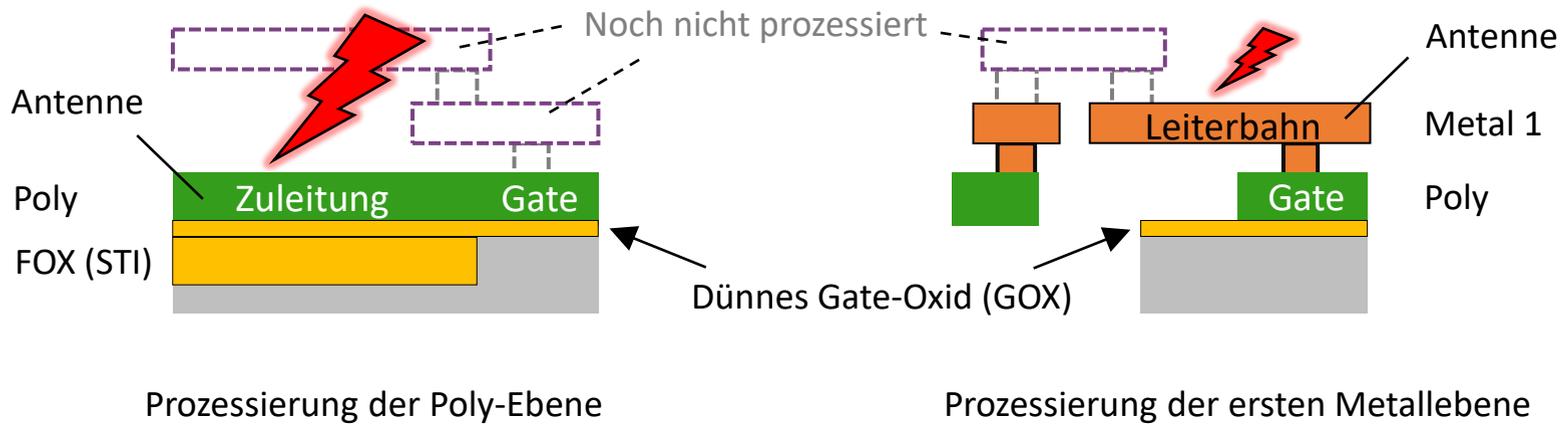




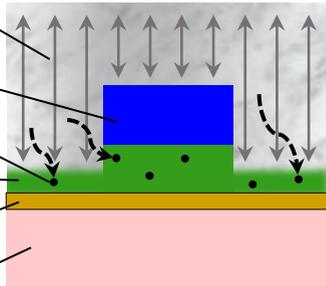
Single-Power-Domain



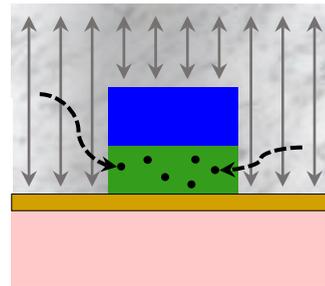
Multi-Power-Domains



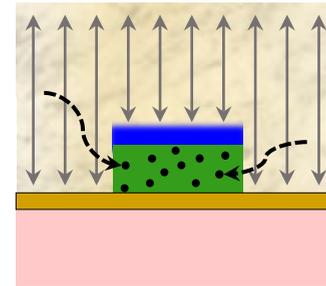
RIE Plasma
 Fotolack
 Ladungen
 Polysilizium
 Gate-Oxid
 p-Substrat



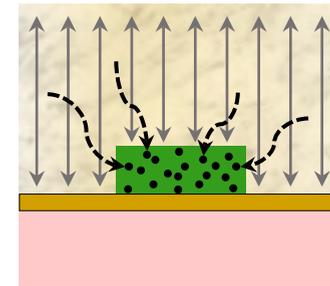
(1) Poly ätzen



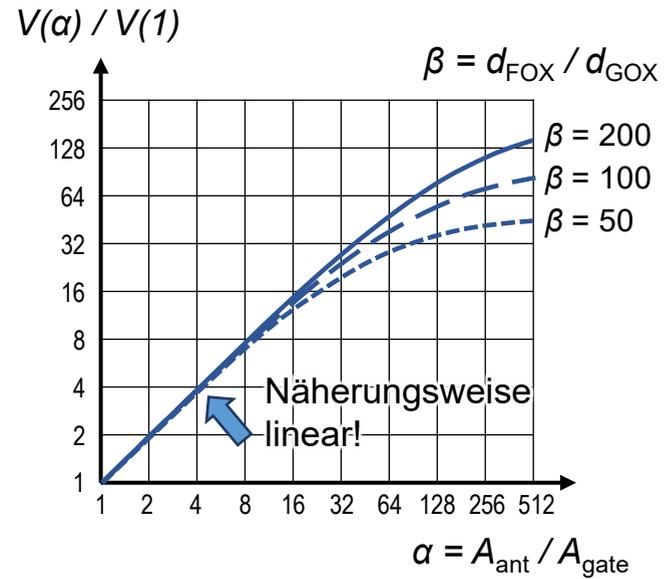
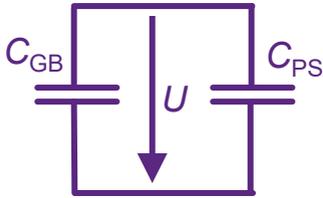
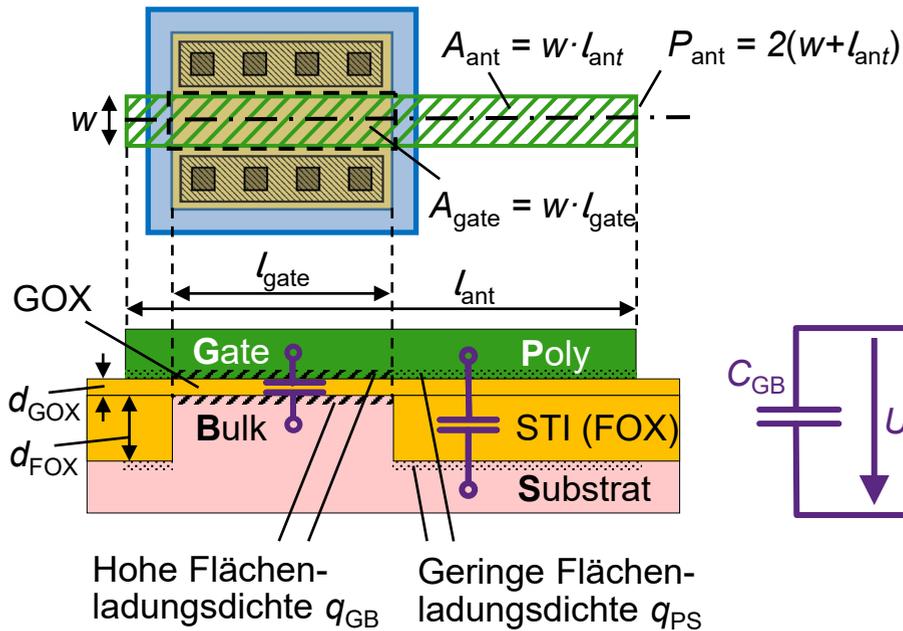
(2) Poly ätzen

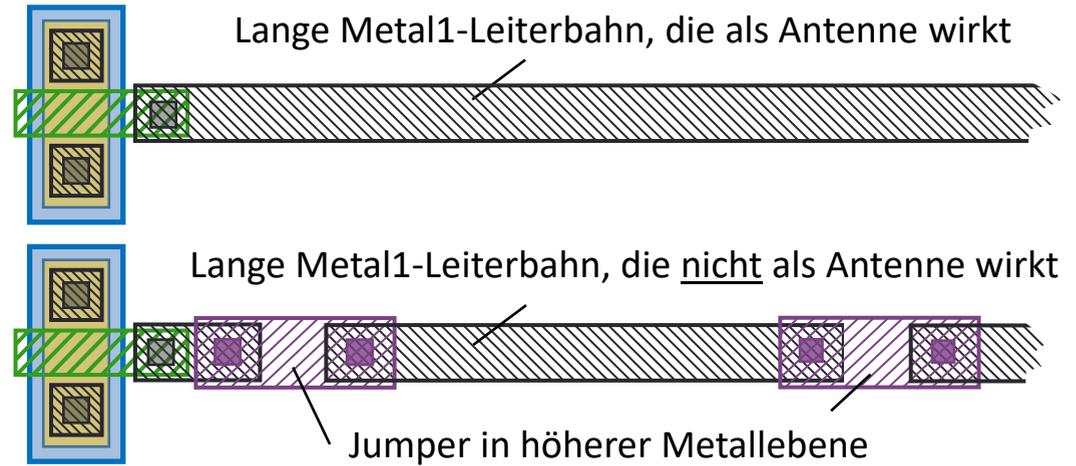
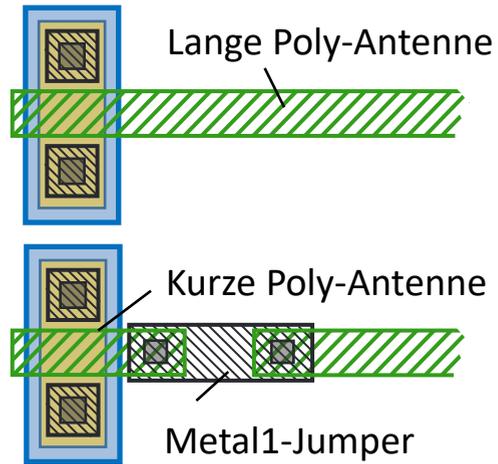


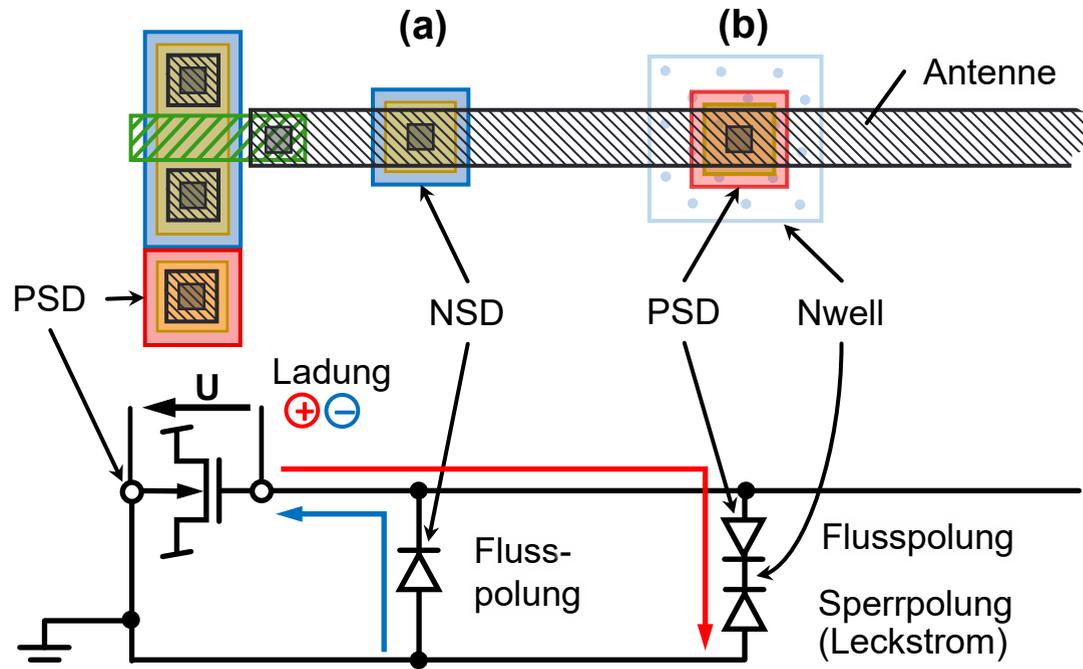
(3) Fotolack
veraschen



(4) Fotolack
veraschen

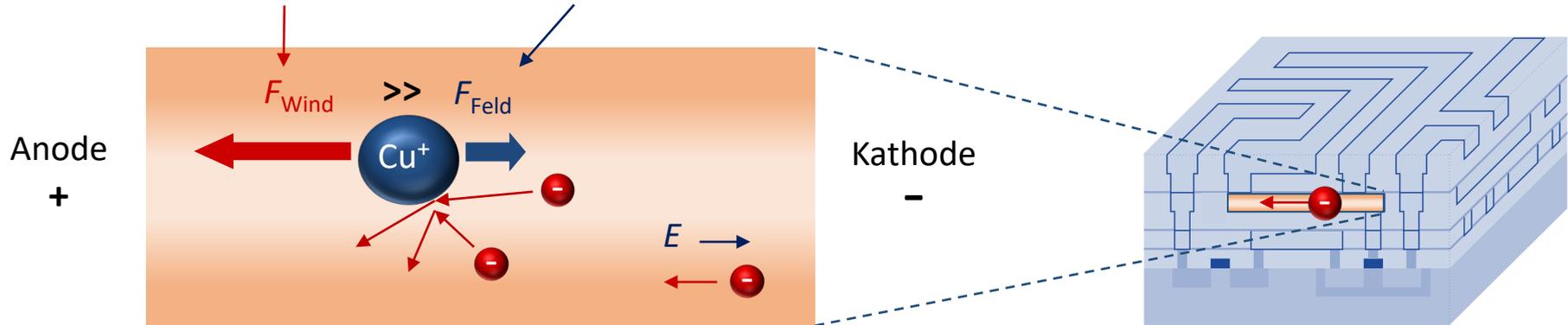




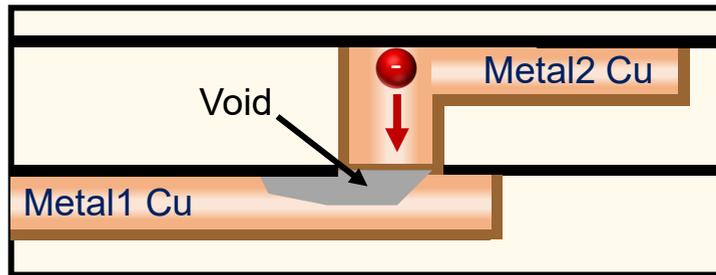


Kraft, welche die Leitungselektronen durch Impulsübertragung auf die Metallionen (Cu^+) ausüben

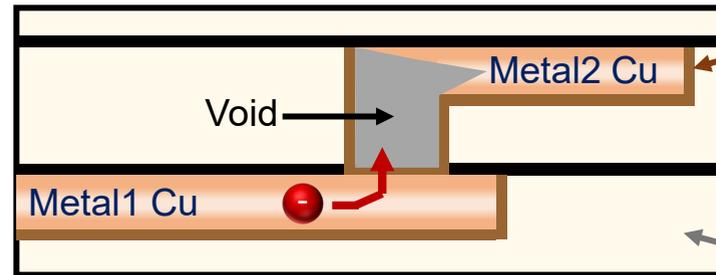
Wechselwirkung des elektrischen Feldes mit den Metallionen



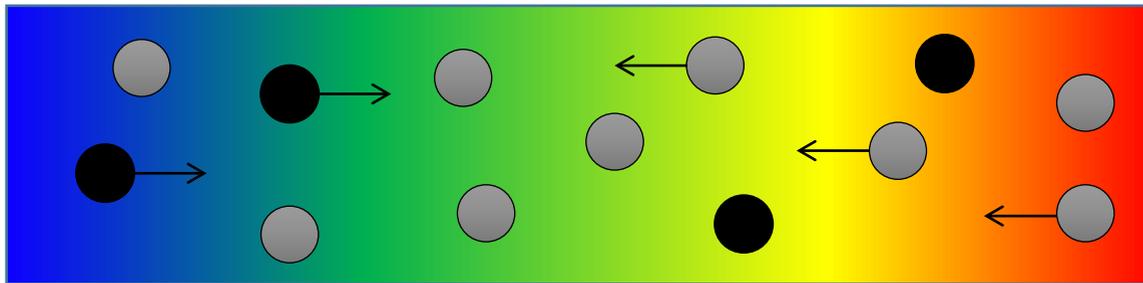
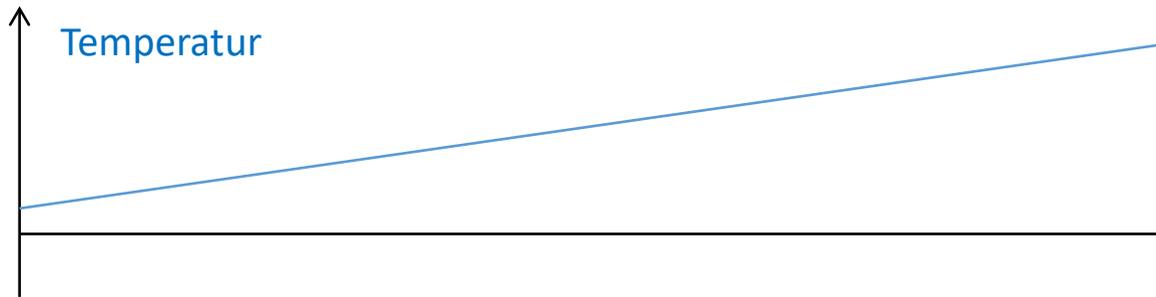
Leitungsverarmung (Line depletion)



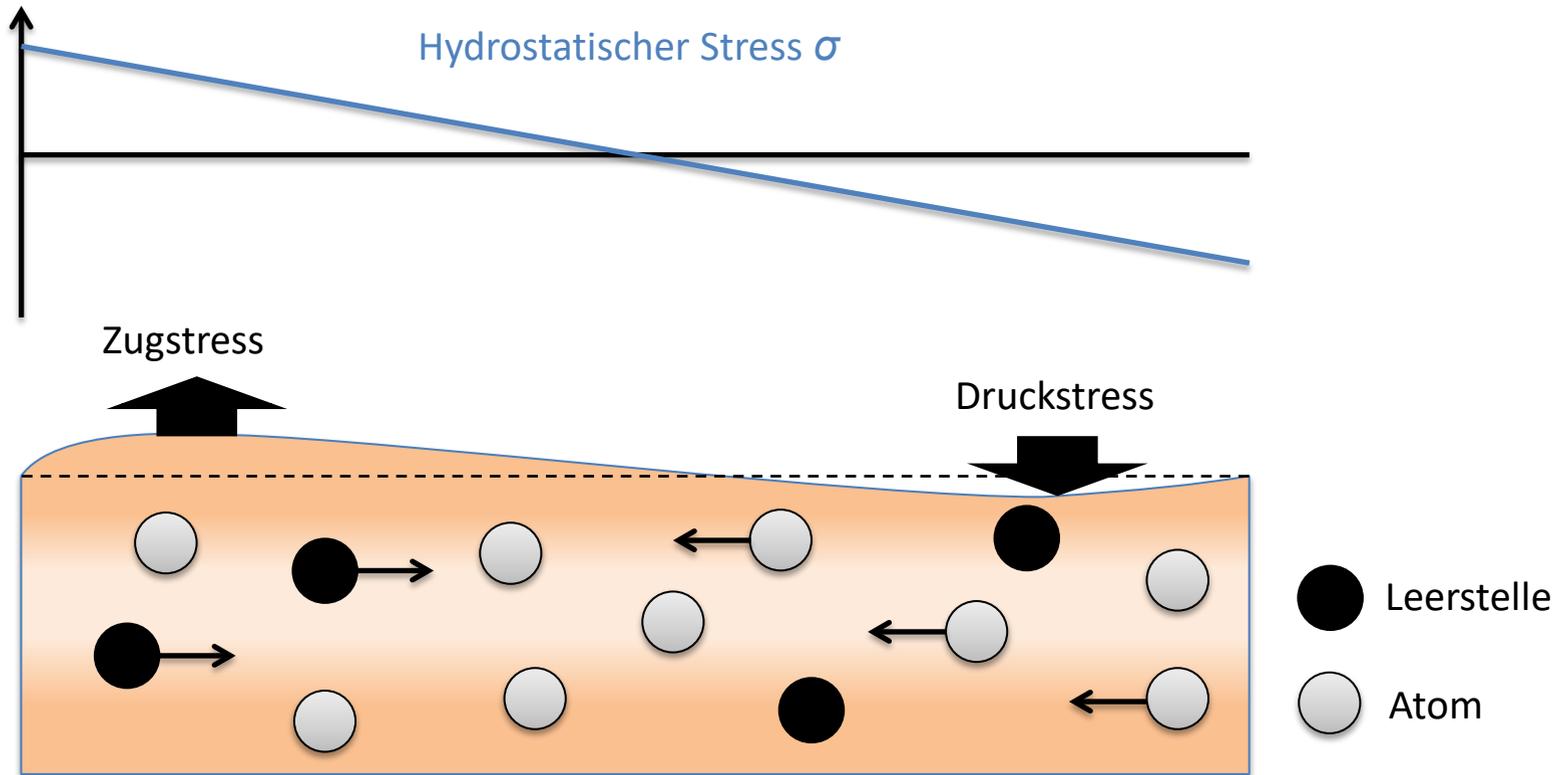
Viaverarmung (Via depletion, via voiding)

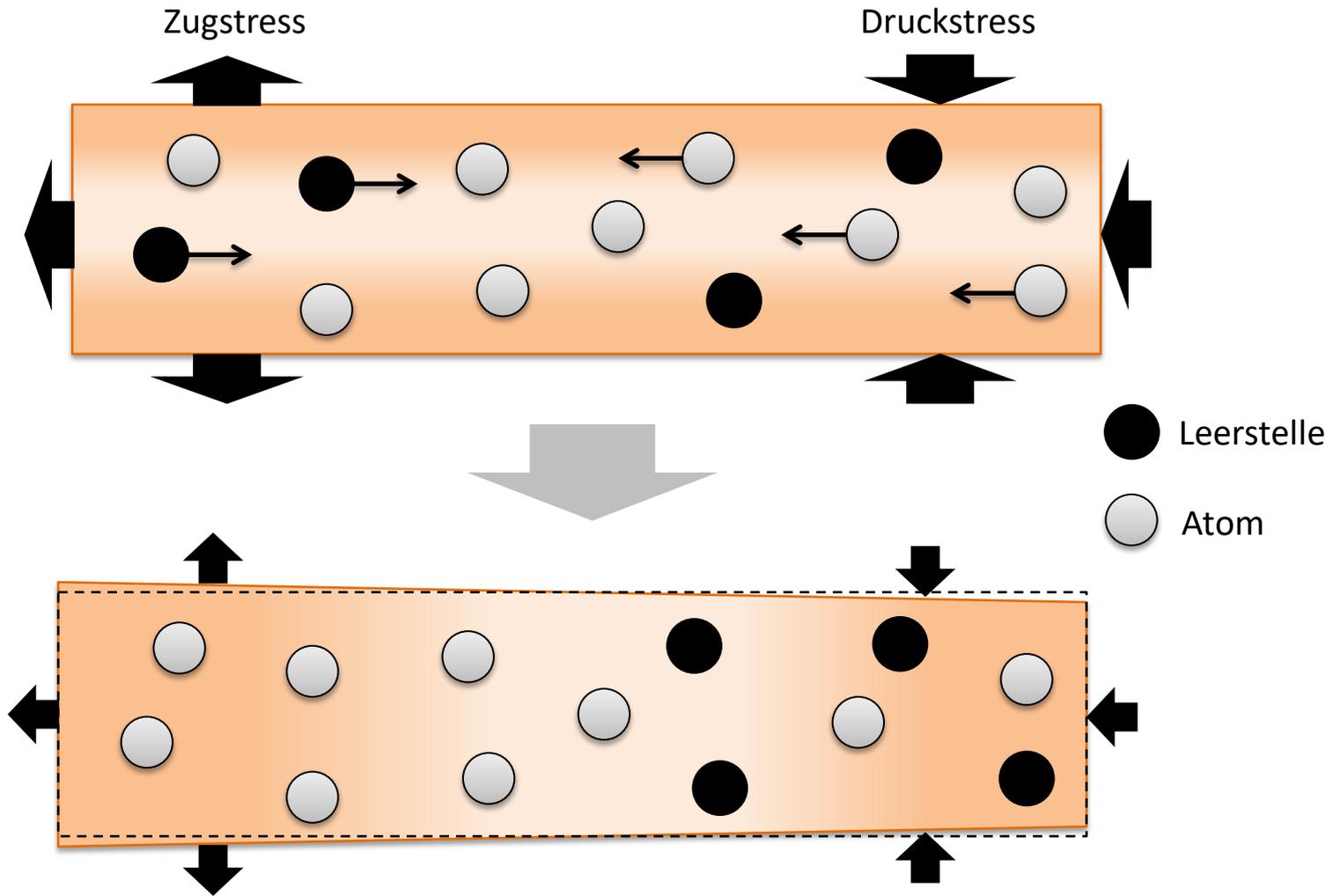


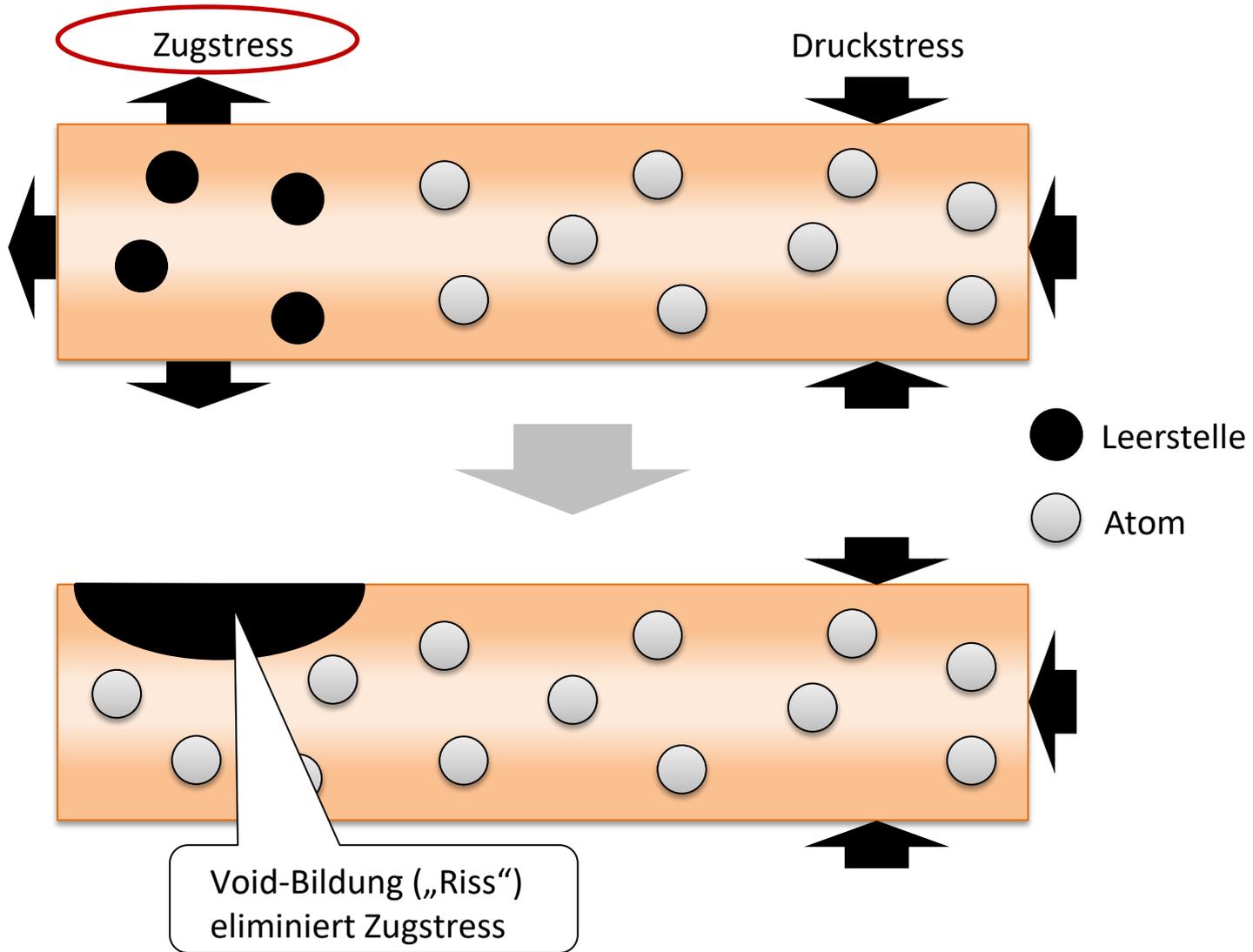
- Ta/TaN Barrierschicht (Metal liner)
- SiN, NSiC Capping-Schicht
- Low-k-Dielektrikum

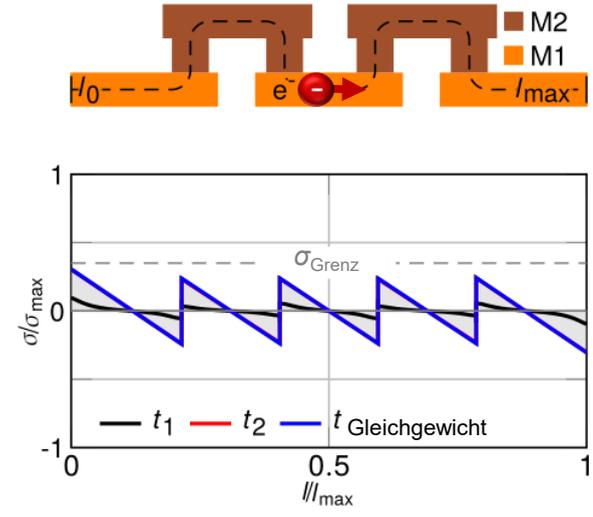
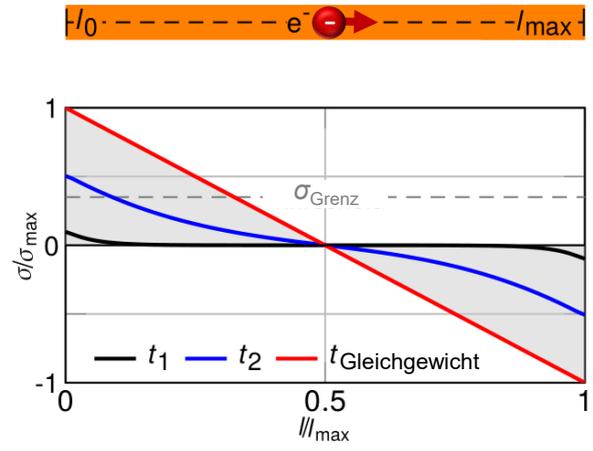


- Leerstelle
- Atom

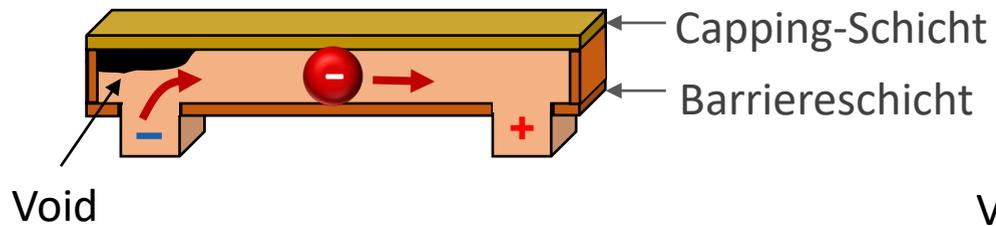




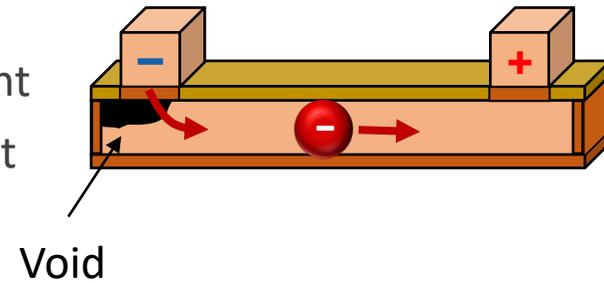




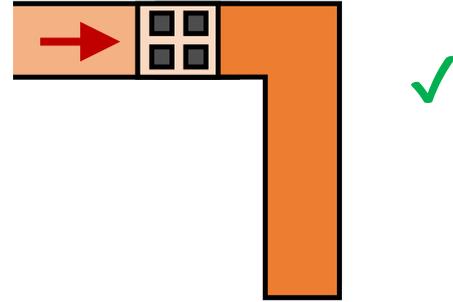
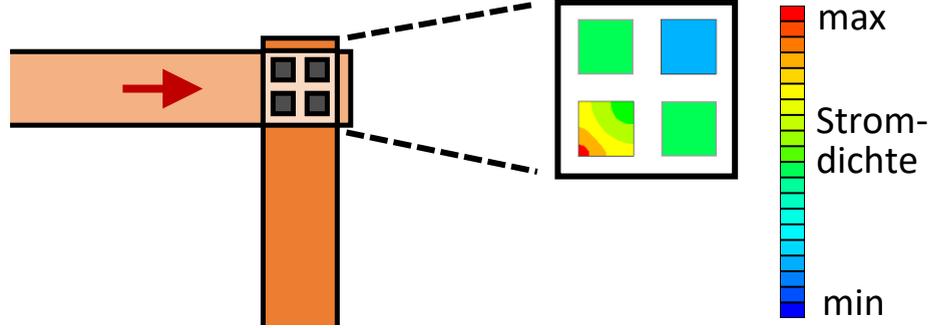
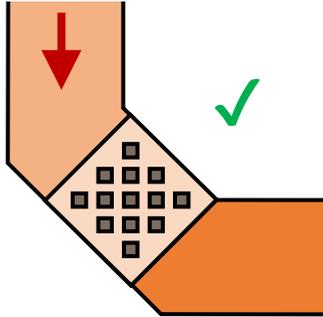
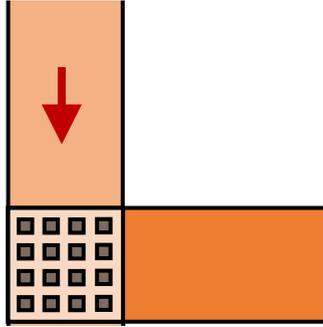
Via-below

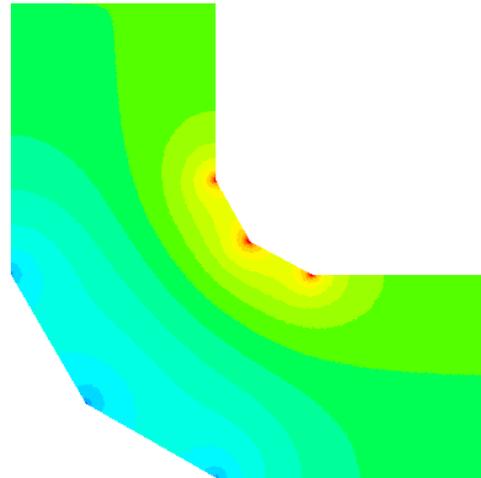
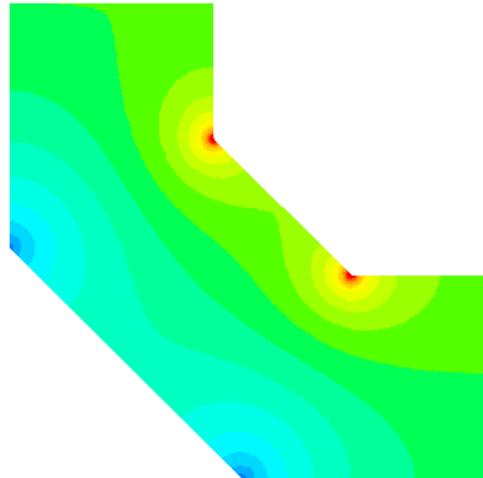
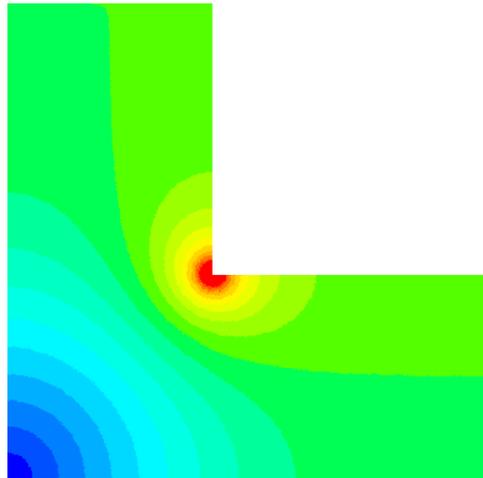


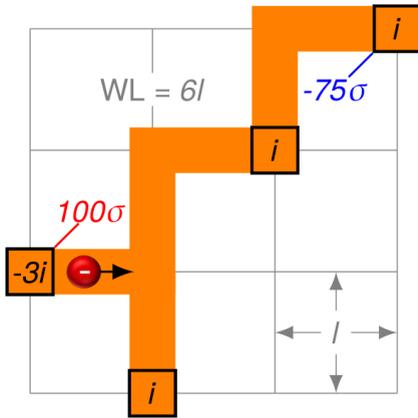
Via-above



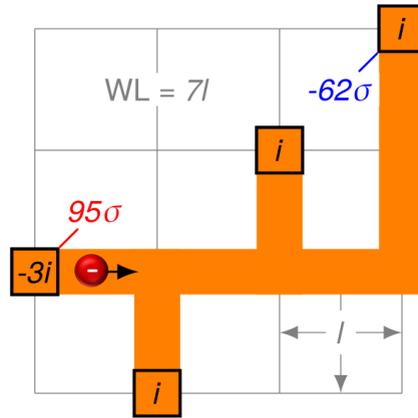
-  Metall (Cu)
-  Barrierschicht (Metal liner)
-  Dielektrische Passivierung (Capping-Schicht)



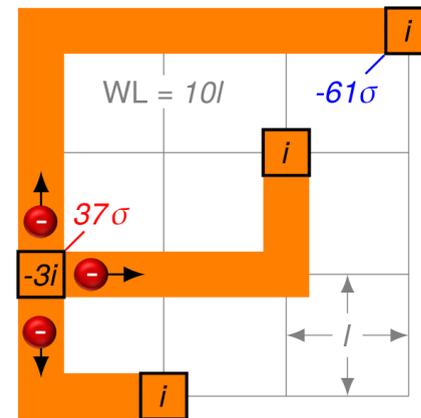




RSMT-Netztopologie



Trunk-Netztopologie



Stromoptimierte Netztopologie