Fakultät Elektrotechnik und Informationstechnik
Institut für Feinwerktechnik und Elektronik-Design

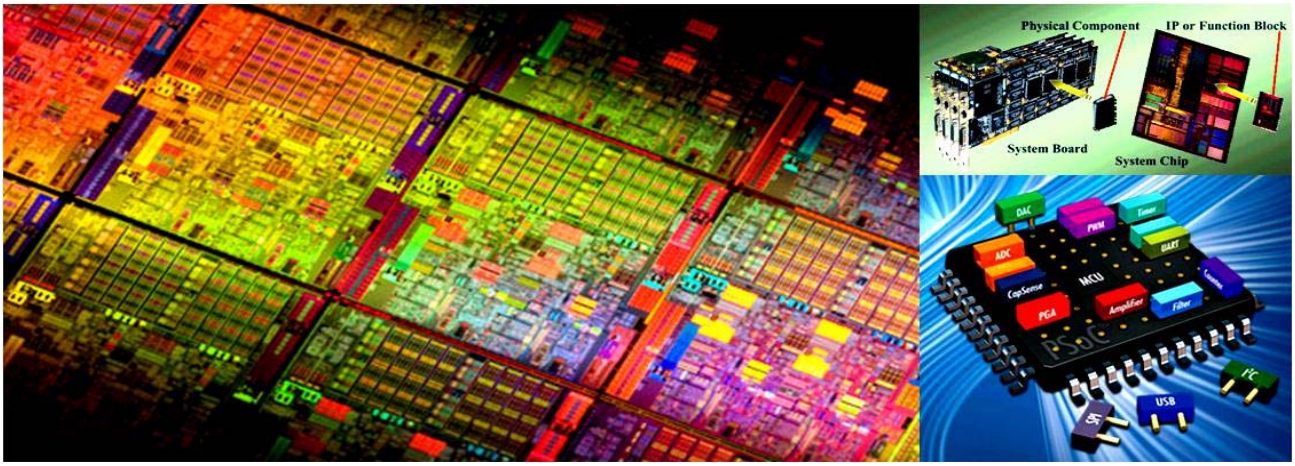
TECHNISCHE UNIVERSITÄT DRESDEN

Einladung zum 127. Institutskolloquium

Thema:	**VLSI Design Verification: Challenges and State-of-the-art**
Vortragender:	**Prof. Dr. Sofiene Tahar** **Concordia University, Montréal, Québec, Canada**
Leitung:	**Prof. Dr.-Ing. habil. Jens Lienig**
Zeit / Ort:	**12. März 2010, 13 Uhr im Barkhausenbau II/56**

In this talk, Prof. Tahar will discuss an important area of R&D activity, namely "VLSI Design Verification". Verification today is known to cost about 70% of industrial VLSI design projects, in terms of human, computer and budget. Many product delays are caused by verification taking longer than expected, and despite multiple efforts, products are delivered with uncaught bugs.

During the seminar Prof. Tahar will present the different kinds of verifications used today in an industrial VLSI design flow, namely design, implementation and fabrication verification. The rest of the talk will focus more on design verification from high level specification to gate level implementation. Several technologies will be displayed and compared, drawing a picture to still open problems and possible research issues. Among them formal verification is one of the most active areas that is carried out in his research group at Concordia University (Hardware Verification Group), which activities will also be briefly introduced during the seminar.



Sofiene Tahar is Professor in the Department of Electrical and Computer Engineering at Concordia University, Montreal, Quebec, Canada. He received his PhD in Computer Science in 1994 from the University of Karlsruhe and his Diploma in Computer Engineering in 1990 from the University of Darmstadt. Prof. Sofiene has made contributions and published over 200 papers in the areas of formal hardware verification, microprocessor and system-on-chip verification, analog and mixed signal circuits verification, VLSI design automation, and formal probabilistic, statistical and reliability analysis of systems. Prof. Sofiene is founder and director of the Hardware Verification Group (http://hvg.ece.concordia.ca).