# Einladung zum 223. Institutskolloquium

Thema: **How Form Follows Function in Integrated Circuit Design**

Vortragender: **Dr. Patrick Groeneveld, Stanford University, Stanford, CA, USA**

Leitung: **Prof. Dr.-Ing. habil. Jens Lienig**

Zeit / Ort: **5. Juli 2019, 15 Uhr im Barkhausenbau II/26**

Microprocessors with 20 billion transistors or FPGAs with 50 billion transistors are incomprehensible, however, they are today's reality. How is it possible to develop integrated circuits that contain more transistors than there are stars in the Milky Way?

In this 45-minutes talk we will analyze the underlying methodologies that are used to design these extremely complex devices. We will start by investigating the surprising differences between the "brains" of the Apple iPhone Xs and the Samsung Galaxy S10+ flagship smartphones. We will also describe the interesting machine learning hardware of Tesla's latest "Full Self Driving" chip. The layouts of these chips do not only reveal their functionality, they also give clues on their physical design methodology. Such an IC design flow consists of hundreds of algorithmic steps that gradually transform a functional description into the actual working circuit. The proper placement and routing of billions of components on a fingernail-sized IC is key in controlling cost, performance, reliability and power consumption. We will discuss how these conflicting objectives are best addressed.
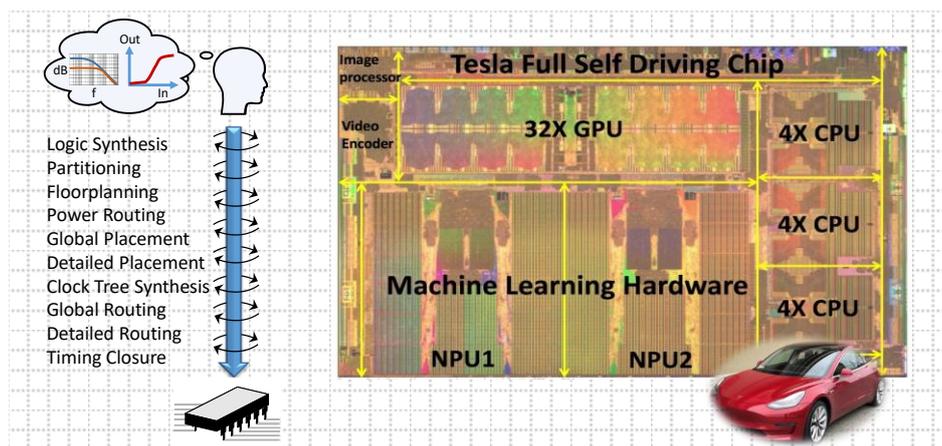
About Patrick Groeneveld, PhD

Before working at Cadence and Synopsys, Patrick Groeneveld was Chief Technologist at Magma Design Automation, where he was part of the team that developed a groundbreaking RTL-to-GDS2 synthesis product. Patrick was also a Full Professor of Electrical Engineering at Eindhoven University. He is currently teaching in the EE department at Stanford University and serves as finance chair in the Executive Committee of the Design Automation Conference. Patrick received his MSc and PhD degrees from Delft University of Technology in the Netherlands.