# FLUTE-EM: Electromigration-Optimized Net Topology Considering Currents and Mechanical Stress

Steve Bigalke and Jens Lienig
Institute of Electromechanical and Electronic Design
Dresden University of Technology
✉ steve.bigalke@outlook.com, ✉ jens@ieee.org

*Abstract*—The future reliability of integrated circuits is endangered by ever shrinking feature sizes and the resulting rise in electromigration (EM) damage. In order to guarantee reliability in future circuits, new approaches are needed in physical synthesis. These approaches must prioritize reliability constraints, such as EM-induced stress reduction during net-topology generation. In line with these insights, our rectilinear Steiner tree is optimized for currents and mechanical stress. We thus aim for optimized EM robustness rather than minimal wire length in the generated net topology. Our results imply a mechanical stress reduction in most cases of more than 50%, thereby significantly abating EM vulnerability. In addition, we show that reservoirs can further reduce the absolute mechanical stress level, and we present an equation for directly calculating the optimal reservoir length.

*Index Terms*—Reliability, Electromigration, Net Topology, Stress, Reservoir

## I. Introduction

In the physical synthesis of very large scale integration (VLSI) designs, producing a net topology with minimal wire length (WL) plays an important role in layout synthesis. It is used in the placement and routing steps to estimate routing congestions, interconnect parasitics or routing paths. The rectilinear Steiner minimum tree (RSMT) is a WL-optimal net topology and the fast lookup table estimation (FLUTE) from Chu [1] is probably the library that is most widely used to determine the RSMT.

Since shrinking feature sizes drastically compromise reliability, we may need to focus our design efforts in future on enhancing reliability instead of minimizing WL. Electromigration (EM) is becoming one of the main cause of chip failures, as downscaling not only increases the EM effect but also lowers EM thresholds. Reliability will therefore be more often endangered by EM damage and might become the downscaling bottleneck [2]. The International Technology Roadmap for Semiconductors (ITRS) predicts that there will soon be no viable solutions available for EM damage [3]. Consequently, a shift from a traditional (post-layout) EM verification towards a robust (pro-active) EM-aware design is needed [4], along with new approaches such as load-aware redundant vias [5] or the presented generation of EM-robust net topologies.

EM is a material migration process caused by collisions between flowing electrons and atoms. Therefore, the main driving force behind EM is current density, which causes atomic dislocation. This dislocation depends not only on current density, but also on the length of an interconnect. It is physically quantifiable by the hydrostatic stress, which we refer to as stress from now on. This stress is not only a consequence of EM but can also serve as its indicator. It is therefore more accurate to identify an EM-robust solution by a relatively low stress than by the widely used current density metric.

In our approach, we aim to reduce the stress by producing an EM-robust net topology (FLUTE-EM) instead of a WL-optimal one, like FLUTE [1]. Our net topology optimizes the connection between the pins in order to enhance the chip reliability in global routing. The subsequent detailed routing can further improve our results, e.g., by vias. Figure 1 illustrates how we reduced the stress of an RSMT net topology by more than 50%. The cost of this reduction is a 60% longer WL.
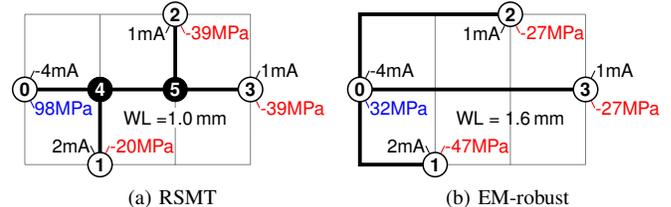


Fig. 1. Reduction of EM-induced stress (red and blue) between the RSMT in (a) and an EM-robust net topology in (b). Pin 0 is a source of $-4\,\text{mA}$ and pins 1 to 3 are sinks of $2\,\text{mA}$, $1\,\text{mA}$ and $1\,\text{mA}$, respectively. Points 4 and 5 are Steiner points. The calculation technique is described in Section II-B.

The first studies on EM-aware net topologies were published in the field of analog design. In 2003, Lienig et al. presented an approach to plan wires (net topologies) in order to reduce the current connection area - representing pin distances, wire widths and currents [6]. Xue et al. solved the Lienig example with a simulated annealing approach, and reduced the area [7]. In 2008, Yan et al. presented an approach for building a rectilinear Steiner tree to reduce the current-driven wire widths. Lin et al. proposed an integer linear programming (ILP) approach to perform the EM-aware wire planning with consideration of obstacles [8]. In 2010, Jiang et al. solved the same problem with a multi-source multi-sink flow network formulation [9]. Tsai et al. took the channel width between the obstacles into consideration [10]. In 2014, Martins et al. minimized the total wiring area with regard to EM and IR-drop constraints for an extended multiport example [11]. Approaches for increasing the EM robustness of digital layouts by addressing detailed routing solutions based on fixed net topologies have been published by Zhang et al. [12] and Paris et al. [13].

All of these studies considered mainly the current or wire width to counteract EM but none of them took the EM-induced stress - produced by material migration - into consideration. Our work is the first to design an EM-aware net topology by considering currents and mechanical stress. We also propose an equation for calculating a reservoir length (this is a passive interconnect structure with no current flow that can further reduce stress).

## II. THEORY

### A. Electromigration in a Single-Branch Interconnect

Electromigration is a material migration caused by the momentum exchange between flowing electrons and fixed atoms. Because of their collisions with electrons, atoms break out of their lattice positions and migrate in the direction of the electron flow. Due to the depletion of atoms at the cathode and their aggregation at the anode, tensile and compressive stresses build up forming voids and hillocks, respectively. A resulting stress gradient is formed producing stress migration (SM) that compensates EM (Fig. 2).
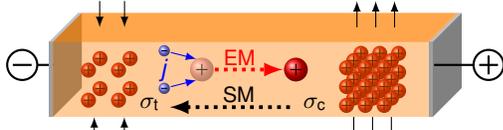


Fig. 2. Electrons (blue) collide with atoms (red), causing the atoms to migrate in the direction of the electron flow. This depletes atoms at the cathode and accumulates them at the anode. These concentration changes introduce tensile ($\sigma_t > 0$) and compressive stresses ($\sigma_c < 0$), respectively.

The stress build-up within an interconnect with blocking boundaries at both ends can be described by Korhonen's equation [14] as

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial l}\left[\frac{DB}{kT}\left(eZ^*\rho j + \Omega\frac{\partial \sigma}{\partial l}\right)\right], \quad (1)$$

with the hydrostatic stress $\sigma$, time $t$, length $l$, diffusivity $D$, bulk module $B$, Boltzmann's constant $k$, temperature $T$, electric charge $e$, effective charge number $Z^*$, resistivity $\rho$, current density $j$ and atomic volume $\Omega$. Equation (1) confirms that the main EM driving force is the current density, and that EM compensation by SM is a function of the length.

Figure 3 plots the stress development described by Eq. (1) in principle. It shows that EM and SM reach a steady state determining the final maximum and minimum stresses within an interconnect. If these steady state stresses are higher than a critical technological stress threshold ($\sigma_{crit}$), EM damage can occur in the form of voids or hillocks.
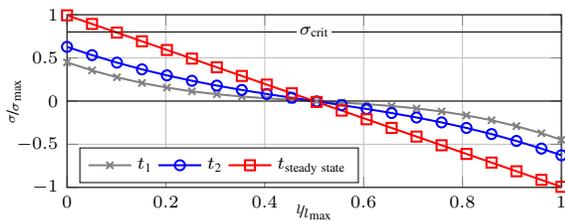


Fig. 3. Basic one-dimensional spatial stress development over time in an interconnect under EM and SM.

### B. Electromigration in Multi-Branch Interconnects

Analog and digital nets consist mainly of multi-branch interconnects. Therefore, one needs to consider the entire net topology. To calculate the stress for multi-branch interconnect problems, we use the voltage-based EM immortality check from Sun et al. [15]. Here, Eq. (1) is applied for multi-branch interconnects to evaluate the overall EM load for any net type. Since our approach produces EM-robust net topologies, we assume that all branches have the same width. This allows us to shorten Sun's approach.

To investigate the cause of the different stress results between Fig. 1a and b, we use the equations from Sun's method [15] for Fig. 1a:

$$V_0 = 0 \qquad L_0 = l_{04} \qquad \sigma_0 = \beta V_g \qquad (2)$$
$$V_1 = i_{04}l_{04} + i_{41}l_{41} \qquad L_1 = l_{41} \qquad \sigma_1 = \beta(V_g - V_1) \qquad (3)$$
$$V_2 = i_{04}l_{04} + i_{45}l_{45} + j_{52}l_{52} \qquad L_2 = l_{52} \qquad \sigma_2 = \beta(V_g - V_2) \qquad (4)$$
$$V_3 = i_{04}l_{04} + i_{45}l_{45} + i_{53}l_{53} \qquad L_3 = l_{53} \qquad \sigma_3 = \beta(V_g - V_3) \qquad (5)$$
$$V_4 = i_{04}l_{04} \qquad L_4 = l_{04} + l_{41} + l_{45} \qquad \sigma_4 = \beta(V_g - V_4) \qquad (6)$$
$$V_5 = i_{04}l_{04} + i_{45}l_{45} \qquad L_5 = l_{45} + l_{52} + l_{53} \qquad \sigma_5 = \beta(V_g - V_5) \qquad (7)$$

$$V_g = \frac{\sum_{i=0}^{5} V_i L_i}{\sum_{i=0}^{5} L_i} = \frac{V_0 L_0 + V_1 L_1 + V_2 L_2 + V_3 L_3 + V_4 L_4 + V_5 L_5}{L_0 + L_1 + L_2 + L_3 + L_4 + L_5} \quad (8)$$

where $V_i$ represents the equivalent voltage at node $i$, $L_i$ the length at node $i$, $i_{ij}$ the current in the edge $ij$ (flowing from node $i$ to node $j$) and $V_g$ the equivalent virtual voltage. In general, upper cases refer to pins or Steiner points (vertices) and lower cases to connections (edges). From now on, we draw the connections as fly lines in our figures but the calculations are always based on the Manhattan length. With Eqs. (2) to (8), the given currents $I$ in Fig. 1a, an assumed area $A$ of $25\,\mu m^2$ ($j = I/A$), an equal length of $l = l_{ij} = 200\,\mu m$ and a factor $\beta$ of $2460\,V\,s\,m^{-2}$ ($\beta = eZ^*\rho/\Omega$), one can obtain the annotated stress values at each node $i$ in Fig. 1a.

To investigate the EM influence of the Steiner point locations in Fig. 1a, we consider lengths $l_{04}$ and $l_{45}$ as independent parameters ($0 < l_{04}, l_{45} < l$). This allows us to calculate the stress as a function of both lengths, as depicted in Fig. 4.
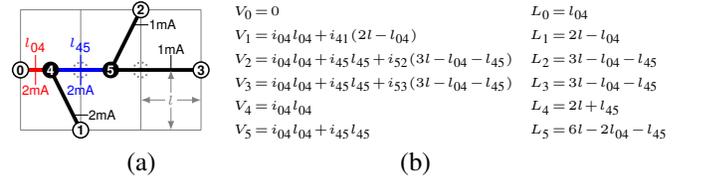


Fig. 4. (a) The Steiner point lengths $l_{04}$ (red) and $l_{45}$ (blue) can vary from 0 to $200\,\mu m$. In (b), we consider both as independent parameters.

The curves in Fig. 5a and Fig. 5b show the maximum stress at pin 0 and the corresponding total wire length. Clearly, the stress and the wire length develop in opposite directions. In other words, the greater the wire length, the lower the stress.

Given that Steiner points reduce the wire length, we come to the following conclusion:

*Axiom 1:* Steiner points increase the EM-induced stress within a net because they accumulate currents from different branches and reduce the wire length. Therefore, Steiner points worsen the effects of EM.
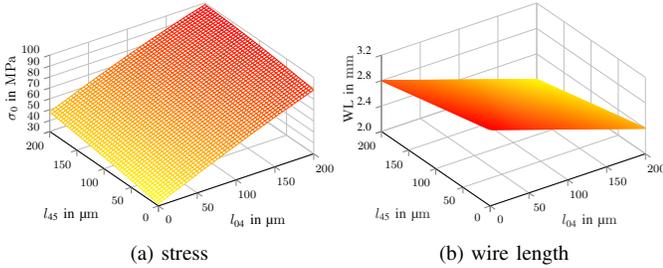
Fig. 5. Stress and wire length curves depending on the location (lengths $l_{04}$ and $l_{45}$) of the Steiner points 4 and 5 in Fig. 4a. The stress is inversely proportional to the wire length.

In the case of a net with one source and any number of sinks (typical in digital designs), the EM net topology with the lowest stress is the clique net model, because it realizes the longest wire length and prevents an accumulation of different currents within one branch. However, if multiple sinks and sources with different currents are present (typical in analog nets), a robust EM net topology is difficult to obtain. To overcome this problem, we propose the following brute force, and iterative approaches for low-degree and high-degree nets, respectively.

## III. Brute Force Approach for Low-Degree Nets

The chicken-and-egg problem here is that without a net topology, one cannot calculate the currents within the net and without the currents, you cannot find an EM-robust net topology. To solve this dilemma, we first randomly select a topology from all possible topologies. Currents and stress values can then be calculated based on the selected topology and pin locations within the net. To find a robust EM net topology, we try all possible net topologies without Steiner points. To do this, we iterate through all possible spanning trees to calculate the occurring stresses. Based on Axiom 1 from the previous section, we expect a robust EM net topology to be without Steiner points. To speed-up our time-consuming brute force approach, we store all valid spanning trees in a look-up table together with their calculation matrices for three to nine pins.

### A. Spanning Tree Generation

Our spanning tree generation is a straight forward trial-and-error approach, because the time to create the look-up table is a one-time cost and therefore of minor interest. Having a net with a number of pins $p$, the number of possible edges $e$ in a spanning tree is equal to the number of edges in a full connected graph given by

$$e = \binom{p}{2} = \frac{p(p-1)}{2}. \tag{9}$$

Knowing that we need exactly $p-1$ edges to obtain a valid spanning tree leaves us with the number of possible trees $t$ as

$$t = \binom{e}{p-1}. \tag{10}$$

Not all of these possible trees are valid spanning trees. We, therefore, have to check that all pins are continuously connected to each other without a loop. All resulting valid spanning trees for a four-pin net are shown in Fig. 6.
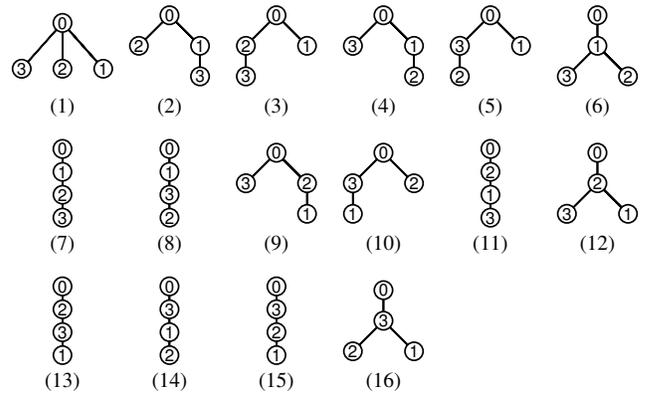


Fig. 6. All valid spanning trees for a four-pin net; they are all tested for their EM robustness.

### B. Direction of Current and Current Calculation

Once the net topology has been picked, one can calculate the current for each edge in the tree by solving Kirchhoff's equations. Since the direction of current is very important for EM, we add a direction to the edges in the tree representation from Fig. 6, as shown in Fig. 7. A positive or negative current value sign signifies respectively that the current flows in the same direction as, or in the opposite direction to, the edge direction.
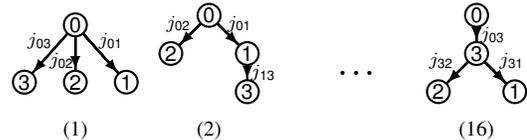


Fig. 7. The edge direction is added to the tree view because the direction of current is an important EM contributing factor. The root is set to the zero node by definition.

### C. Stress calculation

As already mentioned, the stress is then calculated according to the technique presented in [15] by solving Eqs. (2) to (8) to obtain the stress values at each node. We use the currents, Manhattan lengths between pins, area and beta factor as input values for our approach to estimate the stress within each net topology based on the range between the maximum and minimum stress.

### D. Look-Up Table Entries

We show what the look-up entries look like using Fig. 7(1) as an example. The inputs for our algorithm are the $X_i$ and $Y_i$ locations and the currents $I_i$ at each pin:

$$X_i = \begin{bmatrix} X_0 \\ X_1 \\ X_2 \\ X_3 \end{bmatrix}, \qquad Y_i = \begin{bmatrix} Y_0 \\ Y_1 \\ Y_2 \\ Y_3 \end{bmatrix}, \qquad I_i = \begin{bmatrix} I_0 \\ I_1 \\ I_2 \\ I_3 \end{bmatrix}. \tag{11}$$

In the look-up table, the matrices $m_s$ and $m_t$ contain the connections between the source and target nodes for each edge, line by line. The matrix $m_{ij}$ serves to calculate the edge currents

based on the pin currents. Matrices $m_L$ and $m_V$ are needed to calculate the node lengths $L_i$ and equivalent voltages $V_i$ based on the edge currents $i_{ij}$ and lengths $l_{ij}$, viz.:

$$m_s = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix}, \quad m_t = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}, \quad m_{ij} = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix},$$

$$m_L = \begin{bmatrix} 1 & 1 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}, \quad m_V = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}.$$

Edge lengths and currents, as well as the node length, equivalent voltages and stresses are calculated as follows:

$$l_{ij} = |m_s X_i - m_t X_i| + |m_s Y_i - m_t Y_i|, \tag{12}$$

$$i_{ij} = m_{ij} I_i, \tag{13}$$

$$L_i = m_L l_{ij}, \tag{14}$$

$$V_i = m_V(i_{ij} \circ l_{ij}), \qquad (\circ ... \text{element-wise multiplication}) \tag{15}$$

$$\sigma_i = \beta(V_g - V_i). \tag{16}$$

## IV. ITERATIVE APPROACH FOR HIGH-DEGREE NETS

Since the brute force algorithm is very time-consuming for nets with more than nine pins (computing time increases from seconds to minutes), we developed an iterative approach that attempts to reduce the stress with the RSMT solution step by step. It can also achieve a compromise between the RSMT and EM-optimal net topology.

Our iterative approach checks all edges in the initial RSMT solution, and reconnects one edge at a time until it finds the edge that reduces stress the most. This means, we remove one edge after another and build up a set of source and target pins as possible reconnection pins for the currently removed edge. The source and target sets contain all reachable pins found by a depth first search from the source and the target pin of the currently removed edge. Here, we exclude Steiner points, as we expect a robuster EM solution to be without Steiner points based on Axiom 1 above. Removing an edge can cause Steiner points to be obsolete, so we remove Steiner points with less than three connections.

To find the best reconnection pins for an edge, we permute all source and sink pins with each other and calculate the resulting stress based on the reconnection. As we go through all permutations, when we find a more EM robust solution than the previous one, we save the reconnection and continue with the next edge. At the end of the loop, we select the best reconnection edge offering the greatest stress reduction, and mark this new edge as fixed. Then, we continue with the next run, which rechecks all unfixed edges to further improve the stress results until the results can no longer be improved. Searching through edge by edge may seem computationally demanding, but it is still faster than the brute-force (see results in Section V). We must search step by step, as reconnecting an edge affects the other edges.

We select a good result by comparing the stress range between the maximum and minimum occurring stress (a narrow range indicates a more balanced solution). In some cases, the stress range is equal to the previous value. In this case, we take the wire length into consideration as well, and select the

| Current Edge | Source Pins | Target Pins | Better Edge | |
|---|---|---|---|---|
| (5,2) | [3,1,0] | [2] | (0,2) |  |
| (5,3) | [2,1,0] | [3] | (0,3) | |
| (4,1) | [0,2,3] | [1] | (0,1) | |
| (0,4) | [0] | [1,2,3] | – | |
| (4,5) | [1,0] | [2,3] | – | |
| (4,2) | [3,0,1] | [2] | (0,2) | |
| (4,3) | [2,0,1] | [3] | (0,3) | |
| (0,4) | [0,1] | [2,3] | – | |
| (0,2) | [0,3,1] | [2] | (0,2) | |

reconnection if the wire length is shorter than the previously selected length.

Table I lists the edges with source and target vertices for each step for the example in Fig. 1a. In this simple example, our iterative approach finds the brute-force solution.

## V. EXPERIMENTAL RESULTS

### A. Brute-Force Approach

To demonstrate the stress reduction achieved with our brute-force approach from Section III, we apply it to two different types of nets. The first example is a typical signal net with alternating currents in a digital design from Fig. 1a. This time, we include the stress values for the charge and discharge net phases, meaning that all pins change from source to sink, and vice versa. Figure 8 clearly shows that the alternating current cause the maximum tensile stress to become the minimum compressive stress, and vice versa.



| | | | Charge | | Discharge | |
|---|---|---|---|---|---|---|
| i | $X_i$[μm] | $Y_i$[μm] | $I_i$[mA] | $\sigma_i$[MPa] | $I_i$[mA] | $\sigma_i$[MPa] |
| 0 | 0 | 0 | -4 | 98 | 4 | -98 |
| 1 | 200 | -200 | 2 | -20 | -2 | 20 |
| 2 | 400 | 200 | 1 | -39 | -1 | 39 |
| 3 | 600 | 0 | 1 | -39 | -1 | 39 |
| 4 | 200 | 0 | 0 | 20 | 0 | -20 |
| 5 | 400 | 0 | 0 | -10 | 0 | 10 |

(a) RSMT obtained by [1]



| | | | Charge | | Discharge | |
|---|---|---|---|---|---|---|
| i | $X_i$[μm] | $Y_i$[μm] | $I_i$[mA] | $\sigma_i$[MPa] | $I_i$[mA] | $\sigma_i$[MPa] |
| 0 | 0 | 0 | -4 | 32 | 4 | -32 |
| 1 | 200 | -200 | 2 | -47 | -2 | 47 |
| 2 | 400 | 200 | 1 | -27 | -1 | 27 |
| 3 | 600 | 0 | 1 | -27 | -1 | 27 |

(b) The EM net topology obtained with our brute-force approach

Fig. 8. The absolute maximum stress in the RSMT net topology in (a) is almost twice as high as the stress in our EM net topology in (b). The lower stress achieved by our brute-force method comes with a 60% increase in wire length.

The second example is a net taken from [6]; it represents a typical net in an analog design with multiple sources and sinks as well as direct currents. In this example, we compare the stress values for the RSMT net topology, the net topology from [9] (latest study without obstacles) and our net topology.

| i | $X_i$[μm] | $Y_i$[μm] | $I_i$[mA] | $\sigma_i$[MPa] |
|---|---|---|---|---|
| 0 | 200 | 2000 | -7 | 629 |
| 1 | 800 | 1200 | 8 | -728 |
| 2 | 1400 | 200 | 4 | **-965** |
| 3 | 2000 | 1400 | -3 | 156 |
| 4 | 2400 | 400 | -9 | **1042** |
| 5 | 2800 | 1000 | 2 | 432 |
| 6 | 2600 | 2200 | 5 | -256 |
| 7 | 2400 | 1000 | 2 | 511 |
| 8 | 1000 | 1200 | 2 | -571 |
| 9 | 2400 | 1400 | 2 | 236 |
| 10 | 1000 | 1400 | 2 | -335 |

(a) RSMT obtained by [1]



| i | $X_i$[μm] | $Y_i$[μm] | $I_i$[mA] | $\sigma_i$[MPa] |
|---|---|---|---|---|
| 0 | 200 | 2000 | -7 | **776** |
| 1 | 800 | 1200 | 8 | -189 |
| 2 | 1400 | 200 | 4 | **-367** |
| 3 | 2000 | 1400 | -3 | -50 |
| 4 | 2400 | 400 | -9 | 264 |
| 5 | 2800 | 1000 | 2 | 67 |
| 6 | 2600 | 2200 | 5 | -327 |

(b) Net topology from [9]



| i | $X_i$[μm] | $Y_i$[μm] | $I_i$[mA] | $\sigma_i$[MPa] |
|---|---|---|---|---|
| 0 | 200 | 2000 | -7 | 281 |
| 1 | 800 | 1200 | 8 | **-407** |
| 2 | 1400 | 200 | 4 | -329 |
| 3 | 2000 | 1400 | -3 | 183 |
| 4 | 2400 | 400 | -9 | **301** |
| 5 | 2800 | 1000 | 2 | 104 |
| 6 | 2600 | 2200 | 5 | -230 |

(c) Our EM net topology obtained by our brute force approach

Fig. 9. Our net topology in (c) reduces the absolute maximum stress by 61% compared to (a) and by 48% compared to (b). In order to achieve this EM robustness, we had to invest 58% more wire length than in (a) and 18% than in (b).

### B. Iterative Approach

To demonstrate the performance of our iterative approach, we solve the same 7-pin-net example from [6], as above, because we can compare it to the best EM solution found by our brute-force method. We improve the RSMT in the first step by reconnecting edge (10,3) to (2,4). In the second step, we reconnect edge (0,10) to (0,1), and we remove the Steiner points 8 and 10, as they are no longer needed.



(a) RSMT     (b) First reconnection     (c) Second reconnection
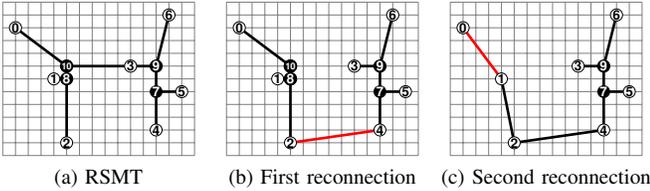
Fig. 10. Improving the RSMT solution iteratively: (a) replace edge (10,3) with (2,4); (b) reconnect edge (0,10) to (0,1); and (c) remove the Steiner points 8 and 10.

The result of our iterative approach seems to be a good compromise between wire-length increase and stress reduction. The approach reduces the stress by 50% with a rise of only 6% in wire length compared to the RSMT.



| i | $X_i$[μm] | $Y_i$[μm] | $I_i$[mA] | $\sigma_i$[MPa] |
|---|---|---|---|---|
| 0 | 200 | 2000 | -7 | **515** |
| 1 | 800 | 1200 | 8 | **-449** |
| 2 | 1400 | 200 | 4 | -331 |
| 3 | 2000 | 1400 | -3 | 259 |
| 4 | 2400 | 400 | -9 | 456 |
| 5 | 2800 | 1000 | 2 | 141 |
| 6 | 2600 | 2200 | 5 | -351 |
| 7 | 2400 | 1000 | 0 | 220 |
| 8 | 2400 | 1400 | 0 | 141 |
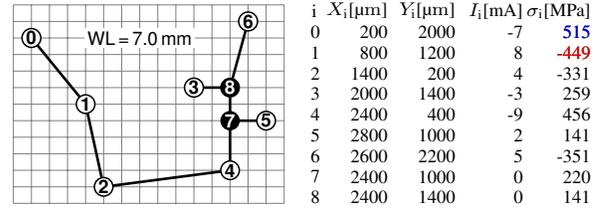
Fig. 11. Net topology generated by our iterative approach for the example from [6]. The absolute stress is about 50% lower than with the RSMT. There is only a 6% increase in wire length. Comparing these values with the best EM net topology found by our brute force approach, which enables a 61% stress reduction with a 58% increase in wire length, shows that this approach offers a good trade-off between stress reduction and increased wire length.

## VI. Additional Stress Improvements With Reservoirs

In the case of an unbalanced stress distribution, as in Fig. 1b, where there is a marked difference in the absolute minimum compressive, and maximum tensile, stresses, the two absolute values can be equalized with a reservoir. The balance between absolute compressive and tensile stresses is expressed by

$$|\sigma_{\min}| = |\sigma_{\max}|. \tag{17}$$

Since the minimum tensile stress is always negative and results from the maximum equivalent voltage (and the positive maximum compressive stress from the minimum equivalent voltage), one can resolve the previous equation as follows

$$-\beta(V_g - V_{\max}) = \beta(V_g - V_{\min}). \tag{18}$$

Given now that the equivalent virtual voltage $V_g$ depends on the node voltage $V_r$ and reservoir length $L_r$, the approach to balance the stresses is

$$V_{\max} + V_{\min} = 2V_g(V_r, L_r). \tag{19}$$

The equivalent virtual voltage $V_g(V_r, L_r)$ expanded by the node voltage and reservoir length is given by

$$V_g(V_r, L_r) = \left( \frac{\sum_{i=0}^{n} V_i L_i + 2V_r L_r}{\sum_{i=0}^{n} L_i + 2L_r} \right), \tag{20}$$

where the reservoir node voltage $V_r$ is equal to the voltage of the node $V_i$ to which the reservoir is connected, since no current flows through the reservoir.

Substituting Eq. (20) into Eq. (19) and resolving the equation according to the reservoir length, yields to

$$L_r = \frac{(V_{\max} + V_{\min}) \sum_{i=0}^{n} L_i - 2 \sum_{i=0}^{n} V_i L_i}{-2(V_{\max} + V_{\min} - 2V_r)}, \tag{21}$$

where $V_{\max}$ and $V_{\min}$ are the nodes in the net with the respective maximum and minimum equivalent voltages.

If the absolute minimum stress is greater than the maximum stress, the reservoir should be connected to any sink, otherwise to any source. The minimum reservoir lengths can be attained if the reservoir is connected as follows

$$\min L_r = \begin{cases} V_r = V_{\min}, & \text{if } |\sigma_{\max}| > |\sigma_{\min}|, \\ V_r = V_{\max}, & \text{otherwise.} \end{cases} \tag{22}$$

If one were to consider the width of a connection, Eq. (21) would contain the node areas $A_i$ instead of the node lengths $L_i$. Different void or hillock stress thresholds or residual tensile stress from the manufacturing process could be considered by lowering the appropriate stress value in Eq. (17).

Analog and digital signal nets alike can benefit from reservoirs because they equalize the absolute minimum tensile stress and maximum compressive stress until the absolute values are equal. In order to prevent any EM damage, it is advisable to keep the absolute maximum stress as low as possible.

Figure 12 visualizes the shortest possible reservoirs for balancing the stress distributions in the examples from Fig. 1a and b, as well as from Fig. 9c. Reservoirs can be located anywhere as long as they realize the calculated length.
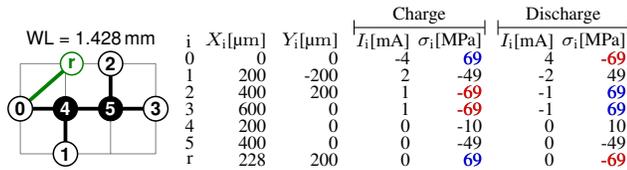


(a) RSMT obtained by [1] with reservoir
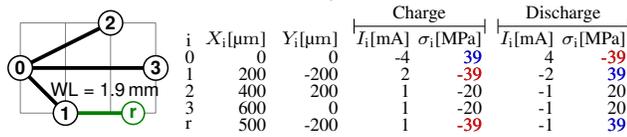


(b) Our EM net topology with reservoir for the example from Fig. 1
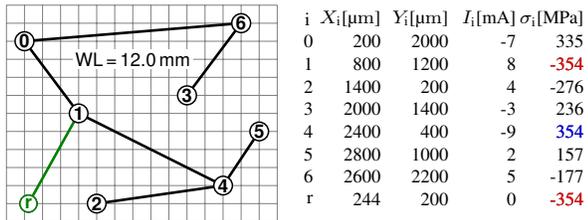


(c) Our EM net topology with reservoir for the example from [6]

Fig. 12. In (a), we improve the stress values in the RSMT solution by 30% with a reservoir, and increase the wire length by 43% over the solutions in Section V. In (b) and (c), we further lower the absolute maximum respective stress by 20% and 15% compared to our brute force solution in Section V with wire-length increases of 19% and 15%, respectively.

## VII. Implementation

Our implementation of the brute-force, iterative and reservoir approaches will be publicly available as open source code under the name EMTO. It is implemented in C++ using the boost and FLUTE libraries. We provide an interface for inputting the $X$ and $Y$ locations as well as the current $I$ for each pin. Our implementation calculates each node's connection given by the predecessor node, the stress value and a reservoir length for each pin based on the theory outlined in this paper. It can be used to determine an EM-robust net topology for any net. It is advisable to harden the nets with the highest EM-induced stresses, and to keep the wire length as short as possible.

Table II contains sample runtimes for our brute force (best result) and iterative (good result) approach on a single core of an Intel Xeon E5-2620 at 2.40 GHz. Runtimes for the brute-force approach in digital nets are clearly very fast. This is because only the clique net topology needs to be calculated.

TABLE II
RUNTIMES FOR ONE SOURCE AND MULTIPLE SINKS (DIGITAL NET) AS WELL AS MULTIPLE SOURCES AND SINKS (ANALOG NET).

| No. Pins | Digital Net | | Analog Net | |
|---|---|---|---|---|
| | Brute Force | Iterative | Brute Force | Iterative |
| 3 | 30μs | 700μs | 60μs | 400μs |
| 9 | 40μs | 17ms | 10s | 15ms |
| 35 | 200μs | 12s | - | 15s |

## VIII. Summary and Conclusion

While FLUTE [1] and the RSMT are well established, it is time to enhance these important approaches with reliability requirements. Given that EM damage is on the rise with every new technology node, an approach like ours that increases the reliability by generating EM-robuster net topologies is absolutely needed. To the best of our knowledge, we are the first to consider stress in the pursuit of EM-robust net topologies. Our net topologies can more than halve the stress in most cases, and thus significantly harden the layout against EM by investing more routing resources. We also show that reservoirs can further lower EM-induced stress, and we are the first to provide an equation for calculating the optimal reservoir length.

## Acknowledgment

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