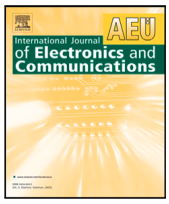
Int. J. Electron. Commun. (AEÜ) 200 (2025) 155909

Contents lists available at ScienceDirect

Int. J. Electron. Commun. (AEÜ)

journal homepage: www.elsevier.com/locate/aeue



Temperature-aware stress-based migration modeling in IC design: Moving from theory to practice

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ARTICLE INFO

Keywords:
Electromigration
Thermal migration
SPICE
Interconnect reliability
Equivalent RC circuits
Temperature

ABSTRACT

Recent research has shown that current density-based models for electromigration (EM) lack precision and should be replaced by physics-based hydrostatic stress simulation. While this new approach is widely accepted in the research community, it has not yet found its way into mainstream IC design flows. This paper aims at bringing state-of-the-art stress-based EM modeling into practical IC design by first examining the reasons that prevent the use of stress modeling in today's verification flows, and then proposing solutions that address these obstacles. We present a method for extracting the necessary technology information from standard IC lifetime testing. The stress modeling approach is then used to calculate the lifetime for example structures based on equivalent RC circuits, using common IC design tools. We further verify this approach by implementing reservoirs for extending interconnect lifetime. Additionally, this paper introduces the effect of local temperature variation and its impact on stress evolution. It is shown how equivalent RC circuits can be extended to also model the impact of local temperature on EM. Finally, we implement thermal migration (TM) into the equivalent RC circuits.

1. Introduction

Electromigration (EM) is a key concern for integrated circuit (IC) reliability. In interconnects that suffer from EM-induced degradation, voids can occur and cause circuit malfunction or complete failure. To prevent this, process design kits (PDKs) contain temperature-dependent current-density limits for short length and long interconnects; these limits are obtained by lifetime measurements on large arrays of test structures [1].

EM modeling has been extensively researched in recent years. It is widely agreed that the conventional current-density verification lacks precision and leads to large safety margins and severe over-design. As current density is reduced by widening wires, this results in (unnecessarily) increased chip area.

Addressing these drawbacks and facing the growing EM issues in small technology nodes, newer models are based on hydrostatic stress evolution (so-called *stress-based* or *physics-based EM modeling* widely ascribed to the work in [2]) with the following advantages:

- capturing the dependency of EM lifetime on wire length,
- handling multi-segment and/or branched interconnects with different current density in each segment,
- considering additional effects, such as local temperature differences, and
- implementing targeted measures enhancing interconnect lifetime.

Despite the enormous advantages that stress-based migration models offer to IC design and reliability, they have not found their way into PDK models, design tools, and thus, IC design flows. While in the EM modeling community stress-based EM lifetime verification is considered the state of the art, IC designers and reliability engineers typically use the empirical models provided in PDKs and are only partly aware of these new modeling methodologies and their possibilities.

To our knowledge, there are three main obstacles preventing the use of stress-based EM verification in IC design: (1) Stress-based models require technology information (i. e., material parameters) that are not provided in standard PDKs. (2) There are no established IC design tools that support stress-based modeling. (3) Scientific publications on stress-based modeling methods come with little to no hands-on instruction on how to implement them in an IC design flow.

Additionally, temperature is usually only considered as a global variable, not as a local interconnect property [3]. Thus, the effect of temperature differences within a wire (both affecting EM and causing

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https://doi.org/10.1016/j.aeue.2025.155909
Received 28 November 2024; Accepted 7 June 2025
Available online 26 June 2025

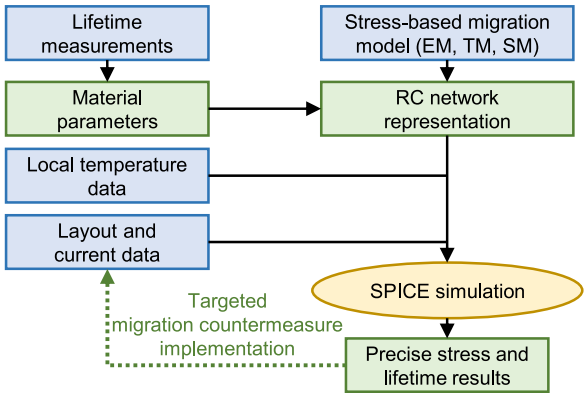

Fig. 1. Overview of our proposed flow on how to apply stress-based migration modeling in IC design. Blue boxes correspond to existing data and models, yellow boxes to recent EM modeling methods, and green boxes highlight the contributions of this paper. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

thermal migration) is widely neglected which leads to errors in lifetime prediction.

This paper aims to close the gap between state-of-the-art stress-based migration modeling and IC design by directly addressing these obstacles and proposing solutions. It is an extended version of [4], which we have expanded by introducing the effect of local temperature variation and its impact on stress evolution: It is shown how equivalent RC circuits can be extended to also model the impact of local temperature on EM. Moreover, we implement thermal migration (TM) into the equivalent RC circuits.

The paper is structured as follows. In Section 2, we introduce the basics of stress-based migration modeling and temperature dependencies. In Section 3, we propose a method for estimating EM material parameters and their temperature dependencies from standard EM lifetime measurements. In Section 4, we present an approach for lifetime calculation using RC networks and SPICE (Section 4.1) which we extend by measures for improved lifetime (Section 4.2), EM temperature dependencies (Section 4.3) and thermal migration (Section 4.4). Since IC designers are familiar with RC models and extensively use SPICE, this method can be intuitively understandable to IC designers and, hopefully, lowers the barrier of using stress-based methods.

Fig. 1 illustrates how our proposed steps are integrated in a migration verification flow.

2. State of the art in migration modeling

2.1. From current density to stress-based modeling

In today's IC design flows, EM modeling relies on two steps:

(1) A maximum temperature-dependent current-density limit for general interconnects is determined using the empirical Black equation [5].

(2) For short wires, a higher current density limit based on the Blech equation is permitted [6].

Black's model is suitable for estimating the allowed current density to ensure a targeted lifetime, but it completely ignores interconnect geometry (e. g., wire length dependency) which influences migration robustness significantly. For very long wires, length indeed has negligible impact on lifetime, but Black's model is known to be highly pessimistic for wires of moderate length (see Section 3.1). Furthermore, it does not consider short-length effects.

The Blech model, on the other hand, checks for "immortal" wires, the so-called short-length effect. In PDKs, it is applied to short wires in which the maximum (steady-state) hydrostatic stress, σ_{steady}, does not exceed the critical stress, σ_{crit}, for voiding (Fig. 2) . A common feature of both models is that they are designed for single-segment interconnects with a constant temperature and stressed with a uniform current density. However, realistic layouts have more complex interconnect geometries (e.g., multiple segments) and different current densities in each wire segment (as illustrated in the example in Fig. 3 which we will come back to in the following sections). Also, temperature differences within a net can occur due to local heat sources and sinks. Thus, applying the models mentioned above to realistic interconnect structures either requires unnecessarily high safety margins or severely underestimates of the actual EM risk [7].

With the critical jL-Product (Blech product of current density j and length L) it is already possible to calculate the steady-state stress of general multi-segment interconnects. The so-called "extended" Blech criterion can thus be used to assess the immortality of realistic interconnects using the procedure in [8].

In contrast, stress-based lifetime modeling cannot be applied in practice yet, because the necessary material parameters are unknown. State-of-the-art (stress-based) EM lifetime models are based on the Korhonen equation and its extensions to multi-segment interconnects. This equation, for a finite single-segment line of length L, describes the evolution of hydrostatic stress, σ, over time, t, as follows:

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}\left[\kappa\left(\frac{\partial \sigma}{\partial x} - \beta j\right)\right] \tag{1}$$

The boundary conditions (BCs) for the single-segment line are given by:

$$\text{BCs:}\quad \left.\frac{\partial \sigma}{\partial x}\right|_{x=0,L} = \beta j \tag{2}$$

Here, j is the current density, $\kappa = DB\Omega/k_{\text{B}}T$, $\beta = e\rho Z/\Omega$, diffusivity $D = D_0 \cdot \exp\left(-E_{\text{a}}/\left(k_{\text{B}}T\right)\right)$, B is the Bulk modulus, Ω the atomic volume, k_{B} Boltzmann's constant, T the Temperature, e the elementary charge, ρ the specific resistivity, Z the electric charge number, D_0 the diffusion constant, and E_{a} the activation energy.

The solution to this equation at a distance x from the cathode, at time t, was derived as [2]:

$$\sigma(x,t) = \beta j L\left(0.5 - \frac{x}{L} - 4\sum_{m=0}^{\infty}\frac{\cos((2m\pi+\pi)\frac{x}{L})}{(2m\pi+\pi)^2 \exp\left((2m\pi+\pi)^2\kappa\frac{t}{L^2}\right)}\right) \tag{3}$$

The above equation (3) enables us to calculate hydrostatic stress evolution in a wire over time. Wire robustness verification with these models detects voiding by comparing σ against the critical stress, σ_{crit}. First, interconnects can be checked for their immortality, invoking the Blech criterion [6] for single-segment interconnects with constant current density, or extensions for multi-segment interconnects with different current densities in each segment [8]. Wires are considered immortal when the steady-state stress at every location of the wire remains lower than the critical stress.

On the other hand, often the steady state is not reached within the lifetime of the chip that contains the wire. Therefore, even for the remaining "mortal" wires, the EM robustness can be verified by checking that the critical stress is not exceeded within the specified lifetime (Fig. 2) [9].

2.2. Considering temperature in migration modeling

Today's PDKs provide temperature-dependent current-density boundaries as invoked by Black's equation. Temperatures are either assigned globally (for the whole chip), net-wise or locally (resulting in temperature differences within nets). Designers are encouraged to predict local temperatures as precisely as possible to avoid pessimistic EM lifetime predictions, as elucidated in [3].

Stress-based EM modeling applying Korhonen's equation, as described in the previous section, is based on two temperature-dependent

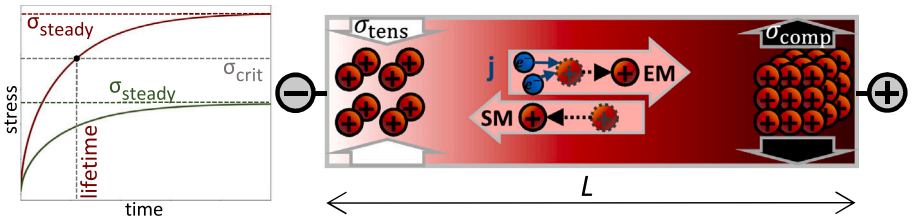

Fig. 2. The basic principle of stress evolution in a single-segment line [1,4]: driven by EM, atoms are pushed from the cathode toward the anode of the wire. The resulting stress gradient causes stress migration as a counteracting force. The tensile stress at the cathode can lead to voids, and the compressive stress at the anode can cause extrusions. In this paper, we focus on voids as the most common EM failure mechanism. The graph on the left shows stress evolution at the cathode end of the wire. If $\sigma_{crit} > \sigma_{steady}$, the wire is considered immortal (green trace). If $\sigma_{crit} < \sigma_{steady}$, the wire will fail when the critical stress is reached (red trace). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

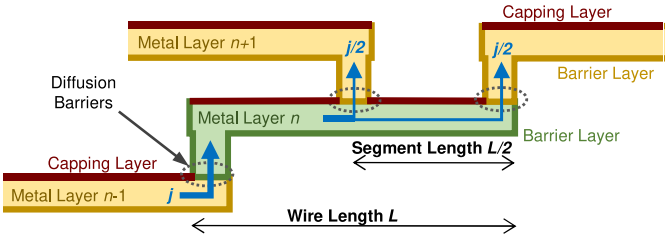

Fig. 3. Illustration of our example in Section 4 in the context of a dual damascene process. We calculate the stress in the green wire, which is part of a more complex net. The diffusion barriers formed by the capping layers allow us to separate the net into stress-wise independent interconnects [4]. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

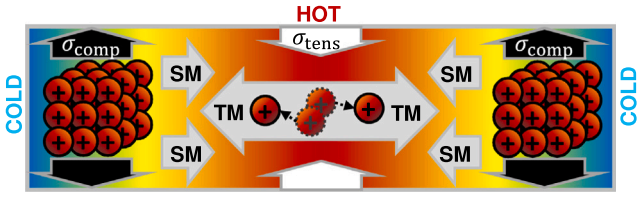

Fig. 4. Thermal migration moves atoms from hot toward cold regions of a wire. The driving force are temperature gradients. The atomic motion causes tensile stress in hot and compressive stress in cold regions of the interconnect [12].

parameters, κ and β, whose explicit dependence of temperature is shown below:

$$\kappa(T) = \frac{D_0 e^{-E_a/k_B T} B\Omega}{k_B T} \tag{4}$$

$$\beta(T) = \frac{e\rho_0(1+\alpha(T-T_0))Z}{\Omega} \tag{5}$$

As in current-density verification, these two parameters can either be set to a constant value (corresponding to a constant net temperature) or vary locally.

Additionally, there is a third migration mechanism driven by temperature gradients. Atoms move from hot toward cold regions of a wire (Fig. 4). This so-called thermal migration (TM) is usually neglected in migration verification, as it is weak compared to EM. However, there are studies indicating that the impact of TM is growing in very small technology nodes and, hence, may become significant for migration-robustness assessment in the future [10–13].

A derivation on how to include TM into Korhonen's equation can be found in [11]. It shows that stress evolution of combined EM, SM, and TM can be calculated as

$$\frac{\partial\sigma}{\partial t} = \frac{\partial}{\partial x}\left[\kappa\left(\frac{\partial\sigma}{\partial x} - \beta j - \gamma\frac{\partial T}{\partial x}\right)\right] \tag{6}$$

with

$$\gamma = \frac{Q}{\Omega T} \tag{7}$$

where Q is the heat of transport.

Hence, when considering TM, we must incorporate a third parameter, $\gamma(T)$, that can vary locally with temperature. Additionally, TM itself is driven by temperature gradients and, thus, is directly dependent on local temperature differences within a net.

Please note that in this paper, we assume the temperature profile of a wire to be known. Nevertheless, we are aware that precisely predicting (local) interconnect temperatures is still an active challenge to be solved.

2.3. Equivalent RC networks for EM simulation of multi-segment interconnects

Several methods have been proposed in the literature for solving Korhonen's equations for general multi-segment interconnects. Most of these simplify migration to a one-dimensional process, neglecting current crowding at wire bends and other similar effects. Nevertheless, this is a reasonable assumption, especially for very small technology nodes, where the EM risk is high and the EM-critical wires are bound to a strict routing direction (due to, e. g., double-patterning in the lower metal layers). This simplification makes EM verification much faster and more efficient. However, three-dimensional simulations are also possible, e. g., by conducting FEM analysis.

In this paper, we will focus on the one-dimensional method of equivalent RC networks because they are intuitively understandable for IC designers and are easy to solve using well-established SPICE simulations. Detailed information on this method for EM simulation at a constant temperature and the derivations for all equations can be found in [14,15]. We will use SPICE modeling as our aim is to ensure tool availability and accessibility rather that optimized runtime. Please refer to [14] for a highly accelerated RC modeling approach applying model order reduction techniques.

In dual-damascene processes, metal layers are separated by diffusion barriers. Hence, we can assume mass conservation for the individual interconnect structures and zero atomic flux at their connection points (i. e., vias) toward other layers [16]. Therefore, in a first step, we split nets into interconnect structures lying within one metal layer. Second, the interconnect structure is divided into smaller elements

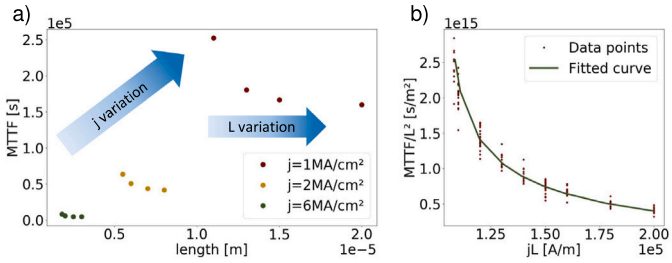

Fig. 5. (a) Lifetime FEM results, (b) Data points with added noise and curve fitting result [4].

(discretization), each with length Δx, width w and height h. Each of these elements is represented by an RC-π-structure, modeled as follows:

$$R = \Delta x/(w \cdot h \cdot \kappa) \tag{8}$$

$$C = \Delta x \cdot w \cdot h. \tag{9}$$

In a third step, current loads i_{EM} are applied as current sources at every point where a current i_{IC} flows into or out of the interconnect with

$$i_{\mathrm{EM}} = \kappa \cdot \beta \cdot i_{\mathrm{IC}}. \tag{10}$$

In practice, this corresponds to adding a current source at every via.

The circuit elements are not to be confused with the *real* (electrical) resistivity, capacitance and currents of the interconnect. They are specifically representing the equivalent circuit for migration modeling. The variables κ and β are the material parameters from the Korhonen Eq. (1).

The resulting RC structure can then be treated using standard electrical techniques. By construction, the voltages in this RC structure map on to the stress at the corresponding nodes in the wire. With an initial condition of zero voltage at every node (for zero initial stress) the circuit can then be simulated in SPICE, and the transient voltage results correspond to the temporal profile of EM-induced stress evolution.

However, this method is only suitable for interconnects at a constant temperature. Temperature differences and their impact on material parameters and TM cannot be modeled. This is where our paper (Sections 4.3 and 4.4) comes in.

3. Material parameters for EM stress modeling

This section presents our novel method for obtaining the material parameters needed for stress-based EM modeling. All scripts used to obtain the results presented here are available online [17].

3.1. Finding material-dependent EM parameters

In order to apply stress-based EM modeling it is crucial to know the material parameters of the technology, i. e., κ, β, and σ_{crit}. These are not provided in PDKs and, to the best of our knowledge, they are not characterized by the fabs today.

In standard EM tests, single-segment wires with length L are stressed with a current density j to determine their lifetime. Based on these measurements, Black's equation, and the Blech criterion, the allowable current densities are determined, depending on the required lifetime after appropriately scaling accelerated aging conditions to normal conditions [18].

Conducting these measurements on mortal wires of different lengths will result in a dataset that captures the dependency of the lifetime on the current density and wire length, as illustrated in Fig. 5a. For the applied current density j, these measurements must cover the length range from just above the longest immortal wire length (where $jL = (jL)_{\mathrm{max}}$) to long wires (where length only minimally impacts the lifetime).

In a single-segment line, the stress profile is symmetric and the maximum stress will occur at the two ends of the wire. Thus, at the moment of failure, we can expect the stress at the end of the wire to equal the critical stress, $\sigma(x = 0, t_{\mathrm{life}}) = \sigma_{\mathrm{crit}}$. Substituting this into Eq. (3), and solving for jL yields

$$jL = \frac{\sigma_{\mathrm{crit}}}{\beta}\left(0.5 - 4\sum_{m=0}^{\infty}\frac{\exp\left(-(2m\pi+\pi)^2\kappa\frac{t_{\mathrm{life}}}{L^2}\right)}{(2m\pi+\pi)^2}\right)^{-1} \tag{11}$$

From Eq. (1), since β and σ are linearly related, we can normalize σ to β. Formally, setting $\sigma' = \sigma/\beta$, Eq. (1) becomes $\frac{\partial \sigma'}{\partial t} = \frac{\partial}{\partial x}\left[\kappa\left(\frac{\partial \sigma'}{\partial x} - j\right)\right]$; BCs: $\left.\frac{\partial \sigma'}{\partial x}\right|_{x=0,L} = j$. The nucleation criterion $\sigma = \sigma_{\mathrm{crit}}$ becomes $\sigma' = (\sigma_{\mathrm{crit}}/\beta)$. Thus, it suffices to know the ratio between σ_{crit} and β and not their individual values, i.e., we only characterize κ and $(\sigma_{\mathrm{crit}}/\beta)$.

To obtain these parameters, we can use Eq. (11) for curve fitting. Terminating the infinite sum at $m = 1$ ensures reasonable precision as the addends of the infinite sum decrease rapidly with m. In practice, the error of the interpolation is determined not by m but by the underlying experimental lifetime data which is noisy and has a limited number of samples. We write each of our data points (Fig. 5) as $[t_{\mathrm{life}}/L^2, jL]$ and understand Eq. (11) as $jL = f(t_{\mathrm{life}}/L^2)$ to find κ and $(\sigma_{\mathrm{crit}}/\beta)$ using the python `curve_fit`-function (from SciPy). For our work, we did not have access to real measurement data. To simulate realistic lifetime results, we performed FEM lifetime simulations (Fig. 5a) with $\kappa = 1.35 \cdot 10^{-16}\,\frac{\mathrm{m}^2}{\mathrm{s}}$ and $\sigma_{\mathrm{crit}}/\beta = 5.20 \cdot 10^4\,\frac{\mathrm{A}}{\mathrm{m}}$. Subsequently, we added random noise (10% standard deviation) to generate 10 data points for each of our FEM simulation results [17]. From that (noisy) data, we obtained $\kappa = 1.38 \cdot 10^{-16}\,\frac{\mathrm{m}^2}{\mathrm{s}}$ (error of 2.2%) and $\sigma_{\mathrm{crit}}/\beta = 5.29 \cdot 10^4\,\frac{\mathrm{A}}{\mathrm{m}}$ (error of 1.7%) as our interpolation results. Fig. 5b shows lifetime normalized to L^2 as a function of jL and how the obtained curve fits the data points.

3.2. Temperature dependency of material parameters

Section 3.1 outlines how we can acquire EM material parameters for one specific temperature. However, the step of transferring these results from accelerated testing conditions (i.e., elevated temperature) to normal operating conditions requires a model for the temperature dependency of EM. The same applies to defining EM limits at different operating temperatures, which significantly impact the permissible current density limits (at lower temperatures, an interconnect can be stressed with higher current densities without violating lifetime constraints).

As described in Section 2.2, these dependencies can be modeled based on the temperature dependencies of κ and β. To obtain these, we can apply the same strategy that is currently used in standard lifetime testing: the experiments from Section 3.1 will be conducted at multiple temperatures $T_1, \ldots, T_{\mathrm{n}}$ to find the corresponding $\kappa(T_1), \ldots, \kappa(T_{\mathrm{n}})$ and $\beta(T_1), \ldots, \beta(T_{\mathrm{n}})$. Subsequently, using Eqs. (4) and (5), we can fit the experimental data into the known temperature-dependent functions of the material parameters. The precision of these results can be increased by using (1) multiple temperature points and (2) a wide temperature range. However, both of these are limited as (1) measuring at more temperature points requires more complex and time-consuming experimental setups, and (2) the temperature range is limited by the

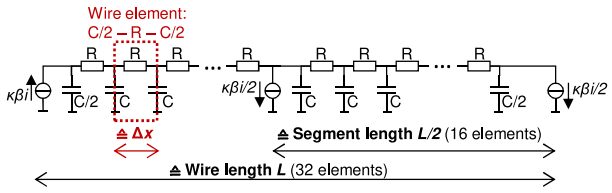

Fig. 6. Equivalent RC circuit for our example in Section 4. Not all π-elements are shown; we divided the two wire segments in 16 elements, each [4].

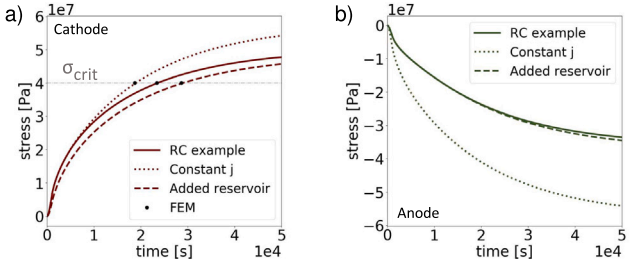

Fig. 7. SPICE results at (a) $x = 0$ (cathode) and (b) $x = L$ (anode) for our example of a two-segment wire, the case with constant current density j for the whole wire for comparison, and our example with a reservoir added to the cathode end at $x = 0$. The stress axis corresponds to the voltage results from the simulation. The results fit well with FEM, the points marked with dots are the FEM lifetime results [4].

duration of the experiment (lower temperatures mean higher time to failure) and the overall temperature stability (higher temperatures can produce unintended failure mechanisms). Fortunately, the already well-established experience of the fabs from current-density characterization can directly be used for determining the temperature dependencies of κ and β. We assume here that σ_{crit} is independent of temperature: this assumption is consistent with the prior literature on migration modeling [10,11].

The experimental characterization of TM and its parameter γ (or, more specifically, the heat of transport, Q) remains an active research topic. The challenge is that in an experimental setup for measuring the impact of EM, the temperature gradient (which is the driving force of TM and must thus be precisely known for TM characterization) can only indirectly be induced by external heaters or Joule heating. One such approach, which uses heaters for the experimental characterization of TM, is presented in [13].

4. Equivalent RC circuits for migration modeling

Next, we demonstrate how RC circuits can be used to run stress-based migration simulation in SPICE. Specifically, we present an approach for lifetime calculation using RC networks and SPICE (Section 4.1) which we extend by measures for improved lifetime (Section 4.2), EM temperature dependencies (Section 4.3) and thermal migration (Section 4.4).

4.1. Estimating lifetime using SPICE simulation

Consider the example in Fig. 3 where the EM lifetime of a two-segment line with current density j in the first segment and $j/2$ in the second segment is to be estimated. In practice, designers typically use one of two approaches to apply the current-density boundaries to this simple configuration, both leading to incorrect results: (1) Taking the total length L (to decide whether to apply short length or standard constraints) and the maximum current density j to compare it with the boundaries given in the PDK; this would be pessimistic, as the second segment is stressed with lower current density. (2) Verifying the two segments independently, taking $L/2$ as wire length and j and $j/2$ as current densities; this approach would underestimate the EM risk as the stress of the two segments will "add up" in reality.

Knowing the material parameters κ and $(\sigma_{\text{crit}}/\beta)$, we can now apply the method from Section 2.3 to this example in two steps:

(1) We build the equivalent RC circuits shown in Fig. 6. Each node voltage corresponds to the node stress σ; to find σ', we exploit the linearity of the circuit: scaling all excitations by a factor $(1/\beta)$ provides node voltages of $\sigma/\beta = \sigma'$. Therefore, we use Eqs. (8) and (9) for the RC values, and apply $i_{EM} = \kappa i_{\text{IC}}$, scaling the current excitation by $(1/\beta)$. Void nucleation is detected by comparing σ' at each node against the characterized $(\sigma_{\text{crit}}/\beta)$ value from Section 3. Both wire segments are divided into 16 elements [15].[1]

(2) We run the transient SPICE simulation and check the nucleation criterion, $\sigma' = (\sigma_{\text{crit}}/\beta)$. If the nucleation time exceeds the targeted lifetime, the wire can be classified as EM-robust. If V_{crit} is not reached at all, the wire is EM-safe.

Fig. 7 shows the results that were obtained with σ_{crit} set to 40 MPa and the extracted parameters, $\kappa = 1.35 \cdot 10^{-16}\,\frac{\text{m}^2}{\text{s}}$, $\beta = 7.69 \cdot 10^2\,\frac{\text{kg}}{\text{s}^2\text{A}}$ (calculated from the extracted $\sigma_{\text{crit}}/\beta = 5.20 \cdot 10^4\,\frac{\text{A}}{\text{m}}$ and the set value for σ_{crit}), $L = 5\,\mu\text{m}$ and $j = i_{\text{IC}}/(w \cdot h) = 150\,\mu\text{A}/(50\,\text{nm} \cdot 100\,\text{nm}) = 3\,\text{MA/cm}^2$. The solid lines show stress evolution for the example described above. For comparison, the dotted lines show stress evolution in the same line, but with constant current density j. Assuming a critical stress of 40 MPa, this leads to an underestimation of the lifetime by $(t_{\text{ref}} - t_{\text{Black}})/t_{\text{ref}} \approx 20\%$. Here, t_{ref} is the lifetime of the interconnect applying the correct current densities and t_{Black} is the pessimistic lifetime assuming the maximum current density for the whole interconnect. Depending on the layout, currents, and material parameters, this impact can range from nearly no difference to the point where an immortal wire is falsely classified as mortal. The dots show FEM lifetime results. We provide full FEM results and scripts in [17].

This simple, yet easily extendable example demonstrates the power of stress-based EM modeling. Please refer to [14,15] for more complex examples like branched interconnect topologies.

4.2. Improving lifetime

For the case where lifetime requirements are not met for certain interconnects, stress modeling also offers some advantages, particularly

[1] The author in [15] states that choosing the number of elements N to be in the range of 16 to 20 leads to precise results regardless of the line length. The simulations that we show here confirm $N = 16$ as a good discretization. However, we found that the number of elements has to be increased with the segment length.

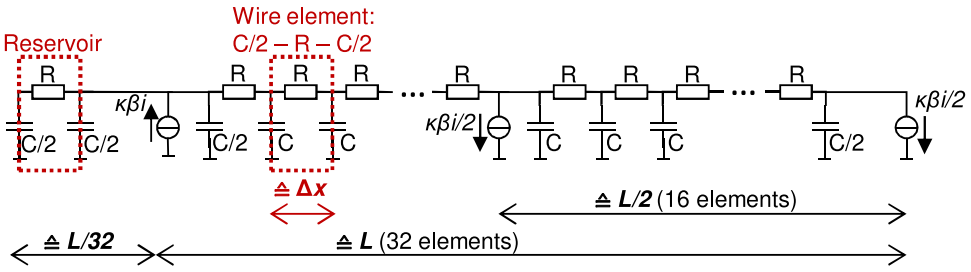

Fig. 8. Equivalent RC circuit with an additional reservoir for extending the wire's lifetime. Not all π-elements are shown; we divided the two wire segments in 16 elements, each.

for multi-segment lines. It shows exactly where the risk of voiding is highest (i. e., which point of the interconnect reaches the critical stress first, $x = 0$ in the example from Section 4.1), and enables us to integrate EM countermeasures [1] at the right place, and check their impact on lifetime. One such measure is the use of reservoirs, i. e. pieces of metal that do not carry current. At a location that would be at risk of voiding, they have the purpose of supplying additional metal atoms.

We can use the method of equivalent RC circuits to model the impact of reservoirs. Like normal current-carrying wires, a reservoir is modeled as an RC network and connected to the corresponding node in the original equivalent circuit. We demonstrate this method by adding one more RC-element $C/2$–R–$C/2$ in our example at the node corresponding to $x = 0$. In the layout, this represents a reservoir of length $L/32 = 0.16\,\mu\text{m}$ as depicted in Fig. 8.

The results are shown by the dashed lines in Fig. 7. We can observe that the steady-state stress is reduced at the critical node $x = 0$. Again, assuming $\sigma_{\text{crit}} = 40\,\text{MPa}$, the reservoir increases the lifetime by $(t_{\text{res}} - t_{\text{ref}})/t_{\text{ref}} \approx 23\%$. Here, t_{ref} is the lifetime of the interconnect without a reservoir and t_{res} is the improved lifetime with the additional reservoir.

This gives us a simple and easy-to-apply method for estimating a reservoir's impact on lifetime and also enables us to assess a reservoir's impact when located at another point of the wire (which might be necessary due to congestion).

4.3. Considering local temperature in EM SPICE simulation

In this paper, we extend the method of RC equivalent circuits for temperature consideration. First, we will focus on the effect of local temperature differences on EM lifetime modeling. As described in Section 3.2, the material parameters κ and β are temperature-dependent and will locally vary if there are temperature differences within a wire. Consequently, in the equivalent RC circuits, the resistors and current sources will also change locally (the capacitors are not temperature-dependent, as shown in Eq. (9)). With the known temperature-dependent parameters, we can write Eqs. (8) and (10) as

$$R = \Delta x/(w \cdot h \cdot \kappa(T)), \tag{12}$$

$$i_{\text{EM}} = \kappa(T) \cdot \beta(T) \cdot i_{\text{IC}}. \tag{13}$$

For the resistors, this strategy can be applied easily. We chose to assign node temperatures to every node of the equivalent circuit (corresponding to a location on the original interconnect) and calculate the temperature for the resistors as the average of the two corresponding node temperatures. As we will describe later, the number of elements N must be increased for temperature consideration which allows us to assume the temperature profile between two nodes to be linear without significant errors.

Adapting the equivalent EM currents i_{EM} is more challenging as merely adapting them to node temperatures would violate Kirchhoff's law. Consider the single-segment line given in Fig. 9, where the two terminals of the wire have different temperatures. This would result

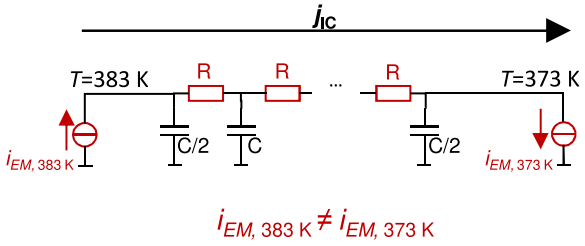

Fig. 9. Example of a single-segment line with a temperature difference between cathode and anode. The resulting temperature-dependent EM equivalent currents are unequal which leads to a violation of Kirchhoff's law.

in $i_{\text{EM},1} > i_{\text{EM},2}$, meaning that the current flowing into the network is lower than the current flowing out of the network.

To resolve that issue, we introduce *temperature currents* i_{T} to the RC equivalent circuit topology. As shown in Fig. 10, these additional current sources will be placed at every node corresponding to a location on the interconnect. They represent the current difference due to the changing material parameters. Thus, we can calculate the temperature current at node n as

$$i_{\text{T,n}} = \kappa_{\text{n}}\beta_{\text{n}} i_{\text{IC}} - \kappa_{\text{n-1}}\beta_{\text{n-1}} i_{\text{IC}} = \Delta(\kappa\beta) \cdot i_{\text{IC}} \tag{14}$$

where node $n - 1$ represents the last node in the direction toward the reference node (see Fig. 10). The reference node is located at one terminal and is the only node without an additional temperature-current source — in this case, we use the node at 383 K.

The number of RC elements N has to be increased compared to EM simulation at constant temperature. This is because of the locally varying material parameters. In our EM simulation, we based the number of elements on the empirical estimate provided in [15] which lead to good results. However, there we assume constant material parameters. For the case of our inhomogeneous temperature profile shown in Fig. 10, we found $N = 50$ as a good compromise of simulation runtime and precision. Like for other numerical simulation approaches (e. g., FEM), N may have to be adjusted depending on the temperature profile, material parameters, current density and interconnect geometry.

To demonstrate the effect that local temperature indeed impacts stress evolution, we added a temperature profile to our two-segment wire and simulated it using the equivalent RC circuit (Fig. 11). For comparison, the stress evolution profiles for constant temperature (applying the maximum and minimum temperatures from the original temperature profile) are also shown. As depicted in Fig. 11, the results from our extended RC equivalent circuit fit well with our FEM simulation. Clearly, the quantitative impact of local temperature on the lifetime is highly dependent on the interconnect, currents, material properties, and temperature differences.

4.4. Combined EM, SM, and TM simulation with SPICE

After introducing temperature-dependent EM parameters in the previous section, we will now focus on thermal migration. Here, tempera-

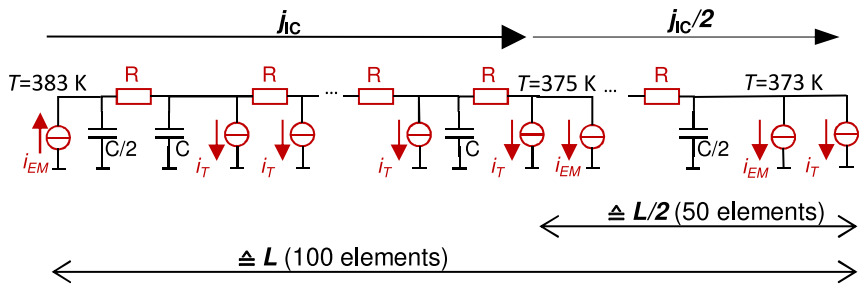

Fig. 10. Extended equivalent RC circuit for our example in Section 4. We model EM with locally increased temperature and linear temperature gradients. Red circuit elements are temperature-dependent. Not all π-elements are shown; we divided the two wire segments in 50 elements, each.

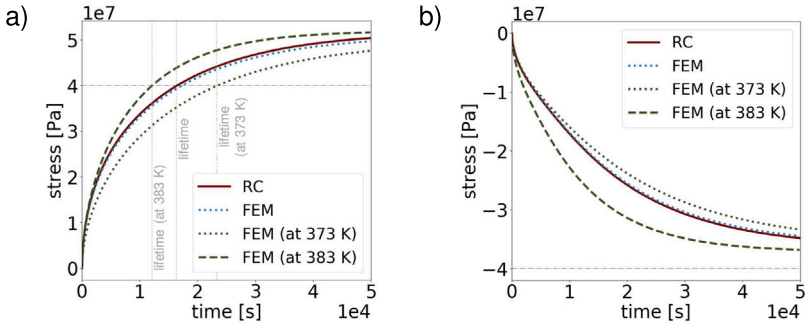

Fig. 11. SPICE and FEM results at (a) $x = 0$ (cathode) and (b) $x = L$ (anode) for our example of a two-segment wire. The cases without temperature differences (at constant temperatures $T = 373\,\mathrm{K}$ and $T = 383\,\mathrm{K}$ for the whole wire) are shown for comparison. The stress axis corresponds to the voltage results from the simulation. The results fit well with FEM; the locally increased temperature decreases the time until the critical stress is reached. The curves of our RC and FEM simulations nearly overlap.

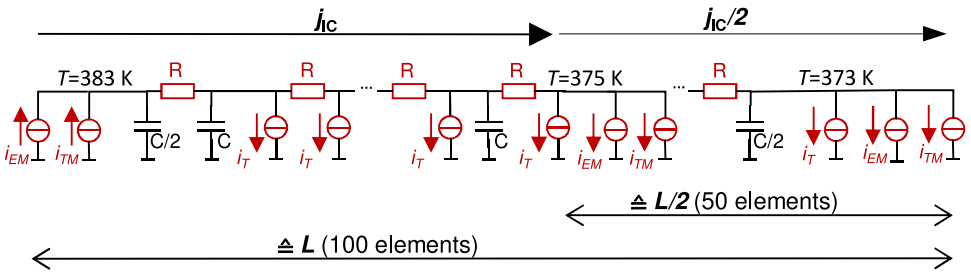

Fig. 12. Extended equivalent RC circuit for our example in Section 4 with locally increased temperature, linear temperature gradients, and TM consideration. Red circuit elements are temperature-dependent. Not all π-elements are shown; we divided the two wire segments in 50 elements, each.

ture differences do not only impact the relevant material parameters κ and γ, but also act as the driving force for TM.

We cannot change the preexisting circuit elements for EM and SM, but we can introduce additional current sources i_{TM} to represent TM. Also, as we can see from Eq. (6), the parameter κ determines both the speed of stress evolution for EM and TM (and SM), which means that we can use the preexisting resistors and the factor of κ for the TM current.

TM impacts both the steady-state stress and the lifetime (i. e., stress evolution). Its driving force is the temperature gradient, which can be calculated as $(T_2 - T_1)/(x_2 - x_1)$ where T_1 and T_2 are the temperatures at the locations x_1 and x_2 of the wire. This corresponds to the current density j as the driving force of EM. As in the EM current sources (i_{EM}) we are working with current ($i = j \cdot wh$), we will also have to multiply our TM current i_{TM} with the cross-sectional area of the wire.

The last missing parameter for TM consideration is γ, which determines the TM-induced steady-state stress. This corresponds to β in EM. Thus, we will include γ as a factor into i_{TM}, which is now calculated as

$$i_{\mathrm{TM}} = \kappa(T)\gamma(T) \cdot wh\frac{\Delta T}{L}. \tag{15}$$

These TM current sources must be added at the terminals of every interconnect, and also at every location where the driving force, i.e., the temperature gradient is changing (Fig. 12). In our two-segment example, we assume linear temperature gradients. The first segment (starting at the cathode) has a higher temperature gradient than the second one (ending at the anode). Consequently, we have to insert TM current sources at the wires ends (cathode and anode) and in the middle of the wire, right between the two segments (at $L/2$).

The TM current sources at a wires terminal can be calculated using Eq. (15). For nodes located along the wire, we can calculate i_{TM} as the sum of TM currents flowing into that node.

Moreover, also for TM we face the issue of violating Kirchhoff's law due to the temperature-dependent parameters κ and γ, as already described in the previous section. Hence, the TM impact must be added to the temperature current sources:

$$i_{\mathrm{T}} = \Delta(\kappa\beta) \cdot i_{\mathrm{IC}} + \Delta(\kappa\gamma) \cdot wh\frac{\Delta T}{L}. \tag{16}$$

As for EM, the TM temperature current corresponds to the temperature-induced difference between the TM currents flowing into and out of a node.

Q is reported to be in the range of 0.09 – 0.9 eV [19]. In our example, we use a heat of transport of $Q = 0.3\,\mathrm{eV}$. We intentionally use strong temperature gradients to demonstrate the TM representation in the RC

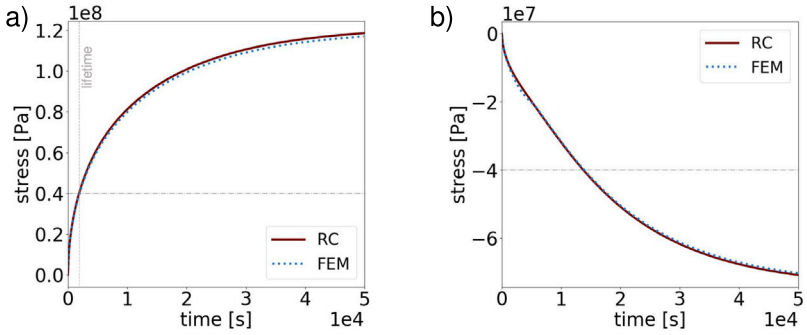

Fig. 13. SPICE results at (a) $x = 0$ (cathode) and (b) $x = L$ (anode) for our example of a two-segment wire with combined EM, TM, and SM simulation. In our case, the location with the highest temperature is at the cathode, thus, TM increases the total stress and decreases the lifetime. The stress axis corresponds to the voltage results from the simulation. The results fit well with FEM, i. e., the curves nearly overlap.

network. Further, we assume that the temperature gradient drives the atoms in the same direction as EM. Consequently, the steady-state stress is much higher with TM consideration (Fig. 13) than the case where TM is neglected (cf. Figs. 7 and 11). Moreover, the lifetime is decreased significantly.

5. Summary

Stress-based migration modeling outperforms today's practice of current-density verification in many ways. However, even after years of promising research on these models, they have not found their way into contemporary IC design flows. Facing the increasing design challenges in terms of reliability, we believe that stress-based modeling must finally be applied in IC design.

With this paper, we aim for implementing state-of-the-art stress-based migration modeling in today's IC design. First, we looked at the difficulties preventing the application of stress-based modeling. We found that two of the main challenges are the missing technology information and the lack of tools for stress-based verification. We presented a pragmatic approach of overcoming these challenges by providing a method for estimating the necessary material parameters from standard lifetime testing.

Second, we demonstrated how a recently published method of equivalent RC circuits can be used to run stress-based EM simulation in SPICE. We showed how reservoirs can be modeled using the RC method and how they can be used to increase lifetime. We further improved that method to also model both the effect of local temperature on EM and the impact of TM.

Using a simple example, we finally presented the advantages of stress-based modeling compared to conventional current-density verification. We demonstrated the impact of local temperature differences on lifetime prediction. Our results and scripts are publicly available in [17].

CRediT authorship contribution statement

Susann Rothe: Writing – original draft, Visualization, Validation, Software, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Jens Lienig:** Writing – review & editing, Supervision, Resources. **Sachin S. Sapatnekar:** Writing – review & editing, Supervision, Resources.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgments

A preliminary version of this paper has been published in the proceedings of the 2024 International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD) [4].

This work was supported in part by the National Science Foundation, United States under awards CCF-2212345 and CCF-2437795, the Claussen-Simon Foundation, Germany, and the Deutsche Forschungsgemeinschaft (DFG, German Research Foundation), Germany – 525041614.

Data availability

Data available on GitHub [17].

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