BGA Lifetime Prediction in JEDEC Drop Tests Accounting for Copper Trace Routing Effects

Frank Kraemer[1)], Steffen Wiese[1)], Sven Rzepka[2)], Jens Lienig[3)]
[1)] Fraunhofer CSP, Halle/Germany;
[2)] Fraunhofer ENAS, Micro Material Center Chemnitz & Berlin/Germany:
[3)] Dresden University of Technology, Institute of Electromechanical and Electronic Design, Germany
frank.kraemer@csp.fraunhofer.de

Abstract

Experimental drop test results of 2nd-level assemblies can be influenced by numerous impact factors. The explicit definition of drop testing conditions by the JEDEC standard JESD22-B111 was intended to create a highly repeatable, and thus comparable, experimental setup. Recent developments showed, however, shifting failure modes from component to PCB side.

Comprehensive drop tests were executed with 3 different memory packages. Failure analysis surprisingly found electrical fails of the assemblies on PCB side with broken copper traces next to the PCB pads. Detailed investigations showed a strong influence of the copper trace routing on their failure probability. Broken copper traces were only found when their routing direction was aligned to the dominating PCB deflection.

The new experimental insights were proven by a two steps simulation approach. In the first step, an experimentally calibrated and validated 3-D JEDEC board model has been set up. In the second step, the copper trace routing effect was investigated by a 3-D sub-model of a single BGA component.

The direction of copper trace routing showed a clear effect on the plastic copper strain. Simulation results were able to prove the experimental observations. Using these results, reliability modeling was started for two drop test configurations: 4-screw and 6-screw board clamping. In both cases, the sequence of failure of the components on the board was matched by using a combined criterion of plastic strain-rate and resultant force integral. The lifetime model based on this criterion was able to predict the experimental cycles-to-failure with less than 25% deviation.

Introduction

Critical test for package qualification can increase time to market dramatically if the test is not passed safely. Drop tests have become such kind of critical experiments since lead was banned from solder materials. Virtual prototyping can overcome those problems already in the early design phase and ensure high product reliability.

The development of virtual prototyping requests high reproducible experiments in order to ensure the verification of simulation models by the deformation behavior and lifetime assessments. In case of high dynamic testing, the JEDEC drop test [1] is the best suited experiment in order to fulfill those requests. This paper presents first steps on the development of a virtual lifetime assessment. Detailed drop test experiments were executed in order to gain trustworthy characteristic cycles-to-failures for different package types. In contrast to many other researchers those characteristic lifetimes were evaluated for each of the 15 component positions on the JEDEC board. A sequence of failure was derived with these lifetimes which were utilized for the evaluation of simulation result criteria. With this criterion a lifetime model should be developed, which predicts the experimental cycles-to-failure with less that ±50% inaccuracy.

Next sections describe the experimental setup and the design of experiments. A detailed failure analysis is executed in order to focus simulations on critical sections of the 2nd-level assembly and determine rules for lifetime prediction.

Drop test experiments

The experimental investigations were executed on a commercial drop test tower at the backend development center of Qimonda Dresden. The schematic setup is shown in figure 1.

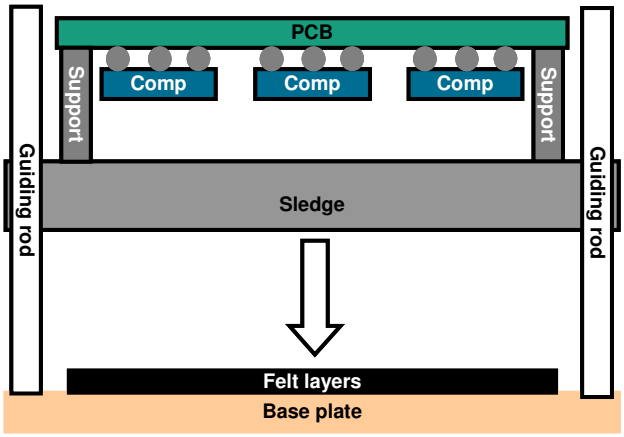


Figure 1: Schematic of the JEDEC Drop Test Configuration

The specimen is fixed via supports on a sledge. The sledge is mounted between two guiding rods. The sledge can move freely along the rods when it is released from a certain height and drop onto a solid base plate. The base plate is covered with felt layers, which decelerates the sledge. Using this experimental configuration a well de-

978-1-4244-7027-310/$26.00 ©2010 IEEE

11th. Int. Conf. on Thermal, Mechanical and Multiphysics Simulation and Experiments in Micro-Electronics and Micro-Systems, EuroSimE 2010
EuroSimE 2010, pp. 1-8, DOI:10.1109/ESIME.2010.5464560

fined half-sine acceleration impulse is created and transferred with a constant impact angle into the specimen. The experimental results presented here were typically gained by using the JEDEC condition B [1] with a peak acceleration of 1500G and a duration of 0.5ms. In this condition a few hundred drop cycles were necessary to create sufficient failure data for each 2nd-level assembly.

The JEDEC PCBs are defined in their size, the stack-up, material and boundary conditions by the standard. With these specifications equal vibration behavior can be achieved for each sample, which allows a direct comparison of the drop test performance of different packages. Furthermore, the high reproducibility of experimental results is ensured with this standard. In addition to these definitions, the test specifications at Qimonda were modified at two items. In addition to the 4-screws fixture condition two more fixtures at the middle of the JEDEC PCB were employed for higher eigenfrequencies and different deformation behavior of the PCB. Secondly, a closer relation to the productive PCBs was achieved by the replacement of the outermost resin only layers of the PCB stack-up by glass-fiber resin layers.

Investigations were executed using three different BGA packages. The geometrical data of these packages are listed in table 1. The packages were assembled with the PCB using SnAg1.0Cu0.5 solder balls. According to the high volume situation, ENiG pad finish was used on component side. The PCB pads were covered with Cu-OSP finish.

Table 1: Geometrical data and I/O arrangement of the tested daisy chain packages

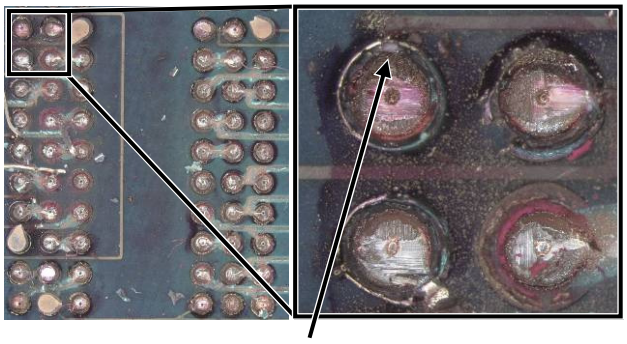
Label	VFBGA-90	VFBGA-60	TFBGA-60
Height [mm]	0.8	0.8	1.2
Package area [mm]	12.5 x 9.5	10.0 x 9.5	10.5 x 8.0
Number of Balls	90	60	60
Ball-out size [mm]	11.2 x 6.4	7.2 x 6.4	8.0 x 6.4
Ball arrangement	15 x 6, full rows	10 x 6, full rows	11 x 6, partly populated

The packages applied daisy chain structures covering almost all of the interconnections. With this setup each of the 15 packages on the JEDEC PCB were monitored by in-situ resistance measurements. This way electrical integrity was captured without delay. According to the standard a package was defined as defect, if its resistance is beyond 1kΩ in three consecutive drops. The numbers of cycles-to-failure were recorded for every package type at every component position separately. These results were used in order to derive sequences of failure for every package type.

Experimental lifetime and failure analysis

Based on numerous publications brittle IMC cracks were expected to be the dominating failure mode in drop tests [2-4]. Intermetallic compounds like Cu_6Sn_5 or $(Ni, Cu)_3Sn_4$ are formed at the pad/solder interfaces during RoHS conform soldering. High stresses are created on these interfaces during drop tests due to high stiffness of lead-free solders and their strain-rate dependent hardening effect. Therefore, the weakest link is shifted to the IMC.

Failure analysis applying the dye and pry test revealed almost no IMC cracks. Defects of the daisy chains were dominated by PCB pad lifts and broken copper traces, which is in agreement with very recent publications [5-7]. The broken copper traces triggered the electrical fails for all of the investigated packages with 4-screws as well as 6-screws fixture of the JEDEC board. IMC cracks were found rarely and none of them caused an electrical defect of a package. Figure 2 shows the failure analysis of a VFBGA-60 package (tab.1), which was tested under JEDEC condition B with 6-screws fixture.



a) Brocken copper trace b)

Figure 2: Dye and pry test results of a VFBGA-60 package, a) Complete ball-out; b) Ball-out section with broken copper trace at a lifted PCB pad

More detailed failure analysis has shown that under 6-screws boundary condition broken copper trace did not appear at every outermost PCB pad. In fact copper cracks could only be found if a trace was routed along the short edge of the PCB. This is the direction of highest PCB deflection with this boundary condition. Furthermore, failure appearance was not limited to the outermost PCB pads only. Dependent on the daisy chain routing, failures could be found anywhere on the uppermost and lowermost interconnection rows. Obviously the trace routing has a strong effect on the copper stress. This will be further investigated applying detailed FEM simulations.

The target of this investigation is the development of a lifetime model for drop tests based on FEM simulations. Simulations are idealistic mathematical abstractions of a non-idealist experiment. Since experiments are subjected to scatter, single results have to be fitted with statistical

methods like the Weibull distribution for better comparability with simulation results.

Weibull distributions were compiled for every package type at all of typically failing positions on the board. Figure 3a depicts two of such distributions for the TFBGA-60 package at position #8 (fig. 3b). In 6-screws fixture mode the occurrence of failure scattered from 48 to 83 cycles. This was a rather small scatter band, which resulted in a big slop of the fitting curve. With 6-screws boundary condition, packages at position #8 were the most critical on the JEDEC board. The number of characteristic cycles-to-failure was 67.6 cycles. The second curve shows the cycles-to-failure distribution with 4-screws boundary condition. Failures scattered from 448 to 621 cycles, which was much higher in absolute scale than scatter at 6-screws fixture. In logarithmic scale, however, both dispersions were similar leading to almost parallel slops of the fitting curves. Position #8 was not the most critical in 4-screws fixture mode due to different PCB deformation. In this condition the N_{63}-value rose to 520 cycles. Since copper trace cracks remained the dominating failure mode, the stress on copper should be much lower in 4-screws fixture mode than with 6-screws boundary condition.

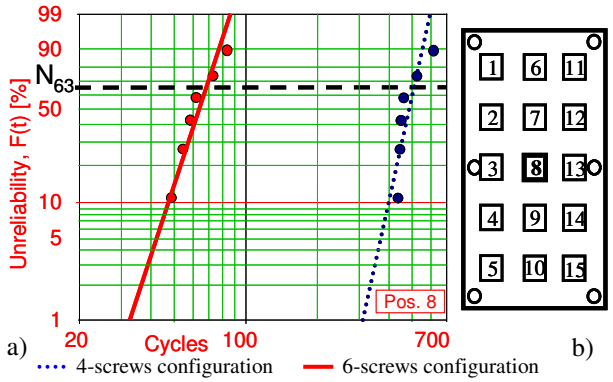


Figure 3: a) Weibull distributions for package-type TFBGA-60; 4- & 6-screws tests; component position #8; b) Component positions on the JEDEC board

Table 2: Compilation of characteristic cycles-to-failures and sequence of failure of the most critical component positions tested under 6-screws fixture

Package type	VFBGA 60	VFBGA 90	TFBGA 60
Comp 06	-	88.7 (4)	-
Comp 07	290.6 (3)	93.9 (5)	161.2 (3)
Comp 08	89.7 (1)	43.1 (1)	67.6 (1)
Comp 09	141.4 (2)	58.4 (2)	112.8 (2)
Comp 10	-	69.5 (3)	-

The characteristic N_{63} values of each Weibull distribution are listed in table 2. The table shows values gained with 6-screws fixture only. Critical component positions were concentrated in the middle row of the JEDEC board. In this boundary condition the packages of the middle row were situated in the section of highest PCB deflection leading to high stress of the copper traces. Component position #8 was the most critical of all investigated package types followed by position #9. Comparing the N_{63}-values with the package geometry it became obvious that bigger components fail earlier. The biggest package, VFBGA-90, even failed at positions #6 and #10 while the smaller packages hardly failed there. This trend was already observed in temperature-cycling tests. The arrangement of N_{63}-values resulted in a sequence of failure for the critical component positions on the board. This sequence will be used for a first qualitative result criteria evaluation of global FEM simulations.

Finite Element Model of the JEDEC drop test

Drop tests are high dynamic experiments that create big plastic deformations. An adequate simulation software has to apply an explicit time integration in order to account for both characteristics correctly. This request is fulfilled with the FEM code LS-Dyna™.

The global model is a complete but rather coarse representation of the entire drop test assembly, see fig. 4. The JEDEC board is modeled without any symmetry conditions, since the global vibration behavior was found to be unsymmetrical [8]. The JEDEC board comes with all 15 components and the supports.

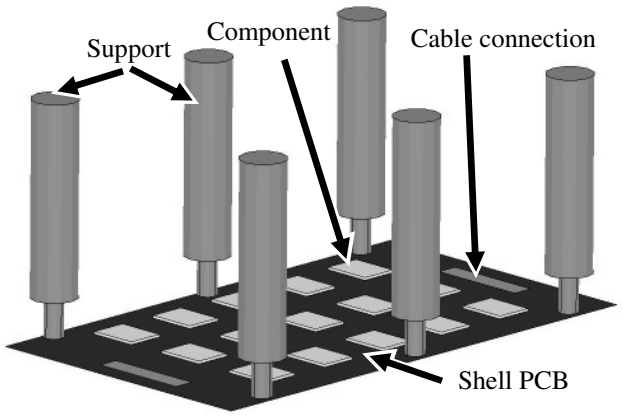


Figure 4: Global model of the JEDEC drop test board with 6 supports and all 15 components

The PCB is meshed with shell elements, which have the ability to capture the composite matrix material of LS-Dyna (*MAT_117) [9]. The complex construction of the PCB results in different tensile and bending stiffness of the laminate [10, 11] which can be captured with this material model. Both properties affect the PCB vibration behavior and the component stress and thus should not be split or neglected.

The global model components are rather coarse representations of the actual memory packages. The bodies

have hexahedral outlines with the size of each package type. The solder balls are arranged according to the specific package as well, e.g. in a DDR2 mapping for the TFBGA-60, see figure 5. Solder bricks meshed with 8 elements of identical size are used at the uncritical inner interconnections. The critical solder joints at the outermost rows are modeled as barrels. These joints replicate the actual dimensions at both pads as well as the equator level. The barrel joints are still meshed in a coarse way using 24 elements, which was found sufficient for a lifetime modeling attempt. The solder balls are directly attached to the component body at one side. The opposite sides are connected via offset contacts to the shell elements of the PCB.

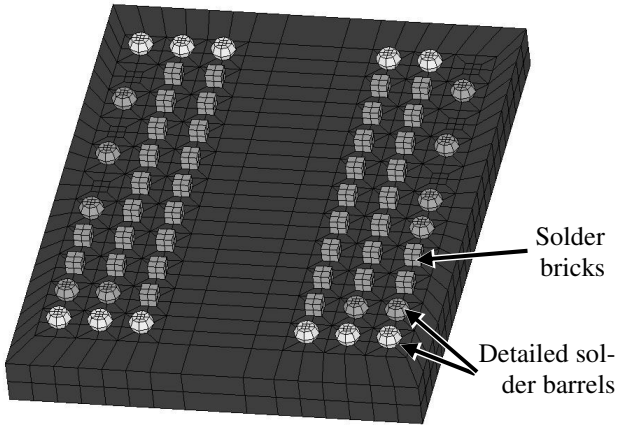


Figure 5: TFBGA-60 component for the global drop test model

The component bodies have effective elastic properties similar to mold compound, coming from the coarse component representation and its failure-free behavior. The solder balls are supposed to fail and to dissipate energy during PCB vibration. They use a plastic material model with strain-rate dependent hardening. Material data for lead-free solders were determined in [12], which are listed in table 3.

Table 3: Strain-rate dependent yield stress of the solder material model

Strain-rate [1/s]	10^{-4}	10^{-3}	10^{-1}	10^{0}	10^{1}	10^{2}	10^{3}
Yield stress [MPa]	40	45	58	67	75	88	105

High effort has been spent in order to represent the PCB vibration behavior as realistically as possible, since it determines the component stress and stress distribution, respectively. Acceleration profiles were found to be the best suited way for comparison of experiment and simulation, because these curves directly show dynamic informations like the vibration frequencies, maximum PCB deformation and damping behavior. Accordingly acceleration profiles at different positions on the JEDEC board were measured and applied for FE model evaluation.

Sections of plated through hole (PTH) via arrays are situated at the short edges of the board. They enable the in-situ resistance measurement of the daisy chains via cable connections. Acceleration measurements showed that a cable connection strongly adsorbs the PCB vibration in this section affecting the overall vibration behavior [8]. This effect was considered by additional damping of one via array.

Furthermore, the setting of fixtures and load application requires additional attention. A first attempt to apply boundary conditions and load initiation at the mounting holes of the PCB failed, since the system behavior was too rigid, see figure 6. The adjustment of the PCB's material properties would require a stiffness reduction down to 10% of its original value, which was not realistic. It was found necessary to model the supports and shift the boundary conditions and load initiation at the bottom of these legs. Even though these cylinders are made of steal with 12mm diameter, they were able to effectively soften the PCB response. The peak acceleration after shock initiation and the basic vibration frequency are close to the experimental profile. The remaining root-mean-square between experimentally measured and simulated acceleration profiles was reduced by 70% as compared to the initial model.

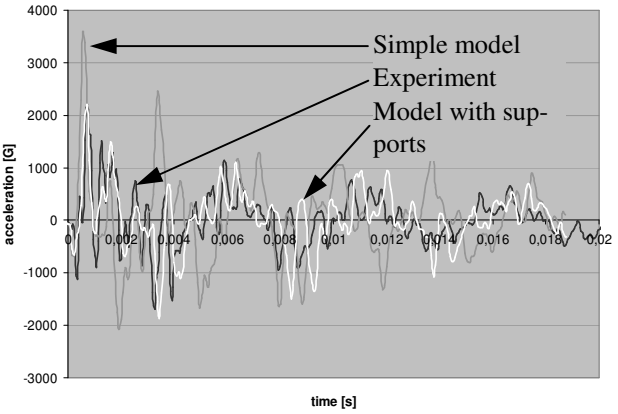


Figure 6: PCB vibration behavior of experiment and different simulation methodologies (6-screws)

The global modeling methodology presented here was successfully verified for 4-screws boundary conditions, too. It sets a solid basis for further sub-model investigations and lifetime modeling.

Sub-models for detailed package investigations

The copper trace routing effect, seen in failure analysis, was investigated with a sub-model. The sub-model applied here is a detailed representation of a single package on the JEDEC board, see figure 7. This model includes all mechanically relevant component parts of the investi-

gated BGA package. The 3-D component body covers the substrate, die-attach, die, mold-compound and solder mask at either of the substrate sides. The material models for all of these parts are simple elastic, because no failures appear within the component body and the materials have a linear behavior at the deformation speeds created under drop test conditions. According to the global model, the sub-model PCB consists of shell elements. Again, these elements apply LS-Dyna's composite matrix material model.

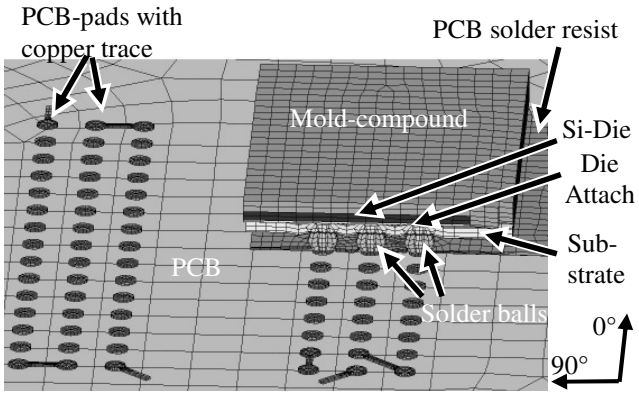


Figure 7: Cross-section view of a VFBGA-90 sub-model mesh

The 2nd-level interconnections are modeled in a very detailed way including the solder joint as well as substrate and PCB pads. Hereby, the mesh density of inner interconnections is reduced because of their lower stress levels. Outermost interconnections use finer meshes with about 500 elements, each. PCB-pads of these interconnections can be connected to a single copper trace. Figure 8 shows the possible routing directions and their nomenclature. Each copper trace can be connected to 8 different routing directions in steps of 45°. These steps are sufficient to capture any practical routing condition and to perform the routing dependent stress analysis at the copper traces.

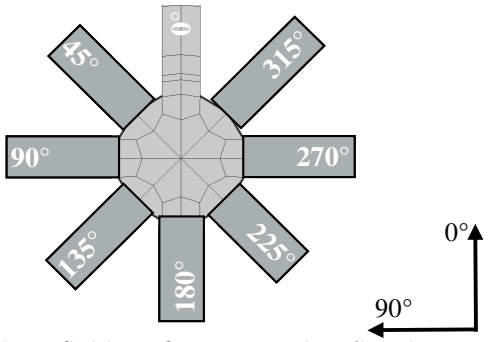


Figure 8: Definition of copper routing directions at the sub-model PCB-pads

Due to possible failure occurrence plastic material models are necessary for copper and solder. The solder joints apply the strain-rate dependent plastic material model presented above, see tab. 3. The PCB and substrate copper apply a bilinear plastic material model neglecting any hardening effects (*MAT_003) [9]. Published material properties of copper vary in a remarkable range, which can be strongly influenced by production processes. The data applied here are based on some conservative assumptions e.g. using a Young's modulus of 127GPa and a yield stress of 65MPa.

The copper trace routing effect

The copper trace routing effect was investigated with package TFBGA-60 at position #8 on the JEDEC board, see figure 9. This package was chosen due to its distinct failure distribution during experiments. Global deformations applied both 4-screws and 6-screws boundary conditions. Eight sub-models with changing orientations of the copper traces at outermost PCB pads were simulated applying both configurations. Based on previous investigations [8], the accumulated plastic strain in the copper trace between PCB pad and solder mask was applied as result criteria. Simulation results showed maximum plastic strain at the edge of the solder ball which was also the position of experimental copper trace cracks.

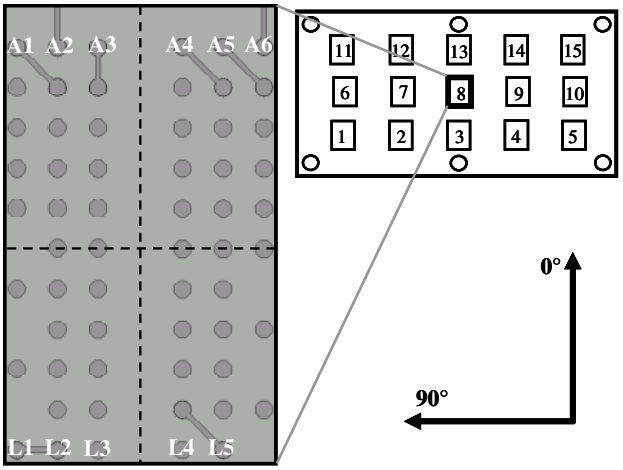


Figure 9: Sub-model orientation on the JEDEC board and experimental/initial PCB pad design

Figure 10 shows the effect of the copper trace routing direction at three interconnections of the TFBGA-60 package with global excitations from 6-screws boundary condition. The copper trace orientation has a big influence on the accumulated plastic strain. The difference between best and worst direction is as high as 77%! Highest strain appears when the copper trace is routed parallel to the short PCB edge leaving the package, which is the 0° orientation in row A and the 180° orientation in row L. This result proves the experimental failure observations. Strain reduces when the orientation is different and lowest strain is created when the copper traces point to the package center. According to the experimental routings, see fig. 9, highest strain, and thus a failure, can be found at the copper trace of interconnection A2 and A6. The orientations of interconnections A1 and L1 are quite safe. The plastic strains created in these traces are just 45% of the maximum possible load.

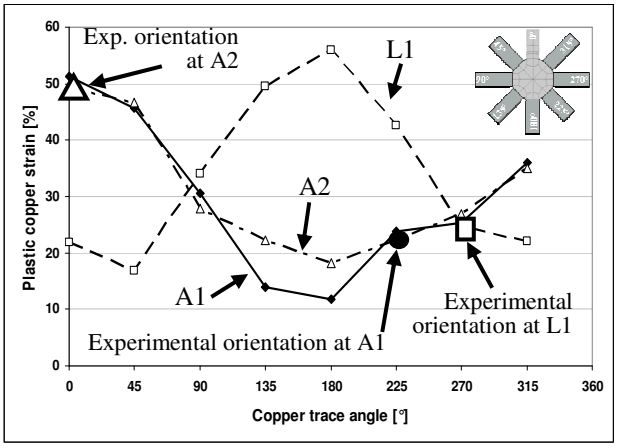


Figure 10: Effect of trace orientation on the plastic copper strain at interconnections A1, A2 & L1 with 6-screws boundary condition

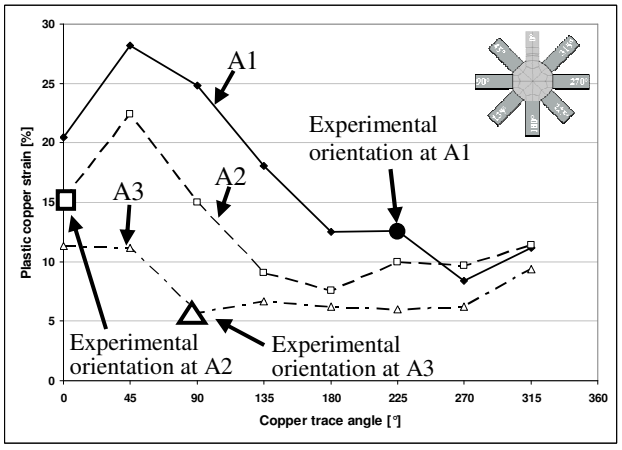


Figure 11: Effect of trace routing on the plastic copper strain at interconnections A1, A2 & A3 with 4-screws boundary condition

Result evaluation at all outermost interconnections shows a symmetrical routing effect. The relative strain distribution is very similar at all component edges. This way the investigation of the routing effect can be reduced to one quarter of the complete ball-out. E.g. the strain distribution at interconnections A4, A5 and A6 is shifted towards the upper left group (A1, A2, A3) by a reflection around the 0° orientation. The according distribution at row L can be derived by shifting each data point of the upper groups by 180°.

A different strain distribution can be found at component position #8 when the 4-screws boundary condition is applied, see figure 11. Still the copper trace routing clearly affects the resultant plastic strain. The difference between worst and best orientation reaches up to 70%! The maximum strain, however, occurs in 45° orientation at interconnections of the upper left group (A1, A2, A3). This is aligned with the first eigenmode of the JEDEC PCB under 4-screws boundary condition. In contrast to the distribution with 6-screws fixture copper strain at the outermost pad A1 is much higher than at adjacent interconnections. Failure should dominantly appear there. Based on experimental routing conditions highest strain occurs at interconnection A2, which was also the failure side. Evaluation of copper trace stress at all interconnections shows the same symmetry conditions in the package as compared to the 6-screws fixture.

Results of figure 10 and 11 are very different in magnitude. The maximum plastic strain created with 4-screws boundary condition reaches just half of the value produced with 6-screws fixture. The plastic strain in experimental routing configuration is even smaller. The maximum strain at interconnection A2 in 4-screws condition is only 30% of the value achieved in 6-screws configuration. This clear reduction of plastic strain results in a higher lifetime with 4-screws configuration which can be also seen in the Weibull plots of figure 3a.

Generally the deformation behavior of the JEDEC board with 6-screws fixture and its influence on the package stress is easier. Interconnections at the outermost rows with copper traces oriented in 0° or 180° direction have an equally high risk to fail. Any stress criteria produced at those interconnections has to be taken into account for lifetime modeling. Stress distribution at 4-screws boundary condition is more complex, due to the equal PCB deformation along length and width direction. The routing effect has to be investigated at each package position, which was not done so far. Simulation and experimental results gained with 4-screws boundary condition can not be applied for further result criteria assessment.

Result criteria assessment on the experimental sequence of failure

A reliable and practical lifetime model has to be applicable on the entire JEDEC board or any other drop test setup. Hence, the simulation result criteria applied for this purpose have to identify the different stress levels of the assembled components on the specific module under investigation correctly. Thus a suited criterion should be able to qualitatively predict the correct sequence of failing components.

Numerous criteria might be evaluated for this purpose, which can be gained in different publications. Due to the type of failure, the result criterion has to be extractable from each single interconnection of the coarse global model which reduces the amount of criteria to continuum mechanics.

Possible result criteria are the plastic strain in a solder element, ε_p, [13, 14], the plastic strain rate of a solder element, $\dot{\varepsilon}_{pl}$, [15, 16], the resultant force at the solder ball PCB interface, F, [17], the first principal stress in solder, σ_1, [3, 18, 19], the van-Mises-stress in the solder, σ_{EQV}, [20], and mechanical energy dissipated in an interconnection, W [17, 21].

The evaluation of four criteria is presented in figure 12. The evaluated criteria are plastic strain ε_p, plastic strain-rate $\dot{\varepsilon}_{pl}$, resultant force F and the new energy criterion SEND, equation (1)

$$SEND = \int \dot{\varepsilon}_{pl} \cdot \sigma_{Pad}\, dt \qquad (1),$$

which is a combination of the strain-rate $\dot{\varepsilon}_{pl}$ and the PCB-pad stress σ_{Pad}. Since all criteria represent a load the lifetime model should follow an inverse power law. Thus a suited criterion has to deliver monotonously declining values for components failing later.

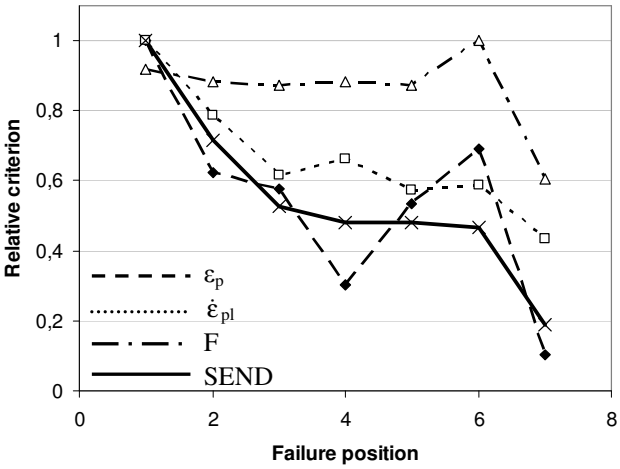


Figure 12: Evaluation of failure criteria

The results presented in figure 12 were gained for a Jedec board with VFBGA-90 packages at interconnections with critical copper trace routing, table 2. The criteria assessment was done by comparison of experimental failure position with the relative value of each criterion at these specific package positions, see tab.2. Except the resultant force, all criteria are able to identify the most critical component position (#8) correctly. In further progression, however, the plastic strain and plastic strain-rate also fail, identifying a component position as too critical. Only the criterion SEND keeps a monotonously declining progress for all 7 component positions, which would not result in any misleading failure sequence. Thus SEND is the criterion in charge.

A lifetime model for the Jedec drop test

The evaluation of the result criterion SEND was continued to the other experimentally tested packages VFBGA-60 and TFBGA-60, tab.1, based on global model simulations. Following the outcome of the copper trace routing investigation, energy values were extracted only from those interconnections with copper traces pointing in 0° or 180° direction. Additionally, the criterion assessment was extended from qualitative to quantitative manner. The values of SEND for each package type and position, respectively, were fitted to the according characteristic cycles-to-failure (N_{63}-values) by an inverse power relation, equ. 2,

$$N_{63} = C_1 / (\mathrm{SEND})^{C_2} \qquad (3).$$

The quality of the lifetime model, which is based on equation 3, is shown in figure 13.

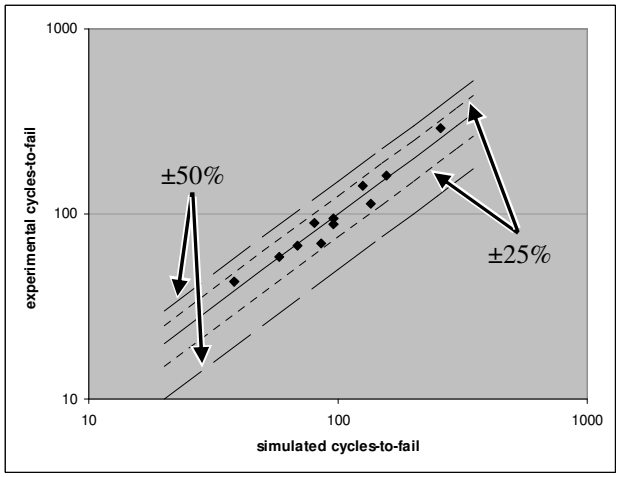


Figure 13: Results of drop test lifetime modeling

Predicted lifetimes are very close to the characteristic cycles-to-failure from experiments. The deviation between both values is less than ±25%, which is just half of the requested accuracy of ±50%. The assessment of each single data point proves the observed difference between prediction and experiment to be well with the experimental scatter. The results gained this way are absolutely sufficient. So, the new criterion SEND delivers trustworthy results for all investigated packages having different geometries and ball-outs. The high prediction accuracy proves the global model mesh density as well as material model assumptions to be adequate for high level lifetime modeling. The criterion SEND is a robust method to assess the lifetime of 2nd-level assemblies under drop test conditions.

Conclusion

By combining experiments, failure analysis, and numerical simulation, a new effect on the drop test performance of BGA assemblies has been identified. So far, the failure mode copper trace crack has rarely been reported and investigated.

Detailed failure analysis has shown that the appearance of copper trace fractures strongly depends on the copper trace orientation on the PCB. In contrast to typically seen IMC cracks, trace fractures may occur at any peripheral joint of the BGA package, if its trace points into the direction of highest PCB deformation. This effect was clearly seen in case of 6-screws clamping of the JEDEC board. Here, a critical orientation of the traces dramatically lowered the number of cycles-to-failure at any outer joint. In the specific case, the trace fracture occurred at the joint next to the corner. Hence, the effect of copper trace orientation has outbalanced the distribution of solder load, which always is highest in the corner

joints. In case of 4-screw clamping, this outbalancing was not seen in the experiments.

A two steps sub-model approach was applied to simulate the experimental observations. It revealed the root causes of the experimental findings. In 6-screws configuration, the JEDEC board induces large plastic strain into the copper traces. The worst case occurs when the trace is oriented parallel to the short edges of the board, which is the direction of highest PCB deformation. Then, very high loads are similarly created in the copper traces at all outer joints, so that any of them may fail first. In case of a 4-screws clamping, the plastic strain induced into the copper traces is generally smaller and the critical orientation is shifted according to the changed PCB deformation. The stress created in the solder of the corner joints is about twice as high as in the adjacent interconnections. Obviously, the level of trace load cannot outbalance this stress concentration when the JEDEC board is clamped by 4-screws configuration while the higher trace load level in the 6-screws configuration is able to do so.

Based on these results, a lifetime model was derived and successfully applied to the result of 6-screws boundary condition. The results gained with global models for 3 different package types had a deviation from the experimental cycles-to-failure of less than ±25%. This is well within the experimental scatter and smaller than the initial target of ±50%. The investigation presented here sets the first step towards virtual prototyping of BGA packages under drop test conditions.

Acknowledgement

Major parts of this work were conducted at the Back-end Development Center of Qimonda Dresden. The authors would like to thank their former team mates for the great support.

References

1. JEDEC Standard JESD22-B111, Board Level Drop Test Method of Components for Handheld Electronic Products.
2. Zhou, T.; Derk, R.; Rahim, K.: Larger Array Fine Pitch Wafer Level Package Drop Test Reliability. Proceedings of ASME 2009 InterPACK Conference.
3. Bentata, Y.; Forster, S.; Goh, K.Y.: Study of JEDEC B-condition JESD22-B111 Standard for Drop Test Reliability of Chip Scale Packages. Proceedings of 9th EuroSimE, p. 261 – 268.
4. Wong, E.H.; Seah, S.K.W.; van Driel, W.D.: Recent Advances in Drop-Impact Reliability. Proceedings of 9th EuroSimE, p. 550 – 558.
5. Tee, T.Y.; Ng, H.S.; Syed, A: Design for Board Trace Reliability of WLCSP under Drop Test. Proceedings of 10th EuroSimE 2009, p. 217 – 224.
6. Agrawal, A.; Levo, T.; Pitarresi, J.: Board Level Energy Correlation and Interconnection Reliability Modeling under Drop Impact. Proceedings of 59th ECTC 2009, p. 1694 – 1702.
7. Lall, P.; Shantaram, S.; Angral, A.: Explicit Submodeling and Digital Image Correlation Based Life-Prediction of Leadfree Electronics under Shock-Impact. Proceedings of 59th ECTC 2009, p. 542 – 555.
8. Kramer, F.; Rzepka, S.; Lienig, J.: Lifetime Modeling for Jedec Drop Tests. Proceedings of 10th EuroSimE 2009, p. 309 – 317.
9. Livermore Software Technology Corporation: LS-DYNA Keyword User's Manual. May 2007, Version 971. www.lstc.com
10. Rzepka, S; Kramer, F.; Grassmé, O.: A Multilayer PCB Material Modeling Approach Based on Laminate Theory. Proceedings of 9th EuroSimE 2008, p. 234–43
11. Tsai; Hahn: Introduction to Composite Material, 1980. Technomic Publishing Company, Inc.
12. Long, X.; Dutta, I.; Sarihan, V.: Deformation behavior of Sn-3.8Ag-0.7Cu Solder at Intermediate Strain-Rates: Effect of Microstructure and Test Conditions. Journal of Electronic Materials, Vol. 37, No. 2, 2008, p. 189 – 200.
13. Lall, P.: Computational Methods and High Speed Imaging Methodologies for Transient Shock Reliability of Electronics. Proceedings of 8th EuroSimE 2007, p. 1 - 13.
14. Syed, A.; Lin, W.; Sohn, E.S.: Plastic Deformation and Life Prediction of Solder Joints for Mechanical Shock and Drop/Impact Loading Conditions. Proceedings of 57th ECTC 2007, p. 507 – 514.
15. Yeh, C.L.; Lai, Y.S.: Strain-rate and Impact Velocity Effects on Joint Adhesion Strength. Proceedings of ICEPT-HDP 2008.
16. Pang, J.; Che, F.X.: Drop Impact Analysis of Sn-Ag-Cu Solder Joints Using Dynamic High-Strain Rate Plastic Strain as the Impact Damage Driving Force. Proceedings of 56th ECTC 2006, p. 49 – 54.
17. Song, F.; Lee, R.; Clark, S.: Characterization of Failure Modes and Analysis of Joint Strength Using Various Conditions for High Speed Solder Ball Shear and Cold Ball Pull Tests. ECTC 2007.
18. Syed, A.; Kim, S.M.; Lin, W.: A Methodology for Drop Performance Prediciton and Application for Design Optimization of Chip Scale Packages. Proceedings of 55th ECTC 2005, p. 472 – 479.
19. Wen, L.; Fu, X.; Zhou, J.: Dynamic Properties Testing of Solders and Modeling of Electronic Packages Subjected to Drop Impact. ICEPT-HDP 2008.
20. Chou, C-Y.; Hung, T-Y.; Yew, M-C.: Investigation of Stress-buffer-enhanced Package Subjected to Board-Level Drop Test. Proceedings of 9th EuroSimE, p. 372 – 377.
21. Song, F.; Lee, R.; Newman, K.: Effect of Thermal Aging on High Speed Ball Shear and Pull Tests of SnAgCu Lead-free Solder Balls. ECTC 2007.