

# Electromigration and Its Impact on Physical Design in Future Technologies

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## ABSTRACT

Electromigration (EM) is one of the key concerns going forward for interconnect reliability in integrated circuit (IC) design. Although analog designers have been aware of the EM problem for some time, digital circuits are also being affected now. This talk addresses basic design issues and their effects on electromigration during interconnect physical design. The intention is to increase current density limits in the interconnect by adopting electromigration-inhibiting measures, such as short-length and reservoir effects. Exploitation of these effects at the layout stage can provide partial relief of EM concerns in IC design flows in future.

## Categories and Subject Descriptors

B7.2[Integrated Circuits]: Design Aids

## Keywords

Electromigration; current density; physical design; layout; interconnect reliability; short-line rules; short-length effects; Blech length; reservoir effect

## 1. INTRODUCTION

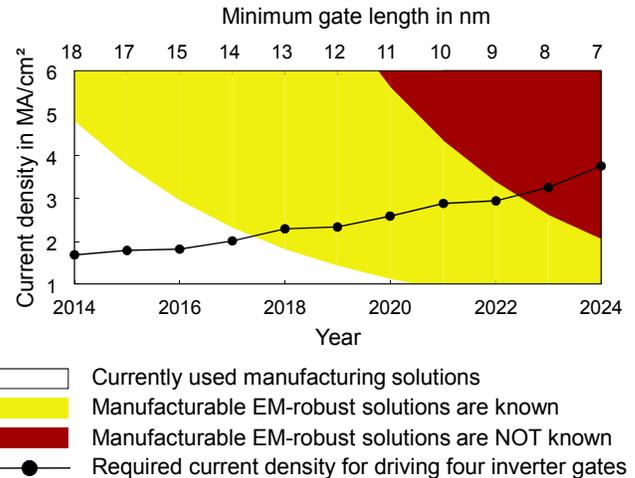
Excessive current density within interconnects – which if not effectively mitigated causes electromigration (EM) and electrical overstress – is a major concern for integrated circuit (IC) designers. This is a growing reliability issue in modern ICs in the wake of smaller feature sizes. Analog designers have been aware of this issue for some time, and digital designs are now being affected as well. The latest edition of the ITRS roadmap [18] predicts that all minimum-sized interconnects will be EM-affected by 2018, potentially restricting any further downscaling of wire sizes (Figure 1).

Current density verification and thus the detection of electromigration issues are already an integral part of the sign-off verification of circuit layouts. Current density violations detected during sign-off are corrected by layout modifications – by the widening of wires, for example.

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**Figure 1. Expected evolution of required and maximum IC wires (ITRS [18]). While the required current density scales with frequency and reducing cross-section, the maximum tolerable current density is shrinking due to smaller structure sizes (see Section 4).**

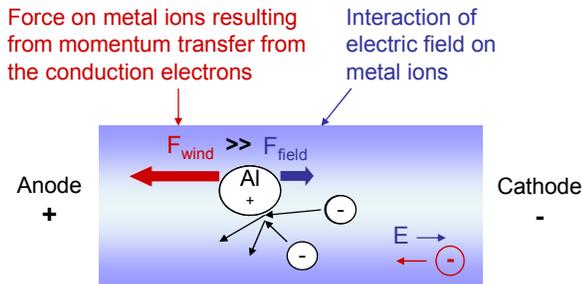
The number of late corrections needs to be capped going forward due to the restrictions imposed by complex circuitry. This can be achieved by adopting electromigration inhibiting measures, such as short-length and reservoir effects, during physical IC design to maximize current density limits. However, we need to understand the physical processes involved, and the constraints and benefits of the EM-inhibiting effects in order to successfully implement them.

In this talk we present the options available to combat the negative effects of electromigration during layout design. In Section 2 we introduce the physical process of electromigration, followed by a survey of how current density is considered in today's analog and digital design flows (Section 3). Section 4 investigates future technology nodes and their effects on current density and electromigration issues in IC layout. Section 5 presents various EM-inhibiting effects that can be exploited in current and future technologies in order to reduce the negative impact of electromigration on the circuit's reliability.

## 2. ELECTROMIGRATION (EM)

Current flow through a conductor produces two forces to which the individual metal ions in the conductor are exposed. The first is an electrostatic force  $F_{field}$  caused by the electric field strength in the metallic interconnect. Since the positive metal ions are

shielded to some extent by the negative electrons in the conductor, this force can be ignored in most cases. The second force  $F_{wind}$  is generated by the momentum transfer between conduction electrons and metal ions in the crystal lattice. This force acts in the direction of the current flow and is the main cause of electromigration (Figure 2).



**Figure 2. Two forces act on metal ions which make up the lattice of the interconnect material. Electromigration is the result of the dominant force, that is, the momentum transfer from the electrons which move in the applied electric field.**

In a homogeneous crystalline structure, because of the uniform lattice structure of the metal ions, there is hardly any momentum transfer between the conduction electrons and the metal ions. However, as this symmetry does not exist at grain boundaries and material interfaces, momentum is transferred much more vigorously in these zones from the conductor electrons to the metal ions. And since the metal ions in these zones are bonded much more weakly than in a regular crystal lattice, once the electron wind has reached a certain strength, atoms become separated from the grain boundaries and are transported in the direction of the current. This direction is also influenced by the grain boundary itself, as atoms tend to move along grain boundaries.

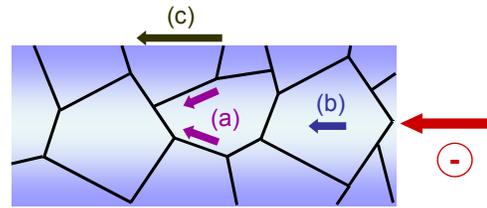
If the direction of an excessive current is kept constant for a longer period, voids and hillocks appear in the wire. Analog circuits, or power supply lines in digital circuits, are thus particularly susceptible to electromigration. When the current direction varies – for example, in digital circuits with their alternating capacitive charging and discharging in conductors – there is a certain amount of compensation due to material backflow (self-healing effect). Nonetheless, interconnect failures are still possible, with thermal migration playing a major role.

Furthermore, the susceptibility of wires to electromigration is a function of grain size and thus of the distribution of grain sizes. Smaller grains encourage material transport, because there are more transport channels than in coarse-grained material. This causes voids to appear at the points of transition from coarse to fine grains, since at these points atoms flow out faster than they flow in. Conversely, where the structure turns from fine grains to coarse, hillocks tend to form, since the inflowing atoms cannot disperse fast enough through the coarse structure.

These types of variations in grain size appear in interconnects at every contact hole or via. Because the current here commonly encounters a narrowing of the conductive pathway, contacts and vias are particularly susceptible to electromigration.

Diffusion processes caused by electromigration can be divided into grain boundary diffusion, bulk diffusion and surface diffusion (Figure 3). In general, grain boundary diffusion is the major

migration process in aluminum wires [33][34], whereas surface diffusion predominates in copper interconnects [9][10][26][40].



**Figure 3. Illustration of various diffusion processes within the lattice of an interconnect: (a) grain boundary diffusion, (b) bulk diffusion, and (c) surface diffusion.**

Detailed investigations of the various electromigration failure mechanisms can be found in [4][9][34][42].

Many electronic interconnects, for example in integrated circuits, have an intended mean time to failure (MTTF) of at least 10 years. The failure of a single interconnect caused by electromigration can result in the failure of the entire circuit. At the end of the 1960s the physicist J. R. Black developed an empirical model to estimate the MTTF of a wire segment, taking electromigration into consideration [3]:

$$MTTF = \frac{A}{J^n} \cdot \exp\left(\frac{E_a}{k \cdot T}\right) \quad (1)$$

where  $A$  is a constant based on the cross-sectional area of the interconnect,  $J$  is the current density,  $E_a$  is the activation energy (for example,  $0.7 eV$  for grain boundary diffusion in Al [3][42],  $0.9 eV$  for surface diffusion in Cu [17]),  $k$  is the Boltzmann constant,  $T$  is the temperature and  $n$  a scaling factor. It has been established through studies on Al and Cu interconnects that void-growth-limited failure is characterized by  $n=1$ , while void-nucleation-limited failure is best represented by  $n=2$  [9][24].

Equation (1) shows that current density  $J$  and (to a lesser extent) the temperature  $T$  are deciding factors in the physical design process that affect electromigration.

### 3. CONSIDERATION OF EM IN TODAY'S PHYSICAL DESIGN FLOWS

#### 3.1 Analog Design

Current strengths in analog circuits vary widely depending on the application: sensor applications require only a few nano-amps, whereas wires in power circuitries need to carry up to several amps continuously. In addition to this broad spectrum of currents, analog circuits may have to operate reliably at very high temperatures. The number of nets in circuits prone to electromigration is growing due to technology downscaling and increasingly complex designs. Issues arising from the joule heating of conductors need to be addressed for the same reasons. Yet another characteristic of analog circuits is that currents in power and signal nets are on the same order of magnitude. Hence, analog designers have been aware of electromigration issues for the past couple of years.

A proprietary design flow that incorporates the comprehensive consideration of current density in analog IC design is presented in [28] (Figure 4). It includes current characterization, current propagation in design hierarchies, current-aware layout Pcells,

current-aware route planning [27] as well as current density verification [19][20].

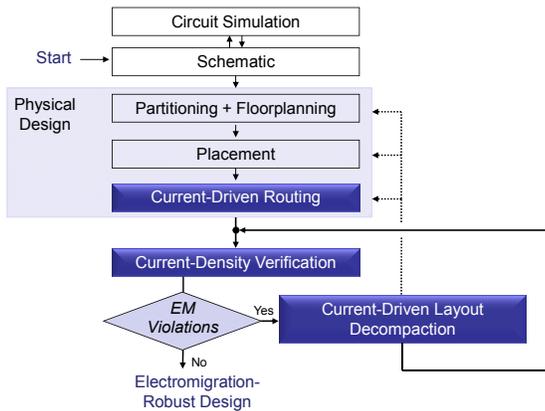


Figure 4. An electromigration-aware analog design flow [28].

Extensive manual intervention in commercial synthesis tools has been needed up to now in order to include the impact of current densities in physical design. A first current-density-aware routing tool has been available from Pulsic Ltd. [12]. It widens wires based on terminal currents. It is however restricted to direct currents (DC).

Verification tools for current densities, such as Cadence Virtuoso Power Systems [13], Synopsys CustomSim [15] and Apache Totem MMX [14], have been available for some time. They extract a netlist from the layout (including parasitics). This netlist is then used to simulate the currents in all wires. If any of the resulting current densities exceed an EM-relevant boundary, a violation is detected and highlighted.

### 3.2 Digital Design

Digital circuits are characterized by net classes that exhibit different susceptibilities to electromigration [30]. We can assume that power nets carry moderately constant currents and that their current directions are consistent. Clock and signal nets, on the other hand, conduct alternating currents (AC). Due to self-healing mechanisms, these alternating currents affect wire lifetimes less than direct currents [29][32]. Thus, the different net classes of digital circuits require different current density limits. Beyond that, digital circuits stand out because of their large number of nets. The complexity of analog circuits does not exceed a few thousand nets, whereas digital circuits typically have millions of them.

Methods employed in analog design to deal with electromigration cannot be applied in digital circuits – other solutions, which can handle the complexity of digital designs, are needed.

In principle, the digital design flow consists of a series of synthesis steps, which methodically concretize circuit geometry (Figure 5a) [23]. Simultaneously, verification steps ensure the circuit acquires the required electrical characteristics and functions, and meets the reliability and manufacturability criteria (Figure 5b).

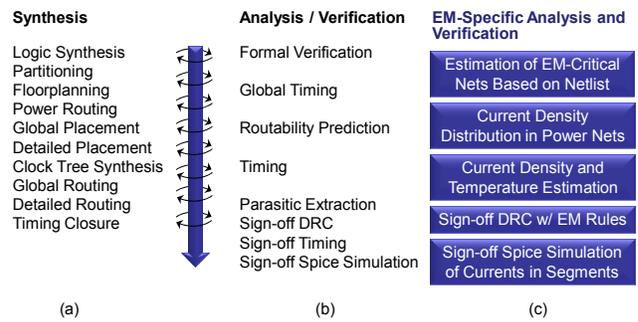


Figure 5. Synthesis-analysis loops in the design flow for digital circuits. The critical steps – physical synthesis (a) and analysis (b) – are shown, supplemented by options to address current density and other electromigration issues (c).

Figure 5c shows flow options to analyze the impact of electromigration on circuit reliability. These have only been partly supported to date by layout tools. However, “Sign-off DRC w/ EM-rules” and “Sign-off Spice Simulation” with subsequent current density verification are now standard functions in state-of-the-art digital layout tools (for example, Synopsys IC Compiler, Cadence Encounter). These functions are also available as stand-alone verification tools (for example, Apache Totem MMX, Mentor Calibre PERC, Tanner HiPerVerify).

An early stage “Estimation of EM-Critical Nets” is presented in [21]. It determines the worst-case bounds on segment currents, so nets can be separated into critical and non-critical sets. Only the set of critical nets, which is typically considerably smaller, requires subsequent special consideration during layout generation.

The “inner workings” of the aforementioned analysis steps are almost identical in the tools. They are based on three global current density limits to identify EM violations: maximum allowable peak, average, and RMS current densities. The actual current density value in each wire segment is determined by transient or steady state Spice simulations at transistor level. EM violations are detected if these actual local current densities exceed a specific limit. Power and signal nets are verified separately.

## 4. EM IN FUTURE TECHNOLOGIES

The global trend in size reduction leads to improved circuit performance, efficiency at higher circuit frequencies and smaller footprints. Line widths will continue to decrease over time, as will wire cross-sectional areas. As shown in Table 1, the cross-sectional area shrinks from about 1,000 nm<sup>2</sup> in 2014 to less than 500 nm<sup>2</sup> in 2018. Currents are also reduced (see Table 1 and Figure 6, left) due to lower supply voltages and shrinking gate capacitances. However, as current reduction is constrained by increasing frequencies, the more marked decrease in cross-sectional areas (compared to current reduction) will give rise to increased current densities  $J$  in ICs going forward (Figure 6, right).

To make matters worse, the maximum tolerable current densities are shrinking at the same time due to smaller structure sizes<sup>1</sup> [17]. As a result, the ITRS [18] indicates that all minimum-sized interconnects

<sup>1</sup> Small voids and other material defects, which could have been tolerated in earlier technology nodes, cause increasingly dramatic damage or resistance change to the wires with shrinking metal structures. Thus, maximum tolerable current densities will have to decrease in order to maintain reasonable interconnect reliability.

will be EM-affected by 2018, potentially limiting any further downscaling of wire sizes (Figure 6, yellow barrier).

Furthermore, the total length of interconnect per IC will continue to increase. As a consequence, reliability requirements per length unit of the wires need to *increase* in order to *maintain* overall IC reliability. This accepted wisdom is contradicted by the future *decrease* in interconnect reliability due to electromigration – as noted above. The ITRS thus states that no known solutions are available for the EM-related reliability requirements that we will face approximately 10 years from now (Figure 6, red barrier).

**Table 1. Predicted technology parameters based on the ITRS, 2011 edition [18]; maximum currents and current densities for copper at 105°C.**

Year	2014	2016	2018	2020	2022	2024	2026
Gate length (nm)	18.41	15.34	12.78	10.65	8.88	7.40	6.16
On-chip local clock frequency (GHz)	4.211	4.555	4.927	5.329	5.764	6.234	6.743
DC equivalent maximum current ( $\mu\text{A}$ )*	18.14	12.96	10.33	7.36	5.53	4.45	3.52
<b>Metal 1 properties</b>							
Width – half-pitch (nm)	23.84	18.92	15.02	11.92	9.46	7.51	5.96
Aspect ratio	1.9	2.0	2.0	2.0	2.1	2.1	2.2
Layer thickness (nm)*	45.29	37.84	30.03	23.84	19.87	15.77	13.11
Cross-sectional area ( $\text{nm}^2$ )*	1,079.7	716.0	451.0	284.1	187.9	118.4	78.13
<b>DC equivalent current densities (<math>\text{MA}/\text{cm}^2</math>)</b>							
Maximum tolerable current density (w/o EM degradation)**	4.8	3.0	1.8	1.1	0.7	0.4	0.3
Maximum current density (solutions unknown)**	25.4	15.4	9.3	5.6	3.4	2.1	1.2
Required current density for driving four inverter gates	1.68	1.81	2.29	2.59	2.94	3.76	4.50

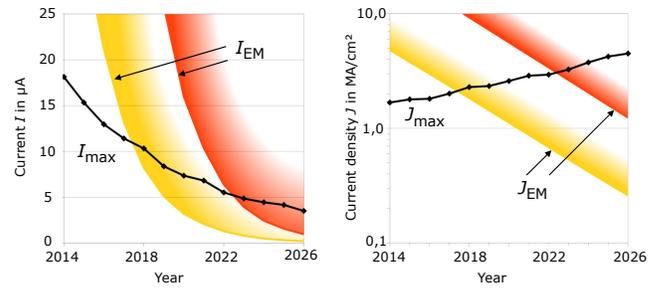
\*) Calculated values, based on given width  $W$ , aspect ratio  $A/R$ , and current density  $J$  in [18], calculated as follows: layer thickness  $T = A/R \times W$ , cross-sectional area  $A = W \times T$  and current  $I = J \times A$ .

\*\*\*) Approximated values from the ITRS figure INTC9 [18].

All remaining values are from the ITRS 2011 edition [18].

Increased interconnect resistivity caused by scattering effects in small wires will throw up further challenges [36]. Coupled with a rise in current densities, this will lead to large local temperature gradients inside the wire caused by Joule heating. It accelerates temperature-dependent electromigration and introduces additional thermomigration [22][43].

The tendency to replace  $\text{SiO}_2$  with low-k dielectrics [18] with less stiffness reduces the stress-induced atomic backflow [39], which counteracts electromigration in short lines (see Section 5.2). Another consequence of this replacement is the increased likelihood of EM-induced compressive failures (extrusions) [41].



**Figure 6. Expected development of currents ( $I_{\max}$ , left) and current densities ( $J_{\max}$ , right) needed for driving four inverter gates, according to ITRS 2011 [18] (see also Table 1). EM degradation needs to be considered when crossing the yellow barrier of currents ( $I_{\text{EM}}$ ) and current densities ( $J_{\text{EM}}$ ). As of now, manufacturable solutions are not known in the red area.**

As already mentioned, the surge in current density is also driven by an increase in clock frequencies (Table 1), in response to the demand for enhanced performance and made possible by smaller transistors. Although higher frequencies will neither worsen nor improve electromigration issues in signal or clock nets ([38], see also Section 5.7), they will increase currents (and thus current densities) in (DC) supply nets which are already sensitive to electromigration in today’s technologies.

## 5. ADDRESSING EM IN PHYSICAL DESIGN: WHAT ARE THE OPTIONS?

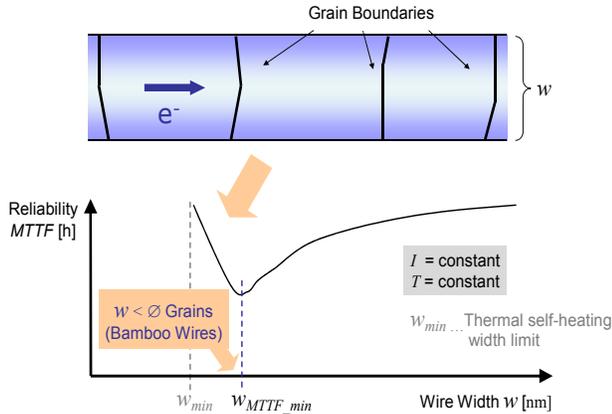
There are a number of well-known options for influencing electromigration and current density, respectively, during the physical design of an electronic circuit.

- **Wire material:** It is known that pure copper used for Cu-metallization is more electromigration-robust than aluminum at low operating temperatures.
- **Wire temperature:** In Equation (1), the temperature of the conductor appears in the exponent, that is, it strongly impacts the MTF of the interconnect. For an interconnect to remain reliable at high temperatures, the maximum tolerable current density of the conductor must necessarily decrease. On the other hand, lowering the temperature supports higher current densities while keeping the reliability of the wire constant.
- **Wire width:** Given that current density is the ratio of current  $I$  and cross-sectional area  $A$ , and given that most process technologies assume a constant thickness of the printed interconnects, it is the wire width that exerts a direct influence on current density: the wider the wire, the smaller the current density and the greater the resistance to electromigration.

These effects have been covered in detail in [28]. They will be of limited use in new generation technologies because they have been largely exploited and/or their application would be counter-intuitive to the new technology node itself, that is, its reduced structure size. Hence, tolerable current density limits need to be maximized by exploiting further electromigration inhibiting factors which are described next.

## 5.1 Bamboo Structure

If the wire width is reduced to below the average grain size of the wire material, the resistance to electromigration increases, despite an increase in current density. This apparent contradiction is caused by the grain boundary locations. In narrow wires, the grain boundary locations are perpendicular to the whole wire (as shown in Figure 7) forming a bamboo like structure. As already mentioned, material transport occurs as much in the direction of the current flow as along grain boundaries (grain boundary diffusion, see Section 2). Because grain boundaries in this type of bamboo structure are often perpendicular to the current flow, the boundary diffusion factor is demoted, and material transport is reduced accordingly.



**Figure 7. Reduced wire width – less than the average grain size – improves wire reliability with regard to electromigration. So-called bamboo wires are characterized by grain boundaries which are perpendicular to the direction of the electron wind and thus permit only limited grain boundary diffusion.**

The bamboo structure improves reliability if the self-heating limit of the layer is taken into account. In order to exploit this, wire widths are deliberately kept narrow enough to maintain a bamboo structure. Also the wire material can be annealed selectively during IC processing in order to support bamboo formation.

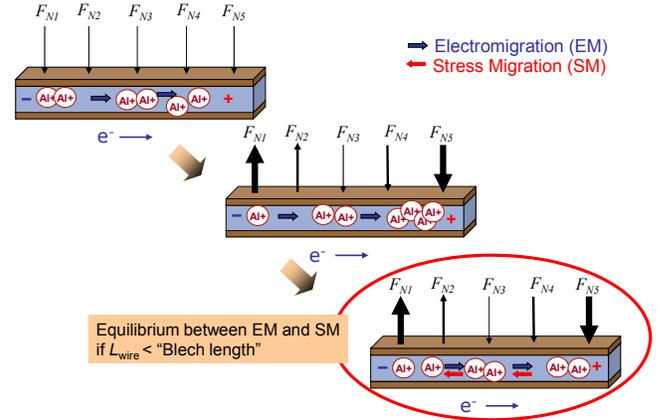
However, the maximum possible wire width for a bamboo structure, which is about 850 nm for damascene copper [2], is often too narrow for signal lines carrying large-magnitude currents in analog circuits or for power supply lines. In these circumstances, slotted wires – in which rectangular holes are carved – can be used. Here, the widths of the individual metal structures between the slots support bamboo formation, and the total width of all the metal structures meets power requirements.

Based on the same principle, a fine-grain power mesh is often superimposed on the circuit. This mesh consists of a large number of wires, and the individual wire widths form a bamboo-like structure.

It must be pointed out that process anomalies often produce variations in wire widths – due to etch loss, lithography issues, and the like – and variations in wire heights – due to metal deposition fluctuations, for example – as well as impacting the via fill rate. It is vital to take these possible process fluctuations into account when determining viable interconnect dimensions.

## 5.2 Short-Length Effects

There are also upper limits set on the length of an interconnect to block electromigration. One of them is known as the “Blech length,” and any wire that has a length below this threshold length (typically on the order of 5-50  $\mu\text{m}$ ) will not fail by electromigration. In this scenario, mechanical stress buildup causes a reverse migration process which reduces, or even compensates for, the effective material flow towards the anode (Figure 8).



**Figure 8. An illustration of stress migration caused by the mechanical stress buildup in a short wire. This reversed migration process essentially neutralizes the material flow due to electromigration.**

Specifically, a wiring segment is not susceptible to electromigration if the product of the segment’s current density  $J$  and the segment’s length  $L$  is less than a process-technology-dependent threshold value  $(JL)_{\text{Blech}}$  [4]. The critical product  $(JL)_{\text{Blech}}$ , often called the “Blech immortality condition,” is obtained from

$$(JL) < (JL)_{\text{Blech}} = \Omega \frac{\Delta\sigma}{z^* q \rho} \quad (2)$$

where  $\Omega$  is the atomic volume of the wire material ( $\text{cm}^3/\text{number}$ ),  $\Delta\sigma$  is the difference in the hydrostatic stress at both ends of the segment,  $z^*$  is the effective charge of the wire’s material (a measure of the momentum transfer from electrons to the ions of the wire’s material),  $q$  is the fundamental electronic charge ( $z^*q < 0$ ) and  $\rho$  is the density of the wiring material [39].

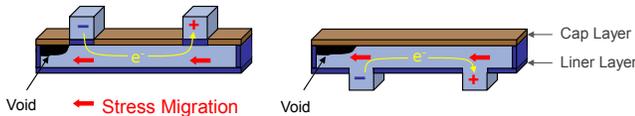
The Blech length can be increased by depositing (stiff) cap layers on top of the copper metal and by using dielectrics with a higher Young’s module (i.e., higher stiffness) because both support reverse stress migration. However, the cap layer also needs to suppress surface diffusion (see Section 5.6).

Besides the *Blech effect* or *Blech immortality condition* discussed above, there is another, related short-length effect. It is based on *void growth saturation* due to mechanical stress buildup. Void-related failures in wiring segments require the void to be grown to a critical size  $V_{\text{fail}}$ . Reverse stress migration in short segments, described above, can block void growth so that it cannot reach  $V_{\text{fail}}$  (Figure 9). Specifically, the void growth with its increase in resistance  $\Delta R$  does not reach the failure state marked by  $\Delta R_{\text{fail}}$ .

There is therefore a critical product  $(JL)_{\text{sat}}$  below which immortality is obtained due to void growth saturation, given by

$$(JL)_{\text{sat}} = \frac{\rho/A}{\rho_1/A_1} \cdot \frac{\Delta R_{\text{fail}}}{R} \cdot \frac{2\Omega \cdot B}{z^* q \rho} \quad (3)$$

where  $\rho/A$  and  $\rho_1/A_1$  are the ratio of resistivity to cross-sectional area of the wire material (Cu) and the liner, respectively, and  $R$  is the initial wire resistance [1][37][39]. The value  $B$  is the elastic bulk modulus for the material that surrounds the wiring segment [24].



**Figure 9. A stress gradient can also cause void growth saturation in short line via-above (left) and via-below configurations (right). Note the lesser impact of voids in a via-below configuration (right, see also Section 5.5).**

It is important to note that, only if  $(JL)_{\text{sat}} > (JL)_{\text{Blechs}}$ , immortality is obtained due to void growth saturation and the wire will not fail until the void size reaches  $V_{\text{fail}}$ . Furthermore,  $(JL)_{\text{sat}}$  is lower for via-above than via-below copper configurations (see Section 5.5 and Figure 9). It is also lower if a low-k (low-stiffness) dielectric is used instead of  $\text{SiO}_2$  [39]. Some of the values of the critical product  $(JL)$  for immortality obtained experimentally are, for example, 1,500 A/cm for Cu/ $\text{SiO}_2$  via-above segments [8], 3,700 A/cm for Cu/ $\text{SiO}_2$  via-below segments [25] and 375 A/cm for Cu/low-k via-above segments [7]. Assuming a current density  $J$  of  $5 \times 10^5$  A/cm<sup>2</sup>, the latter (low) value of 375 A/cm corresponds to a segment length of 7.5  $\mu\text{m}$ , while Cu/ $\text{SiO}_2$  via-below segments can have lengths of up to 74  $\mu\text{m}$ .

Exploiting the critical product  $(JL)$  for immortality, however, requires knowledge of the effects of *linked* segments. Specifically, the entire interconnect tree, which is the set of segments that are linked without diffusion barriers – that is, within one layer of metallization – needs to be included in the calculation [6][39]. Inactive segments require special attention because they can serve as reservoir sinks (see Section 5.3) [6].

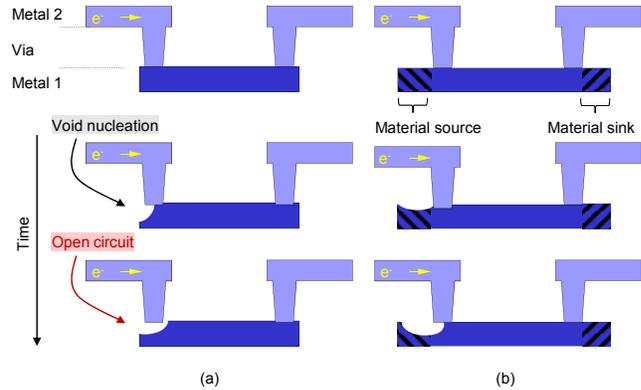
Starting with the 45 nm technology node, short-length effects can be exploited to deliberately generate EM-resistant wire segments during the routing step. This is particularly relevant for minimum-sized wires because they “automatically” become increasingly EM-resistant with shrinking feature sizes. Also, wires that are too long for short-length effects can be split into shorter, more EM-resistant segments by inserting vias. The downside is that vias are susceptible to electromigration, this must be considered at the same time (see Section 5.4).

### 5.3 Reservoir Effect

The so-called “reservoir effect” [31] can significantly improve the lifetime of multiple-level interconnects. Increased metal-via layer overlaps enlarge the amount of interconnect material at one of the prime points of EM failure: below, above and within the via. Reservoirs can act as sources that have to be drained before voids generated by electromigration become critical to the circuit. This

does not actually decrease the effects of electromigration itself, but prolongs the time to failure due to void growth.

Reservoirs that serve as a material source typically prolong lifetimes, and reservoirs that act as dominant sinks for migrated interconnect material can degrade lifetimes. Whether a reservoir acts as sink or source depends on the direction of current flow (Figure 10).



**Figure 10. The reservoir effect in (b) extends the lifetime of the via configuration compared to a regular via without layer overlaps (a).**

The reservoir effect needs to be considered in conjunction with short-length effects because any sink effectively increases the wire length and thus reduces any possible stress buildup. Consequently, the reservoir effect is most effectively used for nets with known, directed currents because, in this case, reservoirs acting as sources prolong time to failure and sinks can be deliberately avoided.

The reservoir effect is also leveraged by using multiple vias (see Section 5.4) since via arrays have a larger reservoir area than a single via. Experimental results in [31] indicate that the prolonged lifetime achieved is more a result of the increased reservoir area than of current sharing between vias.

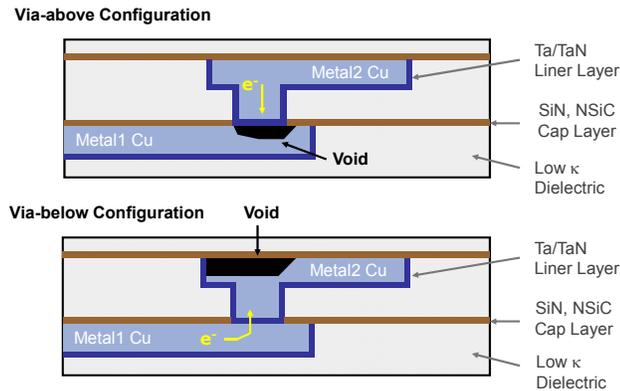
### 5.4 Double/Multiple Vias

Particular attention needs to be paid to vias and contact holes, because generally the ampacity of a (tungsten) via is less than that of a metal wire of the same width. Moreover, migration velocities in the via material, the diffusion barrier and the metal wire differ. Hence, vias are one of the prime points of void nucleation and thus EM failure. To compensate for this increased vulnerability and to address typical manufacturing and yield issues, double or multiple vias are often deployed. The via array geometry is crucial here: multiple vias need to be arranged so that the resulting current flow and thus EM degradation is distributed as evenly as possible throughout the parallel vias [28].

### 5.5 Via-Above and Via-Below Configuration

The generation of voids in the vicinity of vias is strongly influenced by the geometry of the via configuration. Depending on whether a specific wire segment is connected from above or below, the configuration is called *via-above* or *via-below*, respectively. As described above, via stacks are prone to void nucleation because of the predominance of interface/surface diffusion in copper interconnects and different electromigration drift velocities. Although this drift velocity is low in the diffusion

barrier, it is higher in the adjacent copper wire and tungsten via. Consequently, electrons passing through the diffusion barrier can cause voids in the material behind the barrier. The impact of excessive current density is a function of the geometry, and can cause a variety of damage [5][39]. Figure 11 shows that even a low-volume void causes a failure if placed directly underneath the via, whereas a void in a via-below configuration has to grow larger before the interconnect is destroyed.



**Figure 11. Via-above and via-below configurations with their different damage locations partly due to the interface/surface diffusion prevalent in copper wires.**

## 5.6 Surface Coating / Metal Capping

As mentioned in Section 2, the Cu/cap layer interface is the dominant diffusion path for electromigration in submicron copper interconnects. Electromigration studies in copper line structures show that mass transport is dominated by diffusion at the Cu/cap layer interface, probably due to the presence of defects (voids) induced by the chemical mechanical polish (CMP) process prior to cap deposition [11][35]. The effect of a dielectric capping layer on interfacial mass transport for copper interconnects can therefore be exploited. For that purpose cap layers which increase activation energies at the interface and which provide a high degree of stiffness (see Section 5.2) will improve EM resistance. For example, Hu et al. [16] demonstrated a significant improvement in EM lifetime by coating the Cu surface with a thin 10-nm electroless layer of CoWP.

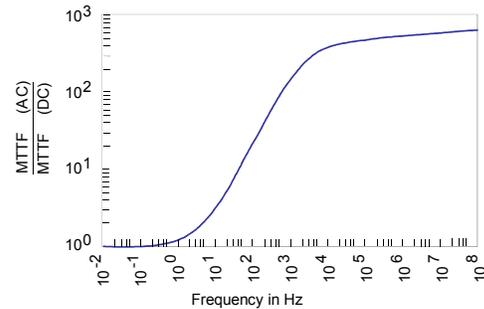
## 5.7 Frequency Dependency

The lifetime of a wire carrying alternating currents (AC) is significantly longer than that of a wire with direct currents (DC), due to damage-healing effects (Figure 12). Material migrating in one direction can partially migrate back to its original location under beneficial conditions. Consequently, the interconnect suffers less damage from electromigration under AC conditions. Experiments in [38] reveal that the effect of self-healing becomes noticeable above 10 Hz and increases with the switching frequency up to about 10 kHz where it reaches a saturation value. There is no improvement in circuit durability at frequencies above this point.

Tao et al. [38] report that AC lifetime at high frequencies is typically over 1,000 times longer for Al-2% Si and Al-4% Cu and over 500 times longer for Cu interconnects.

As a consequence, two different sets of maximum allowable current densities are commonly used in practical current-density

verification, one for signal nets with frequencies above 10 kHz and one for the remaining (DC) nets, such as power supply lines.



**Figure 12. Mean time to failure (MTTF) if interconnect is stressed by an alternating current (AC) compared to MTTF if a directed current (DC) is applied [38].**

## 6. OUTLOOK

Electromigration (EM) is becoming an increasingly difficult design challenge due to higher interconnect current densities. The on-going trend in IC downscaling is producing physical designs with ever-smaller feature sizes, which can easily give rise to current densities that exceed their maximum allowable value.

In order to address this problem during layout synthesis, this talk has focused on basic design issues that affect electromigration during interconnect physical design. The aim is to increase current density limits in the interconnect by utilizing electromigration-inhibiting measures, such as short-length and reservoir effects. Exploitation of these effects at the layout stage provides partial relief of EM concerns in today's design flows.

In order to use these effects in next generation design flows, we propose establishing a dependence between the applied current density limits on the specific circuit geometry and the application's mission profile. Design tools can significantly improve the EM robustness of the generated layout by utilizing EM-optimized layout configurations as constraints during synthesis steps, such as routing. We believe that this inclusion of EM-specific requirements in the physical design can provide relief from severe reliability constraints in future technologies.

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