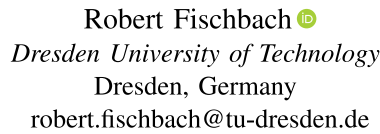
Design for Manufacturing and Assembly for Heterogeneous Integration Using Micro-Transfer Printing

Robert Fischbach 
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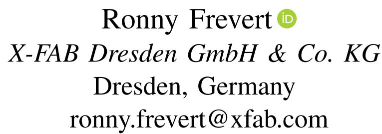
Ronny Frevert 
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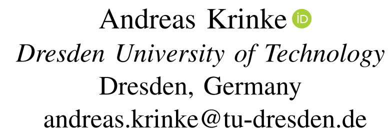
Andreas Krinke 
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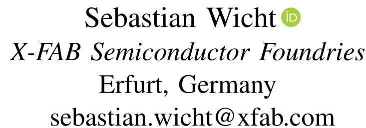
Sebastian Wicht 
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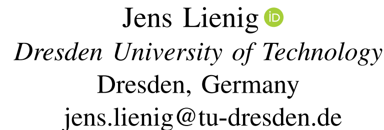
Jens Lienig 
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***Abstract*—Micro-transfer printing (µTP) enables heterogeneous integration of different semiconductor technologies, offering high flexibility for next-generation electronic systems. However, transitioning µTP from research demonstrations to mass production requires systematic design methodologies that address unique fabrication constraints absent in conventional integrated circuit (IC) design flows. Unlike traditional chip design, µTP introduces interrelated design decisions that span die-level layout, wafer-level planning, and packaging considerations, requiring specialized approaches and tools. This paper presents a comprehensive design methodology for µTP-based heterogeneous integration. Our methodology covers the entire design flow from initial wafer planning to layout implementation, explicitly considering the process constraints of µTP. Supported by a representative design example, this work offers chip and packaging designers a practical introduction to manufacturable µTP design, substantially minimizing the need for iterative refinement.**

***Index Terms*—Heterogeneous Integration, Micro-Transfer Printing, EDA, Design Methodology, VLSI, Chip Design**

I. Introduction

Modern electronic systems increasingly demand heterogeneous integration of different semiconductor technologies, e.g., to combine high-performance logic with specialized RF, photonic, or other sensor components. Monolithic integration approaches face fundamental constraints such as process incompatibilities between technologies, yield degradation with increasing chip area, inflexible IP integration requiring full process commitment, and high non-recurring engineering costs that limit economically viable production volumes.

Advanced packaging technologies address these limitations through heterogeneous integration strategies that can be broadly categorized into three classes: (1) wafer-level approaches, such as 3D integrated circuits (3D-ICs) using through-silicon vias (TSVs) and wafer-to-wafer bonding; (2) die-level approaches, including chiplet-based integration on interposers, die-to-die bonding, and Embedded Multi-die Interconnect Bridge (EMIB); and (3) hybrid approaches, including fan-out packaging and micro-transfer printing (µTP) [3]–[5]. These technologies offer varying trade-offs in performance, density, cost, and design flexibility to meet demands across server, networking, and consumer applications.

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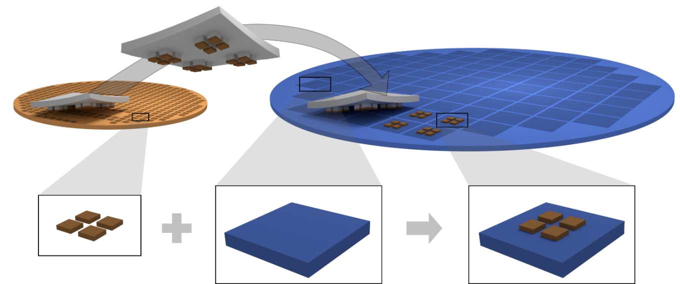

Fig. 1. Overview of the micro-transfer printing (µTP) process. An elastomer stamp (gray) transfers pre-fabricated chiplets from a source (left) to a target wafer (right). This process exploits the velocity-dependent adhesion of the stamp material: during rapid motion, van der Waals forces promote die attachment to the stamp rather than the source wafer (pick-up), while slower motion reverses this effect, enabling die release on the target wafer

High-density solutions (3D-IC, advanced interposers, EMIB) go very well with performance-critical applications where fine-pitch interconnects, minimal signal latency, and low power consumption justify their cost and design complexity [6]. However, emerging applications, such as next-generation RF front-ends, integrated photonics, and biomedical sensors, often accept a more relaxed interconnect density but with a stronger focus on integrating specialized materials and devices.

This paper focuses on micro-transfer printing (Fig. 1), which enables cost-effective heterogeneous integration for such emerging applications. Based on the experiences of initial tape-outs, our main contributions are (1) defining the challenges of µTP design, (2) developing a new µTP-specific design step, and

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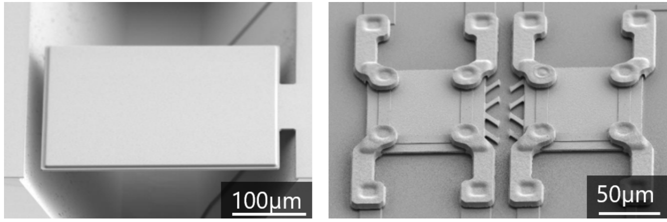

Fig. 2. Scanning electron microscope pictures of a print-ready chiplet on a μTP source wafer, formed by wet chemical under-/release etch and kept in place by the tether-anchor structure (left) and chiplets printed onto the target substrate with redistribution layer (RDL) interconnects (right)

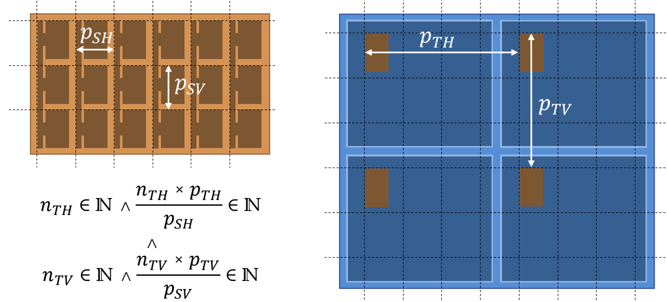

Fig. 3. Pitch compatibility between source and target reticles/wafers: print-ready source reticles with anchor and tether structures holding the lateral etched chiplets (left), target reticle dies with in-between scribelines and a repeating chiplet placement (right). The chip-corner to chip-corner distances determine the respective pitches of source and target, which are required to form a least common multiple for a valid stamp pattern. It may be expedient to print only every n^{th} target die (horizontally and/or vertically)

(3) integrating this new step into the design and manufacturing process in order to overcome the aforementioned challenges.

Sections I-A and I-B introduce the technology and its unique design challenges. Developing manufacturable μTP designs necessitates a systematic methodology that differs fundamentally from traditional IC and packaging design flows. The complete design flow, including the novel wafer planning step, is presented in Section II. Section III finally provides a representative design example.

A. Micro-Transfer Printing

Micro-transfer printing (μTP) is an assembly technology that enables heterogeneous integration by transferring pre-fabricated (also called print-ready) devices from source wafers to target wafers using a micro-structured elastomer stamp (Fig. 1) [7]–[9]. The process exploits the viscoelastic properties of the PDMS (Polydimethylsiloxane) stamp material that enables a velocity-dependent adhesion: during rapid stamp motion, van der Waals forces bind dies more strongly to the stamp than to their source wafer (pick-up), while slow motion reverses this relationship (release).

Such stamps enable high throughput values by a pronounced parallelization of the integration process of up to thousands of chiplets per transfer operation. The process involves three key elements: (1) source wafers with devices released by selective under-etching, (2) the elastomer stamp as transfer medium, and (3) target substrates prepared with adhesion layers. The

TABLE I
INTERRELATED DESIGN PARAMETERS TO BE CONSIDERED FOR μTP

Scope	Parameters
source die	size, pad locations
target die	size, pad locations, clearance, print areas
source reticle	anchor & tethers, spacings (etch trenches)
target reticle	scribe line, PCM, peripheral ring
top level	source die placements, RDL
stamp	post pattern, size
metrics	wafer utilization, print count

μTP steps are followed by conventional wafer-level backend processing, including redistribution layer (RDL) fabrication for electrical interconnection.

The right part of Fig. 4 (next page) provides a visual representation of the μTP manufacturing process. Based on the source and target wafer layouts, the corresponding wafers are manufactured in their respective technologies. Source wafers are required to run through the aforementioned etch process to create freestanding print-ready chiplets attached to tether and anchor structures (Fig. 2, left). The stamps required for transfer printing are fabricated on the basis of the stamp layout derived from the wafer planning step. After printing, electrical connectivity can be established at the wafer-level through an RDL fabrication step (Fig. 2, right). The final μTP device is obtained after wafer separation and packaging.

The following subsection examines how μTP fundamentally alters the design process compared to conventional IC design.

B. μTP-Related Design Challenges

Unlike conventional IC design flows, where chip design and packaging are related but largely independent phases, μTP creates new interdependencies across multiple design domains. This introduces challenges for established design flows:

1) Interrelated Design and Manufacturing: Chip design needs to be aware of reticle/wafer-level layout decisions usually deferred to backend (in-fab) stages after tape-out. For example, the validity of source die placements is affected by the actual chiplet pitches on the print-ready wafer with its anchor and tether structures and spacings. The required pitch compatibility between the source and the target is illustrated in Fig. 3.

2) Multi-Technology Coordination: Designers must simultaneously handle multiple semiconductor processes (CMOS, MEMS, SiGe, etc.) where each source and target wafer follows independent process design rules. This requires concepts to combine and modularize the process design kits (PDKs) involved. Interrelated design steps, such as top-level floorplanning, must implement cross-technology and context-dependent rules.

3) Inter-Layout Dependencies: Design constraints are no longer restricted to the chip layout at hand. Changes in one layout may require adjustments across all other layouts to maintain a correct design. Source and target chip layouts must simultaneously consider die sizes, print and pad positions, and RDL routing.

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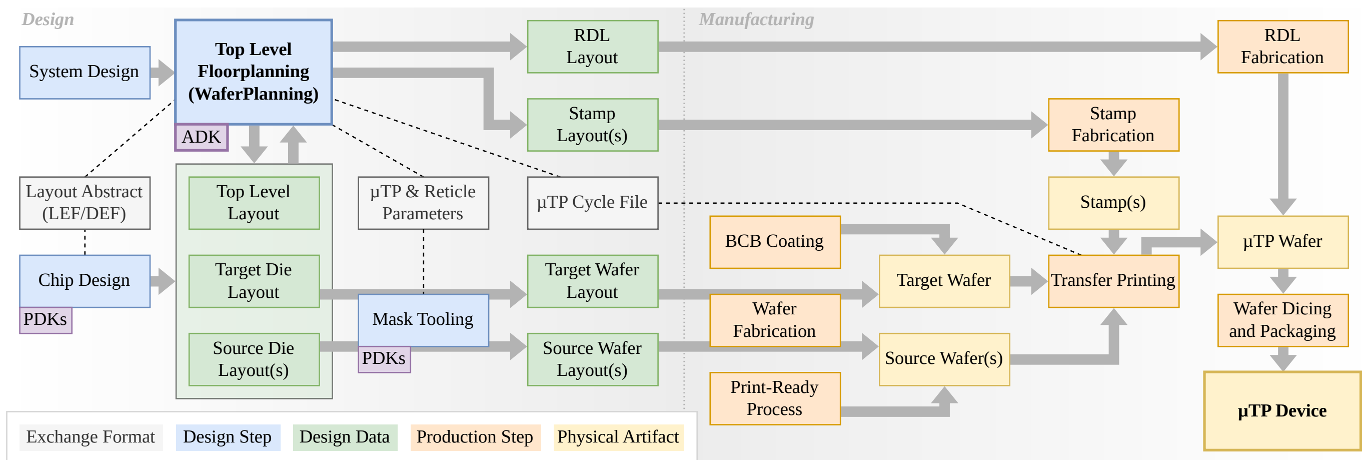

Fig. 4. Design (left) and manufacturing flow (right) overview. µTP design involves wafer level considerations usually conducted after sign-off within the fab (mask tooling). Furthermore, fabrication steps become design dependent (stamp layouts and printing sequences). The new wafer planning step aims to improve user accessibility by processing all dependencies in one place

4) Multi-Level Design Aspects: µTP design choices extend beyond the sole chip level:

- *Chip level:* Individual die layout, I/O placement;
- *Reticle level:* Die arrangement and spacing on source wafers, anchor design;
- *Wafer level:* Source wafer utilization, printing sequence optimization.

Conventional IC design tools operate on chip level and do not capture the required cross-level dependencies. Table I provides an overview of the relevant design parameters.

5) New Design Steps: The µTP process incorporates design stages that are absent from traditional integrated circuit (IC) workflows:

- *Wafer planning:* Floorplanning of source dies originating from different source wafers, their reticle layouts, and printing sequence—a chip-wafer co-design step absent in monolithic IC design.
- *Anchor/tether design:* Requires explicit modeling and parametrization of mechanical release structures on wafer-level.
- *Cross-technology verification:* Design rule checking must span multiple PDKs and verify assembly constraints.

These challenges necessitate a systematic design methodology: The connection of individual chip designs with wafer-level decisions, ensuring consistency across the different scopes. The management of cross-technology constraints must enable the consideration of design rules and technology setups that span multiple PDKs. By introducing wafer planning as an additional design step, layout decisions of the source and target wafers are moved to early design stages with direct impact on µTP design.

Section II outlines a design flow tailored to these requirements. Within it, the wafer planning phase (Section II-B) serves as a crucial link between chip-level and manufacturing-level decisions.

II. Design Flow

As noted in Section I-B5, the µTP design process augments conventional IC design flows with additional, specialized steps. These address the multi-chip, multi-technology integration challenges that we identified in Section I-A. Fig. 4 illustrates the complete flow from system specification through manufacturing. While many steps resemble traditional design phases—system architecture, individual chip design, fabrication, backend processing—µTP introduces a critical intermediate step absent in conventional flows: *wafer planning*. This new step bridges chip-level design decisions to wafer-level manufacturing constraints, serving as the coordination mechanism for heterogeneous integration.

The flow requires additional data exchange formats and design interfaces not present in conventional IC design. Unlike traditional flows where GDSII and standard PDK formats suffice, µTP necessitates formats that capture cross-technology relationships, wafer-level layout data, and manufacturing information. These formats enable communication between chip design and fab engineering.

During *system design* (also known as specification and architecture phase), system requirements drive functional partitioning, technology selection, and interface definitions. However, unlike in monolithic designs where a single technology is chosen, µTP requires simultaneous selection of multiple source technologies (e.g., CMOS logic, III-V photonics, MEMS sensors) and early consideration of how these will be physically integrated.

The subsequent design phase also introduces closer interaction between *chip design* and *mask tooling* than conventional IC design. Since source and target wafer layouts directly influence transferability and assembly efficiency, mask design must be addressed early in the design process to ensure that reticle layouts meet both chip-level electrical requirements and manufacturing constraints.

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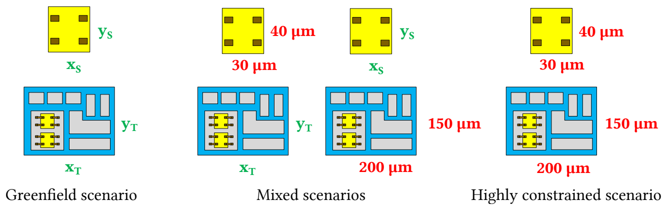

Fig. 5. Illustration of various design flexibilities (degrees of freedom). Depending on the origin of the components, the design is more or less constrained. Examples show two source dies (yellow) printed on a target die (blue), spanning from the most relaxed design on the left (all components are designed concurrently, enabling holistic co-optimization across the design hierarchy) to a highly constrained design on the right

Verification extends beyond traditional single-technology design rule check (DRC) and layout versus schematic (LVS) to include cross-technology constraint checking and the validation of the µTP-related aspects. Foundries can implement this through modular PDK architectures where separate rule decks address the different aspects: print-ready design rules for source reticles, RDL-specific rules for interconnect layers, and chiplet/target rules for pitch compatibility.

A. Design Flexibility and Component Origin

The degrees of freedom available during wafer planning (Table I) vary significantly depending on whether components are designed specifically for integration or adopted from existing designs. Fig. 5 illustrates three typical scenarios:

1) Greenfield Scenario: When all components (source and target dies) are designed concurrently for the µTP integration, designers have maximum flexibility. Die sizes, I/O positions, and chiplet placements can all be optimized jointly to maximize source wafer utilization, minimize alignment sensitivity, and simplify RDL routing. This scenario allows holistic co-optimization across the design hierarchy.

2) Mixed Scenario: More commonly, some components are constrained while others are flexible. This occurs when integrating commercial off-the-shelf chiplets that arrive with fixed dimensions, I/O locations, and pad configurations. Reusing designs from previous projects may also fall into this category, which is common if redesign costs outweigh the benefits of optimization. In these mixed scenarios, wafer planning must account for existing component constraints while designing the remaining elements—typically the target die and RDL—to effectively bridge fixed and flexible components.

3) Highly Constrained Scenario: In some cases, both source and target die geometries are predetermined (e.g., integrating multiple third-party chiplets onto a finished IC design). Here, wafer planning reduces to feasibility analysis—verifying that the fixed components can be integrated using µTP given the available printing technology and RDL capabilities. If constraints cannot be satisfied (e.g., incompatible source and target die spacings, or alignment tolerances exceed RDL landing pad sizes), the integration may not be realizable without component redesign.

This spectrum of design flexibility means wafer planning cannot follow a one-size-fits-all approach. The methodology must be adaptable to both fully optimized greenfield designs and highly constrained integrations involving pre-existing components.

B. Wafer Planning: Bridging Design and Manufacturing

We introduce *wafer planning* as a novel design step unique to µTP, thereby addressing the challenge of coordinating multiple heterogeneous source wafers into a coherent integration plan. This multi-level optimization problem requires design decisions that affect chip, reticle, wafer, and stamp levels simultaneously. The resulting design solution is referred to as µTP assembly data.

Fig. 6 illustrates the main steps required during wafer planning. To validate the proposed design methodology, a software demonstrator (Fig. 7) was developed to implement these steps which are outlined below in more detail.

1) Layout Import and Technology Setup: Wafer planning begins with an optional step to import µTP assembly data from existing design data via Design Exchange Format (DEF) files from external design tools. These imports focus on layers relevant to physical placement and transferability, such as device outlines, anchor/tether geometries, I/O pad positions, alignment marks, and clearance zones, while abstracting away lower-level interconnect and transistor layers that do not affect wafer planning decisions. Layout imports accelerate planning by eliminating manual data entry and ensure consistency with existing chip designs. For off-the-shelf or external fab components, imported DEF files establish fixed geometric constraints.

µTP design constraints, such as available print-ready rules, wafer diameters, minimum die spacing, stamp pitch requirements, and alignment tolerances, can be specified. This establishes the process boundaries for all subsequent planning decisions. The central wafer planning data model (XML-schema-based) consolidates layout and technology information into a unified project representation

2) Layout of Source and Target Die Abstracts: This step establishes fundamental geometric parameters for each die type: dimensions (width, height, aspect ratio), I/O pad locations, and keep-out zones. Parameters may be imported from DEF files or defined from scratch. For greenfield designs, users specify intended values based on circuit estimates and interface requirements. For off-the-shelf or external sources, abstracts capture fixed constraints. Once evaluated (see Section II-B6), parameters can be adjusted to achieve a feasible µTP design.

3) Reticle and Wafer Models: With die abstracts defined, reticle and wafer models describe the physical arrangement of dies for mask generation and fabrication. Both source and target wafers require reticle layouts for wafer-level fabrication, though they differ fundamentally in structure. Source wafers must be print-ready, incorporating anchor and tether structures that enable die release and transfer. Target wafers follow more traditional layouts with scribe lines separating individual dies. Fig. 3 outlines the essential layout for source and target reticles.

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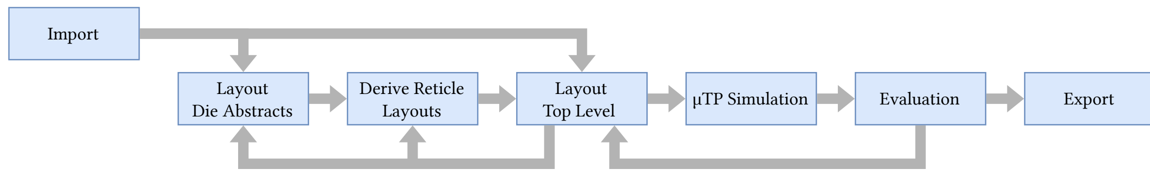

Fig. 6. Simplified wafer planning flow. Typically the layout scope extends with each step (die to reticle to wafer). The configuration of global technology parameters (not shown) allows the consideration of µTP- and technology-specific constraints in all steps

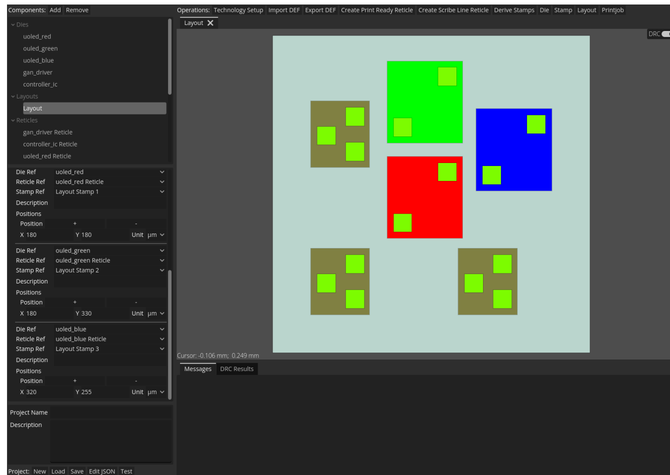

Fig. 7. Screenshot of the software demonstrator used to perform various tasks of the wafer planning step, showing an early floorplanning result of three identical GaN drivers (gray) and three µOLEDs (red, green, blue) from the example described in Section III

4) Top-Level Floorplanning: During top-level floorplanning, source dies are positioned on the target die, defining the physical integration layout. To allow printing of multiple chiplets at once, their placements must align based on source and target die pitches from the reticle models. Printing areas define regions with dedicated alignment marks providing position references for the µTP tool's vision system. Multiple chiplets can share a common printing area.

Routability assessment evaluates electrical interconnects using I/O pad locations from die abstracts [10]. RDL design rules constrain the routing capabilities: minimum trace widths and spacings as well as alignment uncertainty are checked. Design rule violations or routing infeasibility at this stage necessitate iterating back to die abstracts and reticle models to adjust die dimensions, spacing parameters, or reticle layouts.

5) µTP Simulation: This step derives stamping patterns from the top-level floorplan and estimates source wafer utilization. Simple chiplet placement in regular rows or columns result in straight-forward stamping sequences. Distributed chiplet placements result in non-trivial solutions, though. The goal of this step is to obtain good printing patterns and to calculate the theoretically achievable wafer utilization (percentage of chiplets being transferred vs. chiplets remaining on the source wafer) [11].

6) Evaluation: Evaluation assesses the quality of the µTP design via wafer utilization and dead space, indicating if further iterations for optimization are required.

7) Data Export: After evaluation, the µTP design is exported in formats for downstream applications—chip design tools, mask preparation, and assembly equipment. Chip-level abstracts are exported to chip design tools via DEF identical to the import format.

Additionally, PCell parameters to support the generation of anchor/tether structures can be exported. The parameter files specify anchor positions/orientations, tether dimensions, spacings, and alignment marks. They can be used to generate chip arrays with properly positioned print-ready structures, applying the optimized reticle layouts.

As a byproduct of µTP simulation, cycle files for the assembly equipment can be generated. The machine-readable instructions contain pick-and-place coordinates, transfer sequence ordering, and alignment marker information.

C. Chip Design and Mask Generation

The subsequent steps of *chip design* and *mask generation* proceed within the constraints established by the µTP assembly data. These steps translate abstract planning decisions into manufacturable layouts with three main goals: component design, reticle generation, and verification.

1) µTP-Compatible Component Design: Technology configurations within chip layout tools should incorporate µTP-specific layers. Foundries provide modular setups extending base technologies with print-ready rules, allowing designers to work in familiar environments while adding integration-specific elements where needed. The chip layouts must comply with the µTP assembly data. For example, I/O placement must consider chiplet placements on the target dies as well as RDL routing.

2) Reticle Layout Generation: Source wafer reticle layouts arrange dies in regular grids that accommodate stamp feature pitch via a matching die spacing. The layout incorporates the anchor and tether structures while ensuring proper placement of alignment marks for vision systems and test structures for process monitoring. Tool-assisted generation using PCells becomes essential for arrays exceeding 1000 dies, where manual layout would be impractical. The outputs are GDSII-format reticle layouts ready for mask generation. In contrast to the print-ready requirements of source wafers, target dies are typically separated by scribelines on reticle and wafer level.

3) Multi-Level Verification: Individual chip-level design rule check (DRC) and layout versus schematic (LVS) are done via base technology PDKs. Additionally, µTP-specific design rules are checked based on the µTP assembly data. Such rules can vary dynamically, for example, anchor requirements

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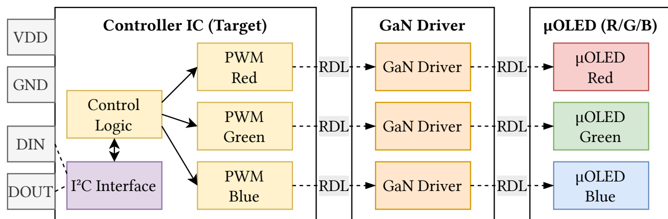

Fig. 8. System architecture of the smart lighting node design example consisting of three identical gallium nitride (GaN) drivers (transferred in one stamping operation) and three µOLEDs in RGB colors from different source wafers

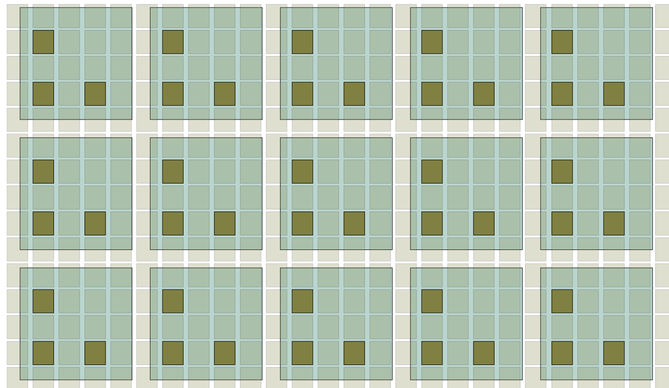

Fig. 9. Overlayed close-up of the reticle and stamp layouts to illustrate the geometric relations between target reticle (controller), source reticle (GaN), and the corresponding stamp after applying the required compatibility adjustments (cf. Table IV). The target dies (large rectangles) on the target reticle (large grid) share a common multiple with the GaN drivers (small rectangles) on the source reticle (small grid). The stamp pattern (small dark rectangles) arises from the top-level layout of the GaN drivers on the controller IC (cf. Fig. 10). Each different source placement requires a suitable stamp

depend on die sizes and the top-level target layout. Print-ready rules verify source reticle layouts based on µTP planning to ensure manufacturability. This includes proper anchor and tether geometries, die spacing, and alignment mark placement. RDL verification incorporates checks for wire width and spacing as well as via landing pad geometries. Sign-off requires passing all verification levels, with failures necessitating iteration potentially back to early µTP planning stages. In practice, modular technology stacks enable independent development of rule decks for new technologies, facilitating continuous expansion.

III. Wafer Planning Example

This section demonstrates the adapted design methodology using a representative example. The wafer planning was performed using the developed software demonstrator (Fig. 7).

The example comprises an intelligent micro-organic light-emitting diode (µOLED, [12]) controller for networked lighting applications, fabricated in standard CMOS as the target die. It provides I/O connections (including a communication bus) and pads for source components requiring pulse-width modulated (PWM) signals across three color channels.

Source components consist of three identical gallium nitride (GaN) drivers (transferred in one stamping operation) and three µOLEDs in RGB colors from different source wafers. Ideally with identical die sizes, allowing one stamp master to be used for all three colors.

The system architecture is shown in Fig. 8. The µOLEDs represent catalog components with print-ready layouts (a yet hypothetical scenario given the current µTP ecosystem maturity). The GaN drivers offer substantial design freedom including mask parameters, while the controller die has a fixed layout but adaptable top metallization for pad placement.

This example demonstrates varying design freedom scenarios. Feasibility verification proceeds with initial parameters; if unsuccessful, available degrees of freedom are adjusted to achieve µTP compatibility. Failure at this stage indicates infeasible requirements, necessitating component reselection or costly redesigns. Table II summarizes the design example specification.

A. Initial Examination of Pitch Relations

Initial feasibility assessment requires only reticle parameters and resulting wafer-level component pitches. A concrete top-level target layout is not needed, yet. Components are entered into the wafer planning tool or imported from commercial EDA tools. Beyond die-level dimensions, corresponding reticle layout parameters must be determined.

For the µOLEDs, wafer-level die pitches are derived from the manufacturer's mask layout. The (assumed) datasheet specifies 25 µm horizontal overhead (anchor width, tether width, chiplet-to-anchor spacing) and 15 µm vertical overhead (chiplet-to-chiplet spacing), yielding a $75 \times 85\,\mu m^2$ pitch.

The GaN driver, co-developed with the fab, offers reticle layout freedom. Initially, technology-mandated DRC-compliant minimum dimensions are used (horizontal surplus: 22.5 µm, vertical: 11 µm). The controller IC, also supplied on wafers, has fixed dimensions and pitch. Table III summarizes the initial parameters.

Obviously, the target-to-source pitch ratios determine the µTP compatibility. For single-pass printing on every target die in the print field, integer ratios are required. Printing every n-th target die (multiplying print operations by n) permits $1/n$ integer ratios. In this example, only integer ratios shall be used.

Initial values yield µOLED ratios of $7.7\overline{3} \times 6.8235$ and GaN driver ratios of $4.7347 \times 5.\overline{225}$. The design is thus µTP-incompatible in its initial state[1]. The remaining design freedoms must be adjusted to accomplish compatible pitch ratios.

B. Pitch Adjustments

To achieve integer ratios, the simplest approach is selecting the next smaller integer value and back-calculating how much the source pitch must increase and/or the target pitch must decrease (if possible). This is accomplished by adjusting the parameters of the reticle (e.g., anchor width) within design rule constraints. The inverse approach (targeting the next larger

[1]For µOLEDs, integer target-to-source pitch ratios occur only at 15× (horizontal) and 17× (vertical) multiples of the target die pitch. A $20 \times 20\,mm^2$ stamp would print merely 4 of 1156 possible target dies in parallel.

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TABLE II
DESIGN EXAMPLE SPECIFICATIONS

Component	Size [μm^2]	Qty	Source	Design Freedom
μOLED (R/G/B)	50 × 70	3	Fixed catalog (5 μm steps)	None
GaN Driver	100 × 100	3	Custom design	High (masks adaptable)
Controller Die	500 × 500	1	Purchased wafer	Limited (top metal only)

TABLE III
INITIAL DIE-RELATED LAYOUT PARAMETERS

Component	Size [μm^2]	Pitch [μm^2]
μOLED	50 × 70	75 × 85
GaN Driver	100 × 100	122.5 × 111
Controller Die	500 × 500	580 × 580

TABLE IV
ADJUSTED DIE-RELATED LAYOUT PARAMETERS

Component	Size [μm^2]	Pitch [μm^2]	Ratio	Adjustment
μOLED	120 × 130	145 × 145	4 × 4	Catalog item
GaN Driver	93.5 × 105	116 × 116	5 × 5	Die size
Controller Die	500 × 500	580 × 580	—	Fixed

ratio) becomes viable only with flexible targets. Shrinking of chip layouts is rarely feasible, as area is usually determined by functional requirements. In general, increased pitches waste wafer area, which must be minimized.

In this example, both target and μOLED pitches are fixed, necessitating a critical decision. We opt for μOLED adjustment. Given the catalog availability, compatible sizes are evaluated first. μOLED area must not decrease to maintain minimum luminosity requirements.

The next suitable μOLED option is $120 \times 130\,\mu\text{m}^2$, which is being considered despite a 4× area increase. Three such μOLEDs arranged horizontally or vertically nearly match the target controller dimensions, making top-level layout feasibility with GaN drivers uncertain but promising.

The GaN drivers, still freely definable, are adjusted to achieve a 5×5 pitch ratio. Back-calculation yields an adapted size of $93.5 \times 105\,\mu\text{m}^2$. Fig. 9 illustrates the resulting reticle grid in relation to the target grid. The chosen reticle parameters target minimum viable values to achieve an optimized wafer utilization. Table IV summarizes the required layout adjustments.

This example adjusts only source die sizes. Since this often entails significant compromises and area losses, reticle parameter adjustment should typically be considered as well. Combining multiple degrees of freedom frequently yields better solutions with fewer trade-offs.

C. Planning the Top-Level Layout

With pitch compatibility established, the top-level target die layout can be created. The GaN drivers, printed simultaneously, are placed first. The relative positioning of source dies from one reticle must maintain the corresponding die pitch, while a shared absolute offset can be set freely within the constraints of the DRC.

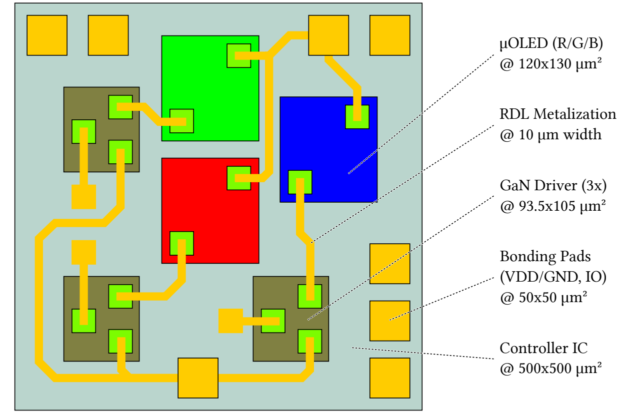

Fig. 10. Top-level layout of the μTP design example showing the placement of the three GaN drivers and μOLEDs (R/G/B), RDL routing, and bonding pads for the package interface

TABLE V
EVALUATION METRICS OBTAINED FOR THE LAYOUT EXAMPLE WITH CONFORMING STAMP SIZES FOR AN (FIXED) 37×37 TARGET ARRAY. THE EXAMPLE SHOWS AN ACCEPTABLE UTILIZATION EXPECTING AT LEAST 84 % USABLE DIES ON THE GAN WAFER.

Component	Die Area Ratio [%]	Stamp Coverage [%]	Dies per Print
μOLED	74.2	100	1369
GaN Driver	72.96	84	4107
Controller Die	73.77	100	1369

Subsequently, μOLEDs are positioned in a way that allows single-layer RDL routing. μOLED placement offers substantial freedom since separate printing eliminates common grid requirements. Spacing and alignment tolerances are the most important factors to consider during placement.

Since top-metal routing on the controller die remains flexible, the pads to contact the printed electronics can be aligned in favor of easy access to the GaN driver and μOLED pads. μTP alignment marks need to be placed as well.

With all chiplets placed and top-metal pads defined, RDL routing is performed using a single layer. Fig. 10 shows the prototypical layout including the placement of the GaN drivers and μOLEDs, RDL routing, and pads for the package interface.

D. Evaluation and Next Steps

The evaluation is based on derived stamps for source transfers. The stamp replicates the source-die layout pattern on

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the target, repeating at target pitch intervals. Fig. 9 illustrates the resulting stamp pattern for the GaN driver chiplets. To maximize reticle utilization, the stamp size should accommodate the maximum number of complete target die pitches without exceeding reticle dimensions.

The stamp-reticle combination enables the calculation of the expected stamping pattern (see Section II-B5). Resulting metrics facilitate the evaluation of the corresponding top-level layout. Table V lists specific metrics for the example layout.

Beyond statistics, the wafer planning step performs DRC verification of relevant rules from various PDKs, sometimes contained in an assembly design kit (ADK). Layout optimization support is also provided.

From the µTP assembly data, GaN driver layout design proceeds with the obtained parameters that result in a µTP-compatible mask layout. Top-level and RDL designs transfer to corresponding tools for final implementation. Additionally, the required design parameters for both stamps (one for the GaN drivers, one common for the µOLEDs) are exported. The printing tool can be programmed based on the optimized print sequences.

IV. Summary and Outlook

This work addresses the core challenges that micro-transfer printing (µTP) introduces to conventional design methodologies. Traditional EDA tools assume (1) a single technology node per design, (2) static design rules, and (3) clear separation between chip and package design. Novel µTP design methodologies violate these assumptions, requiring cross-technology understanding and runtime-dependent rules. Key challenges include interrelated design and manufacturing decisions, multi-technology coordination, inter-layout dependencies, and multi-level design aspects extending beyond chip boundaries.

To address these issues, we introduced a wafer planning step as a coordination mechanism for heterogeneous integration. This intermediate step bridges chip-level design decisions with wafer-level manufacturing constraints, enabling:

- Rapid design space exploration for source/target configurations,
- Integrated µTP rule checking across the relevant design levels,
- Algorithms for utilization optimization,
- Support for multiple data exchange formats and tool chain integration.

Designers can evaluate partitioning strategies and validate µTP compatibility early, before committing to detailed implementation. The presented design example illustrates the practical application of our proposed methodology.

Future enhancements could include optimization algorithms for automated layout suggestions and design space exploration. Additional support is planned for alternative lithography processes (e.g., contact lithography), wafer maps, and advanced verification functions such as LVS or simulator export for thermal analysis.

Micro-transfer printing is highly promising for applications in photonics, displays, and heterogeneous integration. The presented approach enables designers to navigate trade-offs systematically and optimize designs to unlock µTP's full potential.

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