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Full custom MEMS design: A new method for the analysis of motion-dependent parasitics

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ABSTRACT

Due to the lack of sophisticated component libraries for microelectromechanical systems (MEMS), highly optimized MEMS sensors are currently designed using a polygon-driven design flow. The advantage of this design flow is its accurate mechanical simulation, but it lacks a method for analyzing the dynamic parasitic electrostatic effects arising from the electric coupling between (stationary) wiring and structures in motion. In order to close this gap, we present a method that enables the parasitics arising from in-plane, sensor-structure motion to be extracted quasi-dynamically. With the method's structural-recognition feature we can analyze and optimize dynamic parasitic electrostatic effects.

1. Introduction

A microelectromechanical system (MEMS) device consists in general of mobile (movable) mechanical structures acting as a mechanical-electrical signal converter whose size is on the order of micrometers, and a separate signal processing unit. Fig. 1 depicts a MEMS inertial sensor on the left, comprising the MEMS element and the evaluation circuit. The REM image on the right in Fig. 1 shows typical mechanical MEMS structures.

MEMS devices are fabricated in silicon at special MEMS foundries. The main steps of a basic MEMS process technology are depicted in Fig. 2. Please note that, after the release etch (Fig. 2, right), the sacrificial oxides under the poly-silicon 2 layer are partly removed. Hence, the mechanical structures in the poly-silicon layer 2 can move. The main cost factor in high-volume production is due to the MEMS-device footprint. Therefore, enormous efforts are made to shrink the device as much as possible in every MEMS product generation. MEMS devices are downsized by the following means:

1. Pushing the limits of the process technology to achieve smaller design structures.
2. Improved evaluation circuit designs require lower MEMS capacitances.
3. Custom MEMS designs make highly efficient use of space.

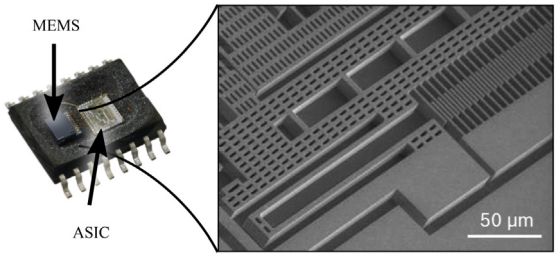

Fig. 1. Left: MEMS inertial sensor with its MEMS element and evaluation circuit (ASIC). Right: REM image of typical mechanical MEMS structures [1].

Fig. 2. Schematic cross-section of the main steps of a basic MEMS process technology [1]. Left: deposition of all poly-silicon and oxide layers. Center: trenching by deep reactive-ion etching (DRIE) of the mechanical structures. Right: release etch of the mechanical structures by a vapor-phase etching step which removes the oxides in certain regions around the holes in the upper layer.

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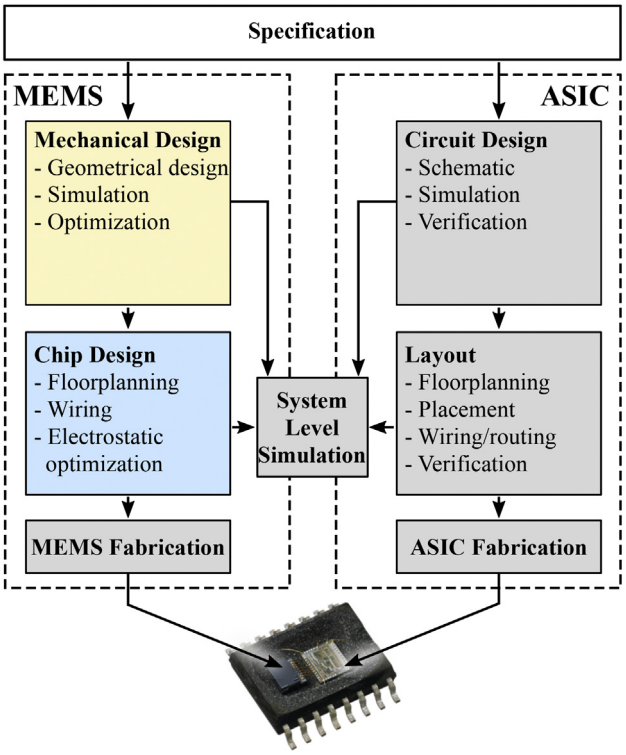


Fig. 3. General MEMS device development flow.

The MEMS design flow is a key success factor as it features simulation and analysis and considers all aspects of the MEMS system. An overview of the general MEMS device development flow is given in Fig. 3. We will focus on the MEMS segment of the development process.

There are currently two different design flows in use for MEMS design: a classical polygon, and a component-library driven design flow. These design flows are described in Sections 3.2 and 3.1, respectively.

As will be shown, the component-library driven flow does not meet the requirements of highly optimized MEMS devices. Therefore, these MEMS devices are currently designed using the polygon-driven design flow. But this flow lacks an accurate method for full-chip analysis of dynamic electrostatic effects.

To close this gap, we present in Section 4 a more advanced version of our method published in [2]. This method approximates the dynamic electrostatic behavior of the MEMS device by quasi-static analysis. Our approach aims to analyze the dynamics of the coupling capacitance in a sequence of deflection phases. The result is a discrete approximation of the dynamic electrostatic behavior which can be used in a continuous dynamic electrostatic model.

Hence, the dynamic electrostatic behavior - along with the mechanical behavior - can be integrated into the design flow. We can thus analyze noise effects triggered by dynamic parasitic coupling capacitances and their positive feedback to the mechanical behavior of the MEMS system.

Due to the polygon representation of the chip geometry in the polygon-driven design flow, the result of the electrostatic analysis includes only the net-to-net coupling capacitances. This is analogous to measuring the capacitance from pad to pad. We have improved our method from [2] by combining it with our structure-recognition algorithm from [3] to reallocate the extracted dynamic electrostatic effects to meaningful parts of the MEMS.

The dynamic electrostatic MEMS response can be exhaustively analyzed and optimized with this quasi-static analysis of the dynamic electrostatic effects at the level of recognized meaningful MEMS parts.

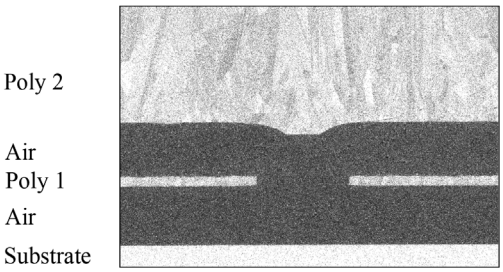


Fig. 4. REM image of a cross-section of a MEMS structure. The center of the image shows the topography of the underside of the second layer (poly 2). This topography is caused by the structuring of the first layer (poly 1) during fabrication.

In summary, this paper makes the following contributions:

1. Analysis of MEMS design flows and their shortcomings.
2. A new method for the analysis of motion-dependent parasitics in polygon-driven MEMS design.
3. Quasi-static analysis of the parasitics comprising the meaningful parts of the MEMS.
4. Validation of our method on a complex 3-axis MEMS yaw-rate sensor.

The problem is described in detail in Section 2 followed by the description of the MEMS design flows used in Section 3. Section 4 shows the modeling of the dynamic electrostatic behavior. In Section 5 the method is demonstrated on a MEMS sensor. The paper closes with a summary and a look at prospective works in Section 6.

2. Problem description

Most MEMS devices are fabricated in silicon. They are commonly composed of mobile mechanical elements and wires. A prominent feature of MEMS is that the wiring and the mobile elements overlap. This results in parasitic coupling capacitances between the wires and the mechanical elements. Additionally, wires below mobile structures can give rise to dynamic parasitics when the structures move. These parasitic coupling capacitances can cause crosstalk between signals or positive feedback converted to a mechanical deflection, especially in MEMS sensors.

We will refine the problem for capacitive inertial MEMS sensors in the following. Similar effects occur in other commonly used MEMS devices.

Conventional inertial sensors have the following structure and working principle. The sensor is composed of a seismic mass, acting as mobile (movable) electrode that is connected by springs to anchor points. The counter electrode structures are located close to the seismic mass. The different electrical potentials of the electrodes cause coupling capacitances to the seismic mass. Thus, moving the seismic mass causes a change in the coupling capacitance. The coupling-capacitance changes are evaluated by a customized integrated circuit.

Topography steps can arise during the fabrication of the MEMS sensor, as shown in Fig. 4.

If the sensor is deflected, these topography steps could move over wires. This would result in a change in the coupling capacitance due to the change in the clearance between electrodes (Fig. 5). This, in turn, disturbs the output signal due to the capacitance-based measurement principle employed in inertial MEMS sensors. Preventive action - based on an analysis of the dynamic electrostatic response - can be taken at the flow front-end against unintended parasitic coupling capacitances. This precludes expensive redesigns and reduces time to market.

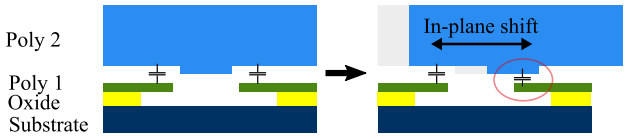


Fig. 5. Schematic cross-section of a MEMS sensor structure. Poly 1 (green): wires, Poly 2 (blue): mechanical structure. Left: The mobile structure is in its resting position. The coupling parasitic capacitances are symmetrical. Right: The mobile structure has shifted. The parasitic coupling capacitance on the right increases, while the one on the left remains constant. (For interpretation of the references to color in this figure legend, the reader is referred to the Web version of this article.)

3. Comparison of existing design flows

In the following subsections, the component-library driven (Section 3.1) and the polygon-driven (Section 3.2) design flow will be described and afterwards compared in Section 3.3.

3.1. Component-library driven design flow

The aim of the component-library driven design approach is to establish a MEMS design flow based on the general idea of the common schematic-driven design flow (SDF) for analog integrated circuits (IC). Therefore, bespoke MEMS component-libraries are introduced for this purpose with the intention of raising the MEMS design abstraction level from simply "drawing polygons" to placing and combining full parametrized components. Such technology-dependent component libraries can nowadays be licensed from MEMS foundries - XFAB [4] is a prime example - as process-design kits (PDK). The models and constraints of the components of such PDKs support the handling of cross-coupling multiphysics effects by restricting the design freedom. This higher abstraction level simplifies the design flow and allows smaller and fabless companies to develop their own application-specific MEMS devices.

The development of this type component-library driven design flow has come into research focus in recent years [5–8]. Fig. 6 gives an overview.

In the flow, the MEMS mechanics are designed by simply placing and combining the parametrized components in a dedicated CAD-software tool (e.g., [9,10]). This design flow features different simulation and analysis methodologies for the mechanical geometry (Fig. 6).

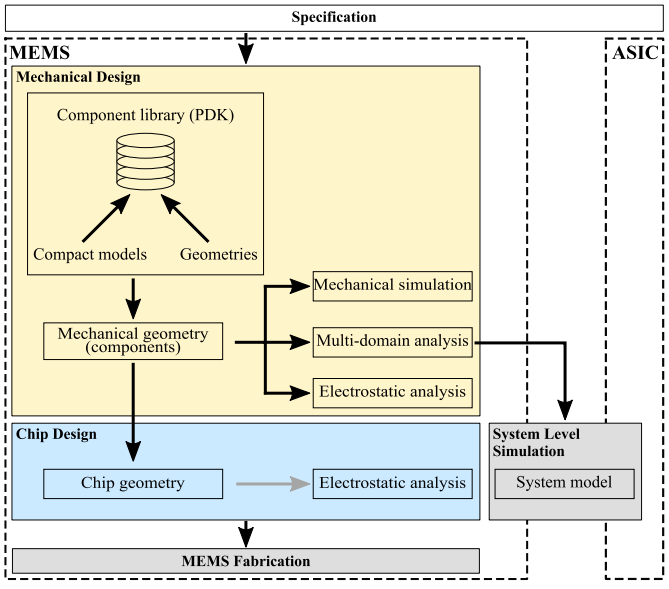


Fig. 6. Schematic overview of the component-library driven design flow.

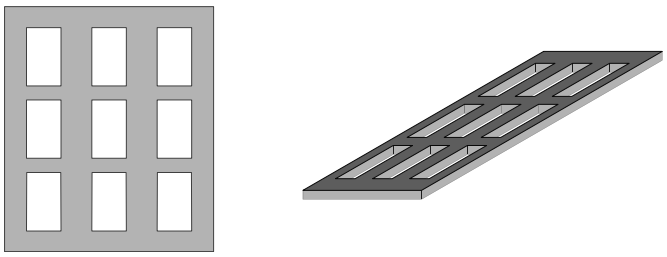


Fig. 7. The perforated plate, shown in 2D on the left and 3D on the right, is a common structural element in MEMS.

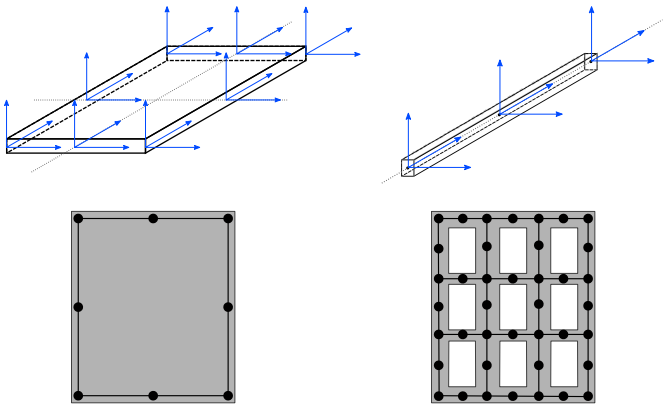
The component-library driven design flow commonly makes use of a circuit simulator to rapidly simulate the mechanical response (e.g. [6,8]). The mechanical finite element (FE) model of each library component must be mapped to a compact model in this method. These models can be connected to an (electrical) network in the circuit simulator that correlates with the components' geometrical interconnections. This simulation method is described in [8,11,12].

The accuracy and speed of this simulation approach are determined by the selected FE models for the components. For example, we consider a perforated plate, as depicted in Fig. 7.

This plate could be described as a plate with a relative density parameter, as shown in Fig. 8a. This description requires fewer degrees of freedom and greatly reduces model complexity. Another option is to model the perforated plate with a number of crossbars (Fig. 8b). The first model can be simulated faster than the second one, but the predicted real mechanical response will be less accurate.

The mechanical analysis can be upgraded to include multiphysics simulation by introducing the electrostatic back-coupling as a non-linear force. The system model is derived from the resultant dynamic multiphysics model. It can be applied to jointly simulate the MEMS element and its evaluation circuit. The design flow provides a detailed electrostatic analysis by a field solver, as well. The resulting netlist includes only the components' electrostatic properties; it neglects all parasitic effects that could arise due to the chip geometry. The chip geometry includes the polygon representation of the mechanical components, the chip frame with the bond pads, and the wiring that connects the mechanical components to the chip bond pads.

The polygon representation of the components is synthesized by parametrized polygon generators, like PCell [14]. After this polygon representation is placed into the chip, the mechanical structures are manually wired to the chip bond pads.



(a) Non-linear 3D shell element. **(b)** Non-linear 3D beam element.

Fig. 8. Top: FEM model for non-linear 3D elements [13]. Bottom: representation of the perforated plate in Fig. 7 with the FEM elements.

An electrostatic analysis by a field solver can then be rerun on the full-chip geometry. The resulting netlist now includes all parasitic electrostatic effects.

3.2. Polygon-driven design flow

The historic root of the polygon-driven design flow is the native polygon drawing of the physical MEMS design. Today, the design of highly optimized MEMS devices is still polygon-driven, and most MEMS geometries are drawn by polygon generators (see the generator for a perforated plate). The value and benefit of this approach is the very accurate mechanical simulation at polygon level by efficient customized methods that enables the use of cutting-edge MEMS process technologies. The complex multiphysics cross-coupling effects arising during the MEMS design must be scrutinized and optimized in detail due to the high level of design freedom. This challenge is tackled by problem-specific and customized simulation methods. Highly complex inertial yaw-rate sensors, including non-linear mechanical effects, can thus be simulated accurately [15,16].

The design freedoms offered by the polygon-driven design approach allows customer requirements for MEMS accuracy, robustness and footprint to be satisfied by pushing the technology envelope. There is still the caveat to be considered here of the major effort needed to customize or incorporate methodologies in the design flow for the analysis and simulation of the MEMS devices. Hence, this design flow should only be considered for highly optimized MEMS devices in conjunction with a process technology development in high-volume production.

The polygon-driven design flow begins with the design of the mechanical geometries by polygons or polygon generators (Fig. 9). An FE-beam model is generated (e.g., Euler-Bernoulli or Timoshenko beam model, Fig. 8b) on which efficient and accurate simulations of the mechanical response are based. The common strategy for complex MEMS devices is to analyze the mechanical behavior among others with an FE-modal analysis [17]. In this simulation the natural oscillation modes of the MEMS-model are computed by solving the eigenvalue problem of the structural dynamics equation of motion. The corresponding eigenvectors represent the natural oscillation modes. A reduced-order subspace is defined by the first n eigenvectors with the smallest n eigenfrequencies. By leveraging the reduced basis defined by these eigenvectors, the MEMS model is transformed into the dimensionally lower mode space. The procedure is also known as modal superposition [18,19]. The resulting reduced-order model is used for further analysis. Hence, in this "open" design flow, the simulation methods can be tailored for individual problems; and special non-linear mechanical effects can be included in the simulation, as well. For example, a lot of effort has gone into integrating the non-linear effects of the drive amplitude of capacitive MEMS yaw-rate sensors in the simulation [16]. The

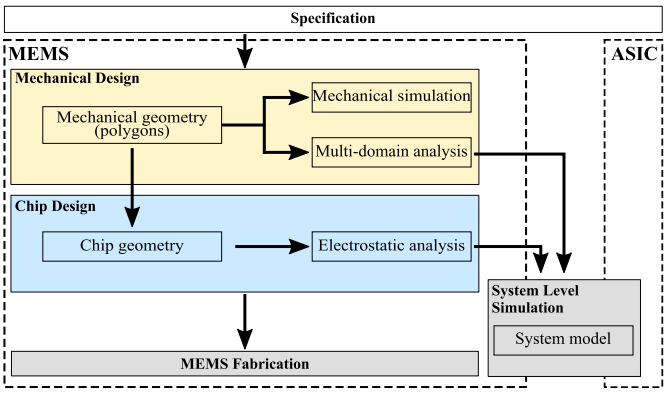


Fig. 9. Schematic overview of the polygon-driven design flow.

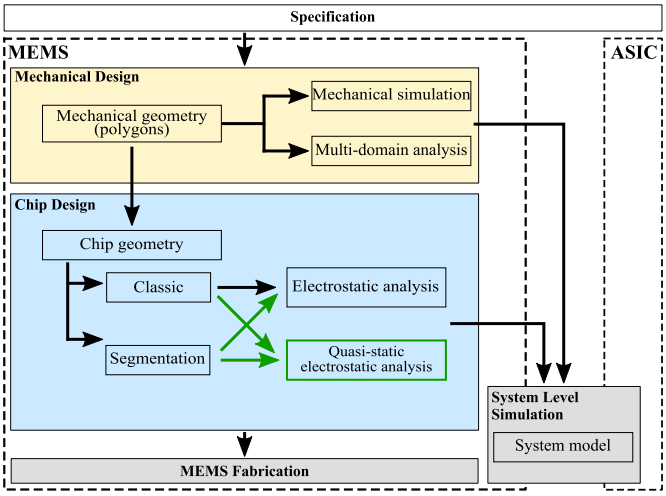


Fig. 10. Schematic overview of the polygon-driven design flow with our new quasi-static electrostatic analysis method (marked in green). (For interpretation of the references to color in this figure legend, the reader is referred to the Web version of this article.)

mechanical simulation has been augmented by the multiphysics simulation described in detail in Ref. [20]. But both simulation approaches are aware only of the mechanical geometry of the MEMS device. This means that parasitic effects, such as coupling capacitances caused by the wiring, are neglected in these simulations.

After the optimization of the mechanics, the mechanical geometry is placed into a chip (Fig. 9). This is followed by the manual wiring of the mechanical structures to the chip bond pads. Wires are commonly required under the mobile mechanical structures due to the highly optimized mechanics. These wires can cause static or dynamic parasitic coupling capacitances as demonstrated in Section 2. They can impact the mechanical response or induce noise effects on the electrical outputs. Therefore, an accurate electrostatic analysis of the full chip geometry is implemented in the design flow by a commercial field solver to optimize the parasitic coupling capacitances (in general, to achieve symmetry of parasitic coupling capacitances) (Fig. 9). Up to now, all additional electrostatic effects, in particular dynamic parasitic coupling capacitances arising from MEMS structural motion/deflections, are neglected.

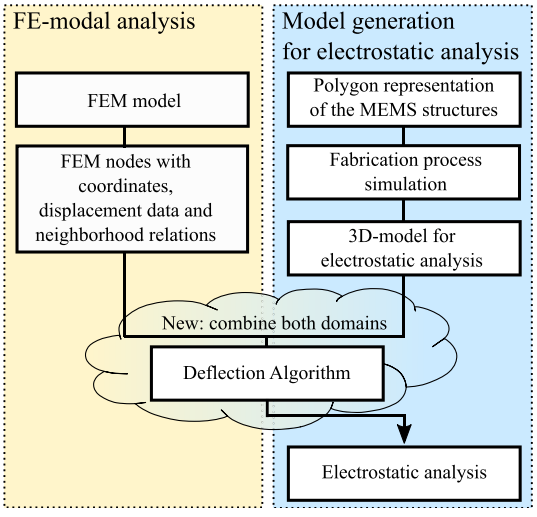


Fig. 11. Our approach for the quasi-electrostatic analysis flow: combining the data from the established mechanical FE-modal analysis with the electrostatic model.

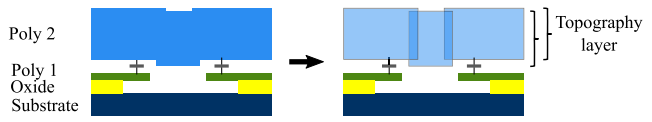


Fig. 12. Modeling the topography steps in the fabrication simulation for the electrostatic analysis (cross-section).

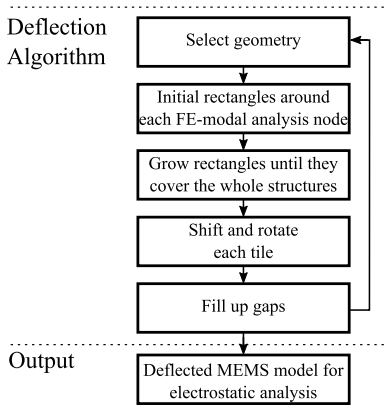


Fig. 13. The deflection algorithm flow.

The electrostatic analysis makes use of a simplified process technology simulation that models the three MEMS-specific process steps depicted in Fig. 2: the topography-aware deposition of materials, trenching and vapor-phase etching. The input to this process simulation is the chip geometry, which is available only as a polygon representation. Therefore, the field solver can extract only the net-to-net coupling capacitances; the nets are defined by text labels on the chip bond pads.

The extracted coupling capacitances are used together with the multiphysics simulation model to generate the system model.

3.3. Contributions to the polygon-driven design flow

The component-library driven design flow lacks sophisticated MEMS component libraries that would provide enough design freedoms for the design of highly optimized MEMS devices, as described in Section 3.1. Therefore, these MEMS devices are currently designed using the polygon-driven design flow described in Section 3.2. This design flow is notable for its accurate mechanical simulation by FE-modal analysis (e.g. [17]). The polygon-driven design flow would benefit from an accurate method for a full-chip analysis of dynamic electrostatic effects, as described in Section 3.2.

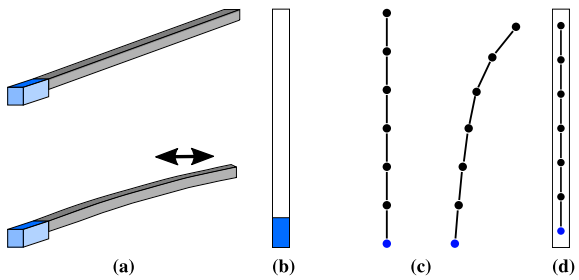


Fig. 14. a) Top: 3D cantilever beam which is fixed at the blue anchor point. Bottom: deflected cantilever beam. **b)** Polygon representation of the cantilever beam. **c)** Left: nodes of the FE-beam model of the cantilever beam at rest. Right: deflected FE-beam model. **d)** FE nodes placed and aligned in the polygon representation of the cantilever beam. (For interpretation of the references to color in this figure legend, the reader is referred to the Web version of this article.)

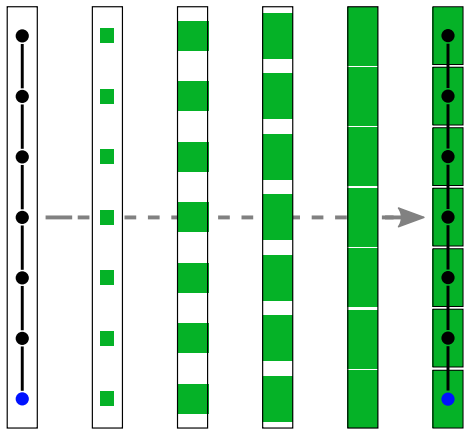


Fig. 15. Growth of the initial rectangles inside the cantilever beam until they overlay the entire geometry.

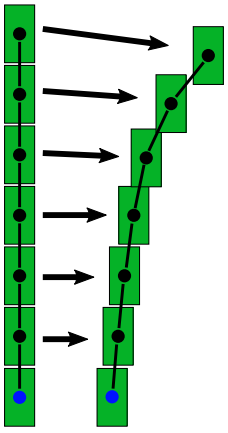


Fig. 16. Tile shifts by the displacement information of the related FE node.

To close this gap in the design flow, we present in Section 4 a more advanced version of our method for analyzing motion-dependent parasitics [2]. The method approximates the dynamic electrostatic behavior of the MEMS device by quasi-static analysis. The goal of our approach is to analyze the coupling-capacitance dynamics in a sequence of deflection phases. To this end, the electrostatics for each deflection phase are analyzed. This electrostatic analysis combines the data from the established FE-modal analysis with the fabrication process simulation (in other words, with the topography and etching processes' effects, see Fig. 2). The quasi-static analysis models can be handled by a commercial electrostatic analysis tool - for example, a field-solver like Calibre xAct3d [21]. Finally, the results of the sequence of electrostatic analyses can be interpolated. This yields an approximation of the dynamic electrostatic response.

The result of the electrostatic analysis includes only the net-to-net coupling capacitances due to the polygon representation of the chip geometry in the polygon-driven design flow. Small dynamic electrostatic effects on the order of some femtofarad, like those occurring in MEMS sensor design, can be superimposed. To remedy this flaw, we supplement our analysis method from [2] with our rule-based, structure-recognition algorithm published in [3]. Major MEMS elements, such as the seismic mass or electrode combs, can be identified as so-called *topology elements* with this structure-recognition algorithm. In combination with the electrostatic analysis, the extracted capacitance values can be mapped to their respective topology elements. Parasitics can thus be allocated geometrically in the chip geometry.

Fig. 10 shows the polygon-driven design flow featuring our new methods.

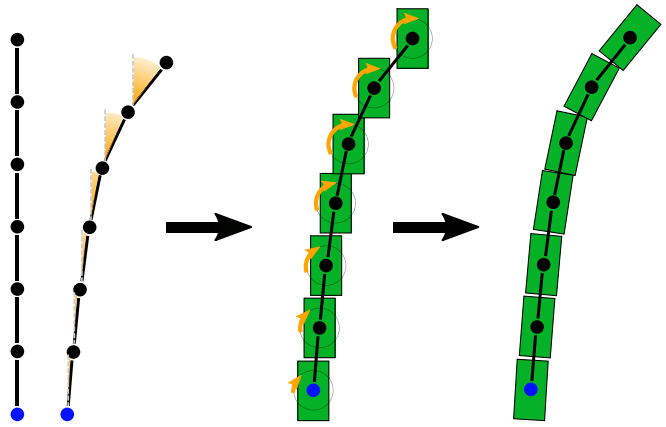


Fig. 17. Left: FE model of the cantilever beam in the rested and deflected positions. The angles between the nodes in the resting position are zero. In the deflected position, the negatively oriented angles are marked in orange. Please note that in more complex FE models a node will have several neighboring nodes with positive and/or negative angles. Center: shifted cantilever-beam tiles from the previous step. Right: rotated beam tiles. (For interpretation of the references to color in this figure legend, the reader is referred to the Web version of this article.)

4. Modeling the dynamic electrostatic response

Mechanical inertia with respect to the electrostatics means that the dynamic electrostatic response can be modeled by a sequence of electrostatic analyses. Each quasi-electrostatic analysis represents one deflection state of the MEMS device. The quasi-electrostatic analysis is described in detail in the following subsections. Fig. 11 gives an overview of the flow.

4.1. Finite element modal analysis

The mechanical response is simulated by an FE-modal analysis on a Timoshenko beam model during the design of the mechanical elements (see Section 3.2, [17]). The FE-model nodes are the start and end points of the Timoshenko beams and can be exported with their coordinates, displacement information and neighborhood relations.

4.2. Model generation for electrostatic analysis

The electrostatic analysis is performed on the polygon representation of the full-chip geometry, as described in Section 3.2.

The fabrication simulation calculates a simplified 3D model from the polygon representation for the electrostatic analysis. This model includes the effects of the etching processes and topography steps (Fig. 4). The topography steps, shown in Fig. 4, are modeled by splitting the original layer into *topography layers* (Fig. 12).

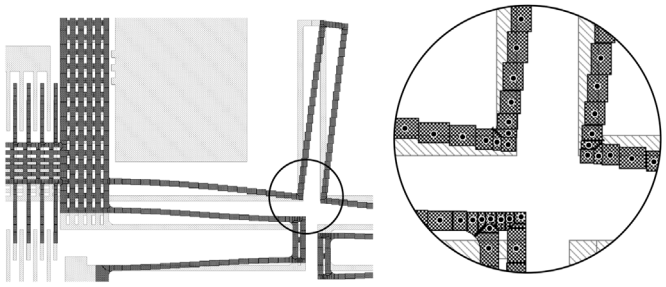


Fig. 19. Tiles shifted by FE-modal analysis displacement data.

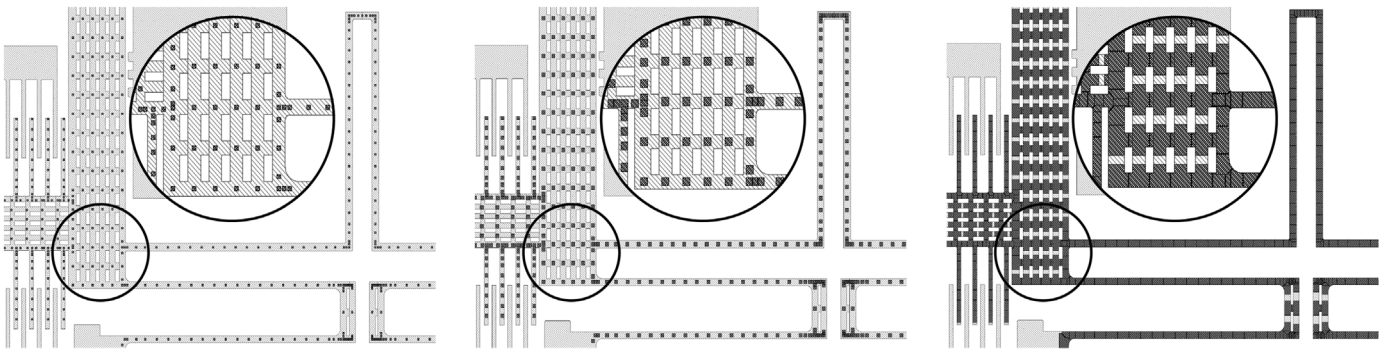
4.3. Deflection algorithm

The deflection algorithm combines the node data exported from the FE-modal analysis with the model of the fabrication simulation. The combination is done by mapping each FE node to a unique part of the geometry of the fabrication simulation model. Afterwards, the displacement information of the FE nodes is utilized to shift the related parts of the geometry. Fig. 13 shows the steps in the deflection algorithm, which are described and visualized below with an exemplary cantilever beam (Fig. 14a).

The algorithm selects the geometry of the first topography layer (Fig. 12) which shall be deflected from the process-simulation model. In the next step, the algorithm places and aligns the FE nodes by their coordinates into the polygon geometry of the selected topography layer (Fig. 14d). All nodes, which are outside the current topography layer, are neglected (see Fig. 12).

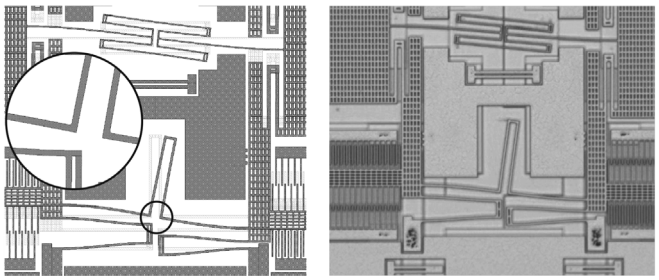
To map the displacement information for each FE node to the selected geometry, the geometry is partitioned into tiles by the following constraints. There is one unique tile for each FE node, and the unification of all tiles is overlaid on the entire selected geometry. The geometry is partitioned into these tiles by generating small initial rectangles around each placed and aligned FE node. A commercial layout verification tool calculates the growth of all regular rectangles inside the current geometry. The initial rectangles are repeatedly grown until they overlay the entire selected geometry (Fig. 15).

Now the selected geometry is segmented into small tiles and each node of the FE-modal analysis is mapped to one of these tiles. Each tile inherits from its node the displacement information from the FE-modal analysis so that each tile can be shifted by this displacement information (Fig. 16).



(a) Growth after 10 iterations. **(b)** Growth after 20 iterations. **(c)** Growth after 80 iterations.

Fig. 18. Growth of the initial rectangles around the FE nodes of a MEMS yaw-rate sensor until they overlay the entire geometry.



(a) The final deflected model for the electrostatic analysis.

(b) Ground-truth microscopic image of the deflected structure

Fig. 20. The final deflected model for the electrostatic analysis compared to a ground-truth microscopic image of the deflected structure [22].

The result is a coarse block representation of the selected geometry of the deflected MEMS (Fig. 16). We refine this first- order approximation by applying an additional rotation to each tile. The rotation angle is derived for each tile from the original, and shifted, positions of the FE nodes and their neighbors (Fig. 17). The loop ends with the filling of all small gaps between the tiles.

To prove that our algorithm also works on complex polygon geometries, we demonstrate our deflection algorithm on a section of a MEMS yaw-rate sensor. Fig. 18 visualizes the growth of the initial rectangles around the FE nodes inside the sensor geometry. Fig. 19 shows the same part of the sensor in the deflected-block representation, and Fig. 20a the final deflected geometry. Fig. 20b shows a ground-truth microscopic image of the same part of the MEMS yaw-rate sensor in the same deflected state as our generated geometry in Fig. 20a.

Please note that, due to the separate deflection of each topography layer of the process simulation model, the topography steps are preserved by our deflection algorithm (Fig. 21).

4.4. Electrostatic analysis

The electrostatic analysis is done by a commercial field solver which usually solves the integral form of Maxwell's equations on the surface of the extruded polygon model by a boundary-element method [23]. It extracts a detailed net list and the coupling capacitances between all nets in the MEMS device that are defined by the bond pads.

4.5. Quasi electrostatic analysis on the level of topology elements

The net-to-net electrostatic analysis here is not well qualified to exhaustively analyze the parasitic coupling capacitances (see Sections 3.2 and 4.4). To address this challenge in the polygon-driven design flow, we propose a new rule-based MEMS structure-recognition algorithm in [3]. Primary MEMS elements, such as seismic masses and electrode structures, can be identified as so-called *topology elements* with this algorithm (Fig. 22).

The algorithm makes use of an initial segmentation of the chip geometry, defined by markers and a predefined rule set. This set of rules

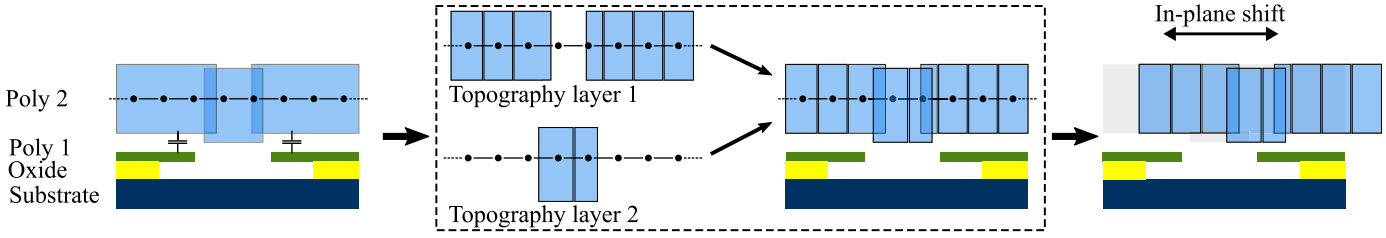


Fig. 21. Left: cross-section of the layer stack with highlighted topography layer (Fig. 12) of poly 2 and FE nodes of the MEMS beam model. Center: each topography layer is split into disjoint tiles as described in Section 4.3 and shown here in a cross-section. Right: the in-plane shift is applied to each tile on each topography layer which preserves the topography steps that arise during fabrication (see Section 2).

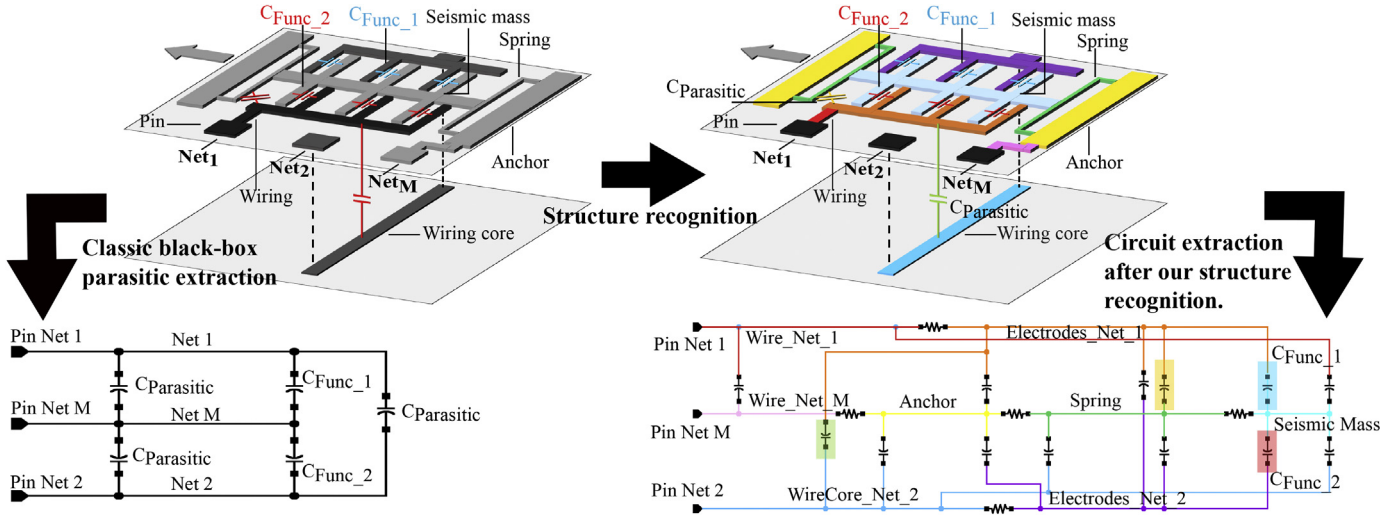


Fig. 22. Overview of our structure-recognition algorithm from [3]. Left: acceleration sensor with conventional black-box parasitic extraction. Top right: acceleration sensor after our new structure recognition method has been applied. The sensor topology elements are shown in different colors. Bottom right: circuit extraction after structure recognition. The recognized sensor topology elements are represented by sub-nets with matching colors. The sub-nets are connected by dummy resistors. (For interpretation of the references to color in this figure legend, the reader is referred to the Web version of this article.)

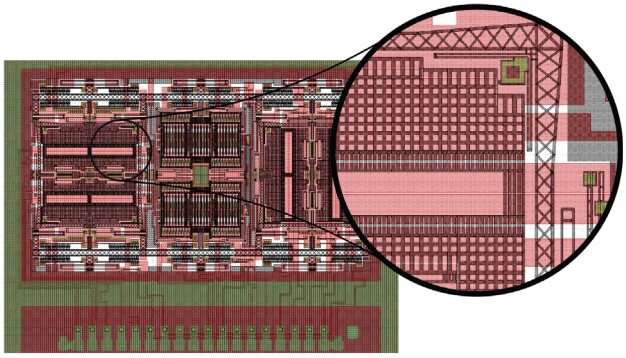


Fig. 23. Three-axis MEMS yaw-rate sensor designed by Bosch Sensortec.

describes only the geometrical relations between topology elements. The key benefit of this approach is that the topology elements are derived and recognized independently of the chip geometry. Hence, the rule-based recognition procedure utilizes only the information provided by the well-known invariant operating mode of the MEMS element and its technology. Therefore, only one rule set needs to be defined for each MEMS type - be it an acceleration or yaw-rate sensor - in each fabrication technology. With this method, the main elements of a MEMS inertial sensor, like the seismic mass, or comb structures, can be recognized by means of an initial segmentation which marks the springs' position in the chip geometry. In [3] we show that the extracted capacitance values can be mapped to recognized topology elements using this structure recognition in combination with the electrostatic analysis. The extracted parasitic capacitances can thus be allocated geometrically in the chip geometry.

We upgrade our deflection algorithm from Section 4.3 to handle topology-element geometries. The main modifications cover the handling of data structures. We can now combine the analysis of the dynamic parasitic capacitances with the structure-recognition logic. Dynamic parasitics can also be analyzed at the level of the recognized topology elements. Furthermore, the dynamic parasitics in the chip geometry can now be reallocated geometrically based on the topology elements. This allows detailed analysis and optimization of dynamic parasitic capacitances in MEMS elements.

4.6. Output of the quasi-electrostatic analysis

The quasi-electrostatic analyses generate a sequence of data points. These data points represent the mapping between the deflection of the MEMS structure and the associated coupling capacitances. Thus, dynamic parasitic coupling capacitances can be designated with respect to mechanical-structure movements.

Functional and parasitic coupling capacitances can be separated with the structure-recognition methods from [3]. And now, we can separate the dynamic parasitics from the functional capacitances with a combination of the structure-recognition method and the quasi-electrostatic analysis. Certain use cases, like the simulation of the drive mode in MEMS yaw-rate sensors, can benefit from adding dynamic parasitic capacitances to MEMS system model output signals. The effects of in-plane dynamic parasitic coupling capacitances - like noise, positive feedback to the mechanical structure, or interference between signals - on the behavior of the whole system can thus be scrutinized and assessed.

We demonstrate in Section 5 our new method for the analysis of the dynamic parasitics on a 3-axis MEMS yaw-rate sensor - first, jointly with the classic net-to-net electrostatic analysis, and then with the structure-recognition technique.

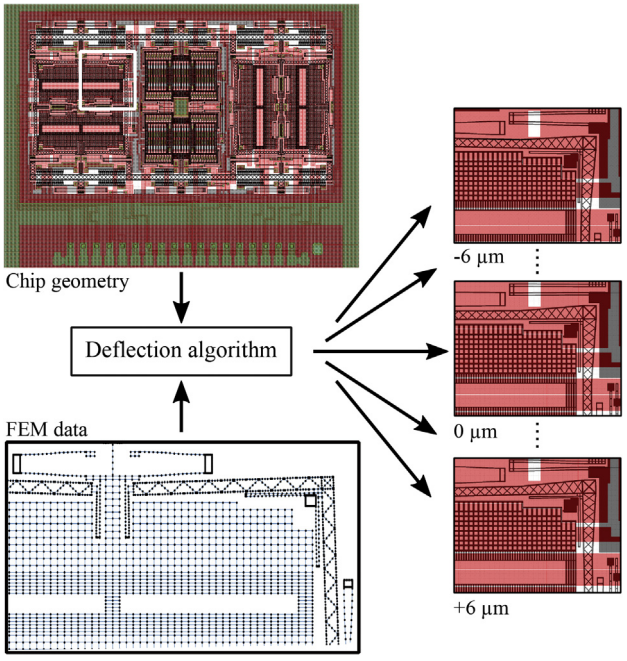


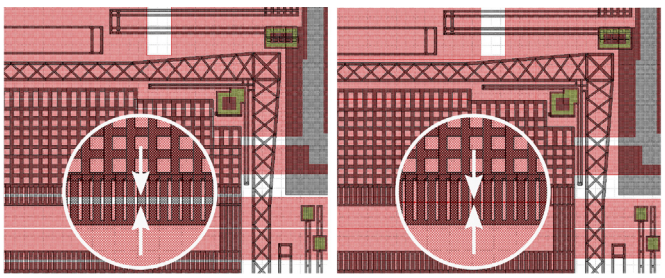
Fig. 24. Demonstration of the deflection algorithm from Section 4 on a 3-axis MEMS yaw-rate sensor. The algorithm consumes the chip geometry and the FEM data, and calculates a set of deflection states for the chip geometry.

5. Demonstration

We demonstrate our method on the 3-axis MEMS yaw-rate sensor shown in Fig. 23. A deflection range of −6 to +6 μm is selected for dynamic analysis. For this purpose thirteen electrostatic analyses, one every half micron, are executed (Fig. 24).

The demonstration sensor is fabricated with the layer configuration shown in Figs. 4 and 5. This process includes a thin poly-silicon layer (poly 1) mainly for the wiring and a thick poly-silicon layer (poly 2) for the mechanical structures. As described in Section 2, there are topography steps below the mobile mechanical structures (poly 2) where the poly 1 layer is structured (see the REM image in Fig. 4). For the demonstration we select a sensor variant with wide gaps between the wiring in the poly 1 layer (Fig. 25a) and one with small gaps (Fig. 25b). Consequently, there are bigger topography steps in the first variant with the wide gaps than in the second one.

The topography steps in the first variant cause dynamic capacitances as described in Section 2 (especially Fig. 5). Based on the formula for a simple plate capacitor, we expect a dynamic capacitance that increases approximately linearly until the topography steps have been shifted



(a) Segment of the demonstration sensor with wide gaps in the poly 1 layer. **(b)** Segment of the demonstration sensor with very small gaps in the poly 1 layer.

Fig. 25. Optimization of the gaps in the poly 1 layer of the demonstration sensor.

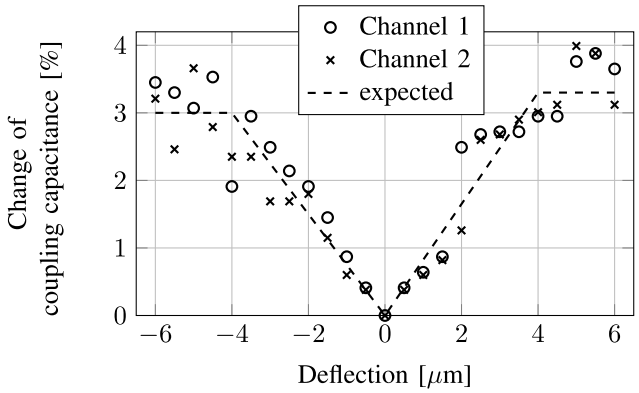


Fig. 26. The plot shows the dynamic capacitance caused by a topography step under a movable central electrode. The capacitance between a central electrode and an underlying detection electrode is plotted as a percentage with respect to the sensor resting position.

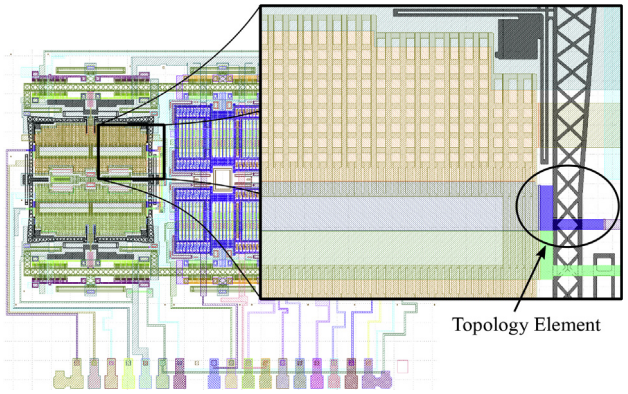


Fig. 27. The structure recognition of [3] applied to the demonstration sensor. The topology elements are shown in different colors. Each topology element will be reported as a sub net in the netlist. The extraction results can thus be back annotated to the chip geometry. (For interpretation of the references to color in this figure legend, the reader is referred to the Web version of this article.)

over the underlying structure. We expect that the dynamic capacitances caused by the topography steps will not change for higher deflection values (dashed line in Fig. 26).

We run our deflection algorithm with the classic electrostatic analysis software to extract the sensor's net-to-net coupling capacitances. Hence, as we want only to analyze the effects of the topography steps, we filter out all other dynamic effects by subtracting the extraction results for the two variants. Fig. 26 shows the dynamic capacitances between the moving electrode and an underlying electrode caused by the topography step. The result is plotted as a percentage with respect to the sensor resting position. The asymmetry in the result is caused by the small geometrical asymmetries in the polygon model.

We introduce a small design error to demonstrate the potential of the combined quasi-dynamic extraction procedure and recognition algorithm (Fig. 27).

If the sensor is deflected, the framework structure will move over the wire as shown in Fig. 28. Based on the formula for a simple plate capacitor, we expect the coupling capacitance to fall, as shown in Fig. 29 (dashed line). The simulated coupling capacitances (Fig. 29, circles) are a good fit with the expected values.

Additionally, we want to quantify the benefit of the combination of both methods in Fig. 29. Therefore, we add the net-to-net coupling capacitance of the original nets (Fig. 22) to the figure (gray crosses). The difference in the dynamic coupling capacitance in the positive and negative deflection range indicates the effect of the introduced defect. Fig. 29 also shows that other defects must exist, as the dynamic coupling

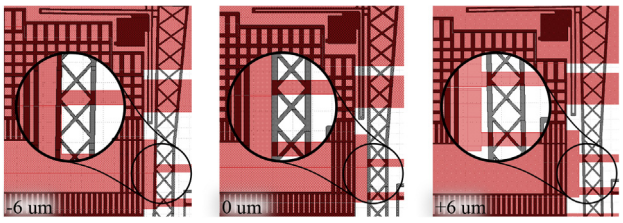


Fig. 28. The three images show how the framework structure moves over the defective wire. Left: the framework structure is over the wide wire and causes a high parasitic capacitance. Center: sensor in its position of rest. Right: the framework structure is over the narrow wire and causes a low parasitic capacitance.

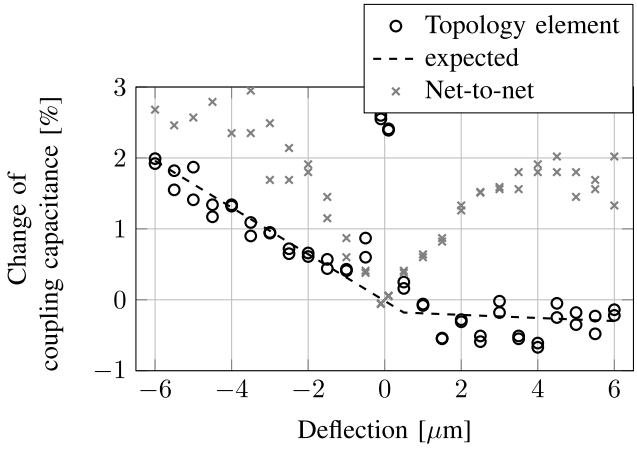


Fig. 29. The black circles in the plot present the dynamic capacitance in the symmetric channels caused by the defect shown in Fig. 28 of the marked topology element from Fig. 27. The transition between (partly) Manhattan to (complete) non-Manhattan structures occurs around the resting point. This causes field-solver inaccuracies which result in outliers around the zero deflection. The gray crosses show the dynamic capacitance of the entire net-to-net capacitance. The values are given in percentages of the entire net-to-net capacitance in the sensor resting position.

capacitance would otherwise have been somewhat higher during the negative deflection.

It is practically impossible to verify the extraction results with physical measurements due to the high number of side effects, like instrumentation, fabrication process variation and mechanical nonlinearities. The impact of these side effects on waveforms are orders of magnitudes greater than the effect we observe in the demonstration (Figs. 26 and 29). But by comparing physical measurements with the extracted data for a sensor at rest, we know that the deviation between the extracted, and measured coupling capacitances is on average on the order of five percent. Furthermore, we observe the expected results in the demonstration (Figs. 26 and 29). We aim to show with our new approach that we can detect very small dynamic parasitics that can affect the output signal. With our new method, these dynamic parasitics can be analyzed and afterwards manually minimized by changing the wiring.

6. Summary and outlook

The analysis of dynamic parasitic coupling capacitances can be integrated in the polygon-driven MEMS design flow with the dynamic analysis method presented here. We also showed that our dynamic analysis method can be supplemented with our detailed circuit-extraction algorithm from [3]. In special cases, like the simulation of the drive mode of a MEMS yaw-rate sensor, dynamic parasitic coupling capacitances can beneficially be integrated into the system model. This allows the effects of the dynamic electrostatic parasitics on the whole system, such as the positive feedback of the parasitic coupling capacitances to the mechan-

ical structures, to be analyzed.

In this paper we demonstrate our method for one critical dynamic parasitic caused by an in-plane shift of the dynamic structure (Section 2). In future work we will develop and expand our method to include the analysis of out-of-plane deflections, as they commonly occur in MEMS inertial sensors.

We demonstrated the method using a MEMS yaw-rate sensor, but the method can be adapted to any MEMS device provided the required FE-modal analysis and fabrication simulation data are available.

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Appendix A. Supplementary data

Supplementary data related to this article can be found at https://doi.org/10.1016/j.vlsi.2018.02.004.

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