Avoidance vs. Repair: New Approaches to Increasing Electromigration Robustness in VLSI Routing

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ABSTRACT

Studies on further IC development mutually predict that the reliability of future integrated circuits (ICs) will be severely endangered by the occurrence of electromigration (EM). The reason for the increasing number of EM damages are the ongoing structural reductions in the IC. Digital circuits are particularly at risk because they have been neglected in the consideration of EM, resulting in a lack of suitable EM measures. For this reason, a paradigm shift in physical design must be accomplished, complementing the traditional EM verification step after layout creation with a proactive EM-robust physical synthesis. This work presents the necessary adaptations and new approaches by modifying the routing step of digital circuits, resulting in an EM-robust routing result. Our contribution includes the development of EM models, the derivation of EM-suppressing measures, and finally the consideration of these countermeasures in an EM-robust routing process. In summary, our work is an important contribution to increase the EM robustness in digital layouts, thereby ensuring the reliability of future ICs.

1. Introduction

With each new technology node, the semiconductor industry continuously reduces the size of the structures within a semiconductor chip. This trend is mainly driven by the need to constantly develop faster and more complex integrated circuits (ICs). To achieve this goal, the integrated transistors and interconnects are continually being reduced in size to integrate more functionality on a given die area.

In recent years, the semiconductor industry has found it increasingly difficult to keep up with Moore's Law [51], which predicts a doubling of IC transistors every two years due to the downsizing of structures [35]. Lowering the structure sizes deteriorates the reliability of the ICs, as they tend to fail due to defects in their interconnects. Electromigration (EM) — a material transport triggered by the current flow — is a major threat to the reliability of future ICs [13].

Excessive current densities in the interconnects are the main reason of EM. These current densities cause an increased momentum transfer when the electrons collide with the atoms. Consequently, there is an increased chance that the atoms break out of their lattice position and start to migrate in the direction of the electron flow. In the worst case, the resulting damages lead to an increase in resistance and thus to the failure of the interconnects or the entire IC.

1.1. EM threat to the reliability of interconnects

Studies on future IC development (e.g., [21], [22]) mutually predict that the reliability of future integrated circuits will be severely endangered by the occurrence of EM. The reasons for the increasing EM threat in the integrated conductors are, on the one hand, the increase in current density over time and, on the other hand, a simultaneous lowering of the current density limits, as can be seen in Fig. 1. In recent years, it has been observed that the reduction in cross-sectional areas of interconnects is slowing down. However, the transistor currents are now increasing due to new technologies, such as fin field-effect transistors (FinFET). Thus, we observe a steady increase in current density and consequently also an increase in EM, as the thresholds continue to fall due to the structural reductions and the use of low-k materials.

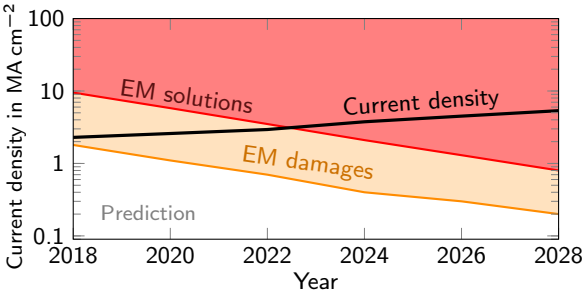

Figure 1: The threat to reliability by EM can be seen in the increase in current density (black) and the simultaneous lowering of the thresholds (yellow and red). At present, we are already in the yellow range, in which EM damages, e. g. voids, occur more frequently. We will enter the red range in a few years, where current, verification-based EM solutions are no longer applicable, resulting in a high demand for EM solutions that ensure IC reliability [21, 22].

1.2. Compensation of the EM in interconnects

Clearly, traditional measures such as interconnect widening or the use of new material are no longer available for the compensation of EM, as the first measure counteracts the trend towards miniaturization and the introduction of a new conductor material is associated with very high costs. Furthermore, currently applied EM verification after place and route cannot be used anymore as the predicted EM increase will cause EM-rule violations for too many nets. This makes subsequent corrections too time-consuming and may even be impossible due to the blocked routing resources.

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A further problem is that for the identification of critical locations usually only the current densities are compared with technological thresholds. At best, these thresholds exist for several discrete interconnect lengths. In the future, a more extensive consideration of the length is needed, otherwise too many vulnerabilities will be identified.

The overall goals of this work are (1) to increase the thresholds from Fig. 1 and/or (2) to lower the current density locally for critical interconnects. Both should ensure that the predicted current-density increase no longer poses a threat to the reliability of digital ICs (Fig. 2).

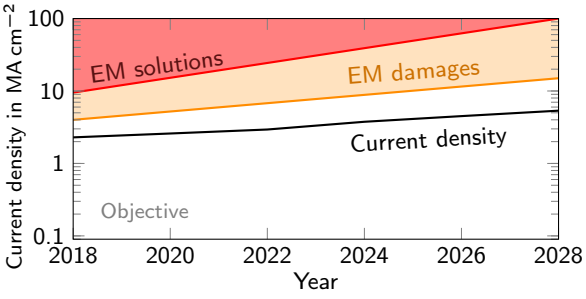

Figure 2: The anticipated increase in current density (black) from [21, 22] is to be compensated in this work either by raising the EM limits (yellow and red) or by lowering the current densities [4].

2. Electromigration

The following discussion of EM characteristics serves as the basis for the subsequent EM modeling, countermeasures and EM-robust routing presented in this work.

2.1. Development of EM-induced stress

EM is related to the electron wind force (F_{wind}) on the one hand and the electric field force ($F_{\text{el. field}}$) on the other hand (Fig. 3a). The electron wind force is generated when an electron collides with an atom. In this process, an impulse is transferred from the electron to the atom. The electric field force is created by the applied electric field. In the case of EM, the electron wind force is much higher than the electric field force because the electrons shield the electric field from the atoms [26]. Therefore, atoms migrate towards the anode. The measure of migration is the so-called atomic flux — indicating the number of atoms per time and area which move in the direction of the electron flow.

The transport of atoms by EM causes a change in concentration within the interconnect. This is responsible for the development of hydrostatic stress, since these two values affect each other [7, 27]. The hydrostatic mechanical stress is the average value of all mechanical stresses from the directions of the reference system. For simplification, hydrostatic mechanical stress is always abbreviated with stress in the remaining part of the work.

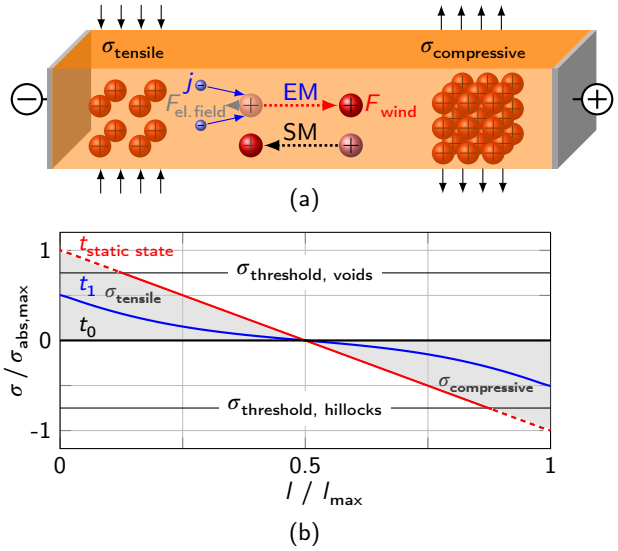

Figure 3: (a) EM displaces atoms and thereby enriches the anode or depletes the cathode. This change in concentration leads to tensile stress (σ_{tensile}) on the cathode and compressive stress ($\sigma_{\text{compressive}}$) on the anode. The resulting stress gradient in turn causes stress migration (SM), which counteracts EM. (b) The stress builds up over time (t_0, t_1, t_2) and increases until the stress gradient is large enough that EM and SM compensate each other ($t_{\text{static state}}$). EM damages occur when their thresholds are exceeded [4, 18].

The EM-induced material migration builds up the resulting stress. In this case, tensile stress occurs in the depleted cathode area and compressive stress in the enriched anode area. As a result of this stress gradient, stress migration occurs, which counteracts the EM.

The static state of the stress is only achieved if EM is fully compensated by stress migration (SM) and if this happens before a technological threshold is reached. In the literature, thresholds in the range of 41 MPa [16] to 400 MPa [19] are reported. If the stress exceeds these values before the static state is reached, EM damages will occur. This reshaping of the interconnect then causes a stress relief. It has already been shown by Blech in [5] that this process depends not only on the current density but also on the interconnect length.

2.2. Influence of the manufacturing process

The dual-damascene process (i.e., the commonly used manufacturing process of copper interconnects) builds up vias and interconnects simultaneously, so that diffusion layers are located below the vias and above the interconnects (Fig. 4). The barrier (mostly consisting of a tantalum compound [17]) and capping layers play an important role in the consideration of EM, because the migration of atoms is stopped at these films. The EM-relevant interconnect length can therefore only refer to the length within a routing layer, since no exchange of atoms takes place between the metal layers.

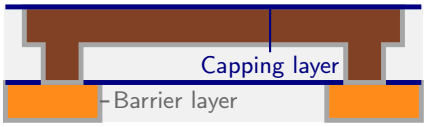

Figure 4: Structure of the vias and interconnects, which are manufactured in the dual-damascene process. The migration is blocked at the capping and barrier layers because the atoms cannot overcome these films.

The different thermal expansion coefficients of the materials can additionally induce stress in the interconnects [53]. This can result in a so-called rest stress, which reduces the stress required for EM damages [11]. This rest stress is usually a tensile stress, so that the void formation is predominant [30, 33]. In the literature, values in the range of 50 MPa [39] up to 400 MPa [20] are reported.

2.3. Occurrence of EM in signal nets

Typically, the EM analysis is based on the direct current value for direct currents (DC), the average current value for pulsed alternating currents, and the average current recovery value for alternating currents (AC) [14]. In this work we focus on the last model because of its conversion of alternating currents into an equivalent direct current taking into account the recovery effect. It is used because the focus here is on the EM compensation in signal nets of digital circuits, which have been neglected for a long time. This average current recovery model of [50] and its further refinement in [29] is widely applied for EM modeling of alternating current loads [47]. It describes a current density recovery value, which contains a recovery factor (ranging from 0.7 [29] to 0.9 [50]) for the self-healing effect. Self-healing describes the effect that the change in direction of the current causes the migrated atoms to return and thus heals the EM damage. Experimental investigations confirm that this effect is incomplete [32, 48, 29].

Liew et al. [32] state the directional influence of grain boundaries as an essential reason for the incomplete self-healing. A further point is the superposition of the dynamic switching current with the static leakage current. These leakage currents can no longer be neglected as they are now in the order of magnitude of the dynamic switching currents [25]. Guan and Marek-Sadowska [13] also mention the increased current densities due to a change of direction in the interconnect (e.g., caused by vias) as a reason for incomplete self-healing. This leads to increased local heating, which in turn causes an uni-directed atomic flux. Another cause is the difference between the charging and discharging curves of a net. As a result, the duration and the maximum current between charging and discharging are different. All these arguments can lead to an uni-directed atomic flux even under alternating current loads.

2.4. Consideration of EM in physical design

EM in digital circuits has been neglected for a long time because the EM danger of AC loads was significantly lower than the danger associated with DC loads [29]. Due to this negligence of EM in (digital) signal nets, there are only very few approaches available which can be used to avoid EM in digital circuits. One measure was proposed by De Paris et al. in [12], where critical interconnects are widened by defining boundary conditions in the routing step. A similar approach is found in [55]. In this work, the width of the interconnect is adjusted with respect to the current. Furthermore, there are studies (e.g., [31], [54], [24], [9]), which also change the width or the connections with respect to the expected current. However, these approaches are unsuitable for the routing of signal nets, as they neglect the interconnect length and counteract the trend of miniaturization. Indirectly, the studies [37] and [38] deal with the compensation of EM in the routing. The authors show that the position of the connection point on the standard cell influences the EM within the cell pin. In summary, there is a clear lack of measures and procedures for the compensation of EM in digital circuits.

3. Contributions of this work

As we discussed in Sect. 1, the emerging EM problems require a paradigm shift in physical design, complementing the traditional post-layout verification of EM robustness with a proactive EM-robust physical design (Fig. 5).

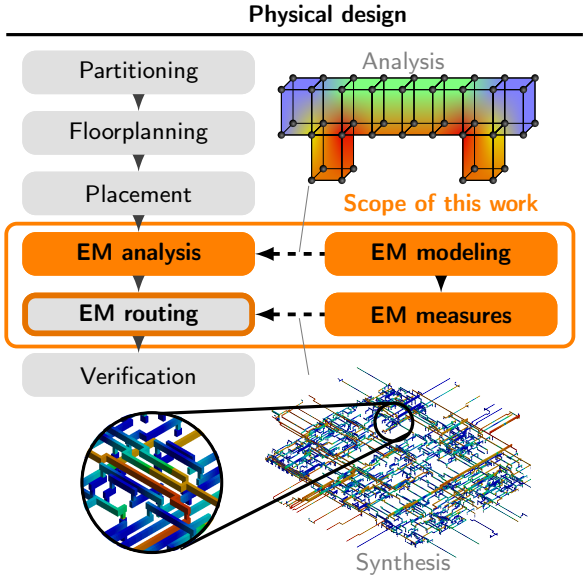

Figure 5: Our extension of the physical design methodology to include a proactive consideration of EM in the routing step.

The necessary adjustments can be split into the following three steps, which are the main contributions of this paper:

1. A tailored EM modelling for the development of countermeasures in routing structures and a fast EM analysis for the integration into the physical design of large digital circuits,
2. The implementation of appropriate countermeasures to avoid EM in signal lines, and
3. A verification of these EM measures in an EM-robust routing step.

These contributions are described in detail in the following Sects. 4, 5 and 6.

4. Modelling of EM in routing structures

Due to the complexity of digital circuits, there is a need for an EM model which is specifically designed for digital routing structures. The modelling of EM in these elements can be approached from "two ends" with opposing requirements: from the perspective of countermeasures or from the routing process. The investigation of countermeasures requires the most accurate modelling of the migration processes. In contrast, the time-consuming routing demands the fastest possible analysis. As a solution (and outlined next), we use the finite element method (FEM) for the development of countermeasures and then apply an adapted EM analysis with certain simplifications in the routing flow.

4.1. FEM model for routing structures

An essential advantage of FEM is the applicability for different physical domains [45]. Thus, different influencing factors can be coupled with each other and their mutual dependencies can be investigated. Due to its diversity, FEM is often the basis for empirical EM models as shown in [46], [49] and [52]. However, standard discretization algorithms often provide too many elements in the relatively simple routing structures, turning computation time into a problem. Therefore, we suggest that the layout tool itself does the discretization using our algorithm presented in [1], which is specifically tailored for routing structures (Fig. 6). This algorithm integrates the discretization step into the routing tool, thereby significantly reducing the analysis effort.

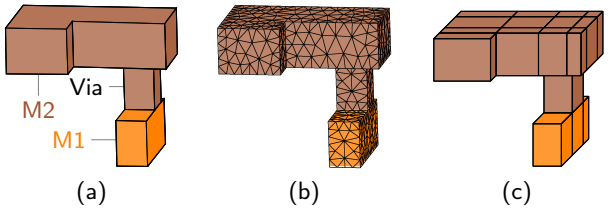

Figure 6: The discretization of the routing structure in (a) results in a significantly higher complexity with the standard algorithm of a FEM suite in (b) than with the adapted algorithm of [1] in (c) [1].

The discretization algorithm from [1] follows the approach of reducing elements at insignificant points. Within a straight interconnect, the current density can be well mapped with only one element. At the same time, the error in the stress build-up is greater, since the curved shape from Fig. 7 is at best interpolated by a straight line. However, this error decreases with the approximation to the static state of stress through the formation of a linear characteristic. Thus, the advantage of a small number of elements outweighs the disadvantage of the error in the time-based stress build-up, since this error is not present in the calculation of the stress maximum. Figure 7 also verifies the stress results as they show the same behavior as the known analytic solution from Korhonen et al. [28].

In order to investigate the influence of current density and interconnect length on the stress curve, Fig. 8 depicts an

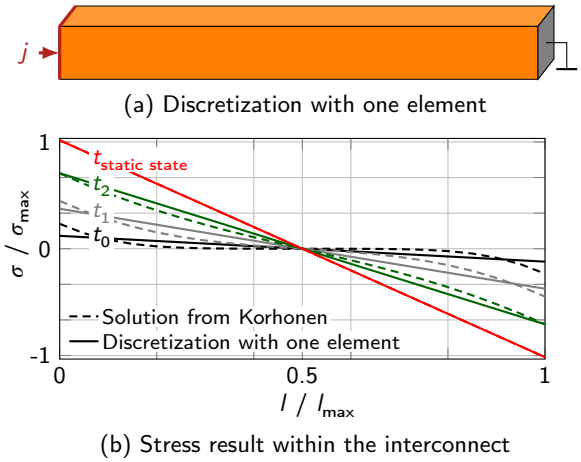

Figure 7: The interconnect in (a) is only discretized by one element. For this reason there is always a linear stress curve in (b) compared to the analytic solution from [28]. The error of this approximation decreases with time, as the curve approaches a linear function in static state.

interconnect with halved current density and one with halved length, both compared to Fig. 7. This comparison allows two conclusions: (1) Lowering the current density reduces the stress at all times. (2) Reducing the length keeps the temporal development of the stress constant, but also reduces the stress maximum in the static state. Hence, we can conclude that EM measures for the digital routing process must reduce either the current density, the interconnect length, or both. This conclusion is consistent with the general understanding of EM, however, the current routing process lacks a profound consideration of this. Furthermore (and not less important), the reduction of static stress can be used as an assessment for the development of countermeasures.

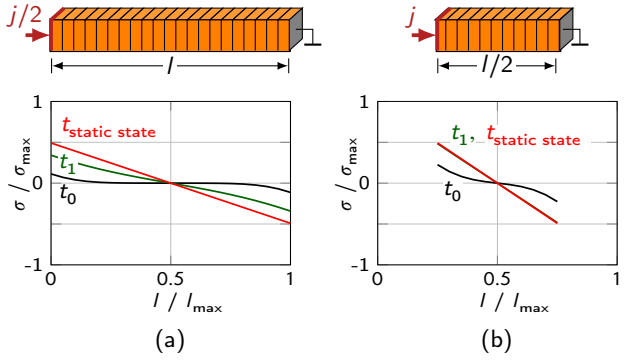

Figure 8: The stress from the current density and interconnect length from Fig. 7 serves as a reference to investigate the change in the time-dependent stress for a halved current density in (a) and a halved interconnect length in (b). It is noticeable that the maximum stress in the static state changes linearly with the reduction of the current density and the interconnect length.

4.2. EM analysis for physical design

As outlined earlier, physical design requires an appropriate EM analysis. Therefore, the concept of reducing discretization points must be extended to shorten the analysis

time further. For this we propose to represent the net as a graph and use Sun's approach [43, 44] to calculate the static stress. The calculation equations for EM-induced stress can be found in references [43, 44]. The vertices of the graph are located at each pin of the net, below and above vias, and at directional changes within a plane. The edges represent the interconnects and vias, with the directions pointing from the output to the input pin. The currents in the edges can then be calculated based on the capacities of the interconnects and pins to be charged.

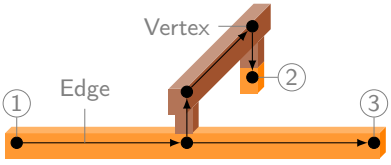

Figure 9: Three-dimensional representation of a net and its pins (1, 2 and 3) in a graph to accelerate the EM analysis for integration into the physical design.

To validate the efficiency and correctness of our EM analysis, the results for a branched tree are compared with a verified stress analysis by FEM. As depicted in Fig. 10, the stress results are very similar (i.e., the average and maximum deviation is in the single-digit range). The small difference is due to the simplification of our EM analysis which neglects, for example, the exact via sizes.

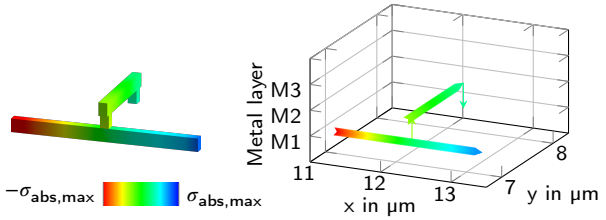

Figure 10: Stress determined from the conventional FEM analysis in (a) and our suggested EM analysis in (b) with normalization to the same absolute stress maximum ($\sigma_{abs,max}$). The colouring proves that the results are comparable.

It can be concluded from Table 1 that our EM analysis is much better suited for the routing process than the (conventional) FEM analysis due to the enormous acceleration of the total running time by almost six orders of magnitude.

Table 1
Complexity and runtime of FEM and EM analysis.

Analysis	Vertices	Time per net	Total time
FEM	149133	8 s	41 min
EM	3598	<1 ms	25 ms
Factor			98400 x

5. Measures for electromigration avoidance

The countermeasures presented here adjust and extend the measures from [4] to increase the EM robustness of a layout during the routing step of digital circuits. Some measures, such as the insertion of reservoirs or redundant vias, can be implemented as a post-routing step. Although the measures are specifically designed for digital routing, they can also improve analog layouts.

5.1. EM net ordering

The literature contains various approaches to determine the optimal net order, such as sorting the nets by the number of pins, the length or a combination of both [23]. In this work, the net ordering is to be determined with regard to the EM danger. The idea is to route EM-relevant nets at an early stage so that their solution space is as large as possible. This facilitates the implementation of countermeasures by maximizing the available routing resources for the EM compensation.

The problem here is that only the routing determines the EM robustness of a net, hence, the EM danger cannot be estimated without the routing. For this reason, we propose to estimate the routing and, based on this, to determine the EM danger of the nets and sort them in descending order. The steps in Fig. 11 precede the routing process.

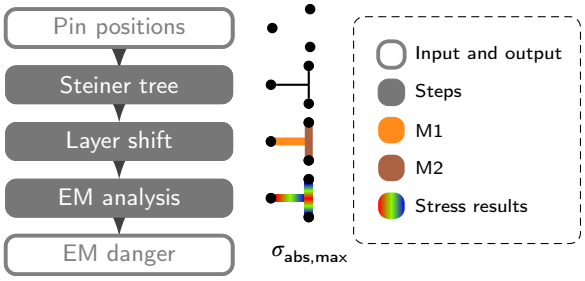

Figure 11: Estimation of the EM danger for each net with the pin positions, which are transferred to a Steiner tree determination [10]. Afterwards, the vertical and horizontal connections of the tree are shifted to the first and second layer, respectively, to simulate EM-important layer changes. The EM-danger for each net is determined with the EM analysis describe in Sec. 4.2. on the basis of the absolute stress maximum ($\sigma_{abs,max}$).

5.2. Net topology improvement

The net topology has a significant influence on the stress development and thus on the EM robustness of a net, as it allows both the current density and the interconnect length to be controlled. Our approach is to reduce the current density by providing independent paths to each pin by a "star-routing methodology". Figure 12 provides an example of this by comparing the Steiner tree and star routing for a 4-pin net.

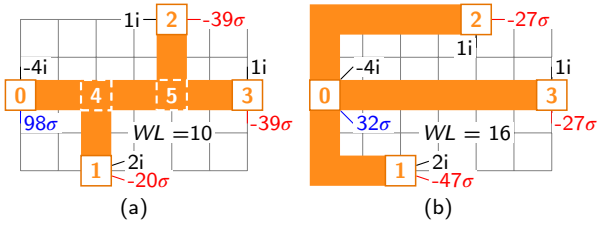

Figure 12: Resulting stress values (σ) and wiring lengths (WL) for the Steiner tree in (a) and the star routing in (b) based on the currents (i) at each pin (0, 1, 2, 3). The routing in (b) reduces the stress by more than half compared to (a) [3].

5.3. Length limitation

Another promising measure is to limit the length of the (longest) interconnect segments (within one routing layer) of a net. As already mentioned in Sec. 4, this length has a decisive influence on stress – the longer the interconnect, the higher the stress. The approach of this measure is a targeted shortening of the longer segments by introducing or shifting of layer changes (vias). With this, maximum stress values per net are reduced and the layout remains routable as the overall routing topology is maintained.

Figure 13 shows an example where adjusting the interconnect lengths on the different routing layer increases the EM robustness of the net by reducing the maximum length.

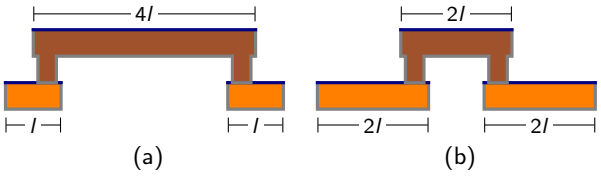

Figure 13: The greater maximum length in (a) results in a higher EM danger than the balanced lengths in (b).

In critical cases, additional layer changes can also be introduced to reduce the interconnect length and, thus, also the risk of EM (Fig. 14).

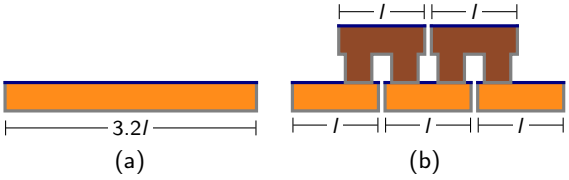

Figure 14: Reduction of the length from (a) by additional layer changes in (b) and thus also a lowering of the EM danger.

5.4. Cross-sectional area widening

In digital layouts, the signal lines are implemented with minimum width and distance from each other, so that any widening blocks several tracks. For this reason, it is recommended that interconnect widenings are only introduced at EM-critical points. Keeping this in mind, we reduce the current density by widening the cross-sectional area of the interconnects. If one wants to exploit the positive effect of a widened interconnects without the disadvantage of blocking resources, we suggest moving the EM-relevant interconnects to higher layers with larger cross-sectional areas (if one is available in the vicinity, Fig. 15).

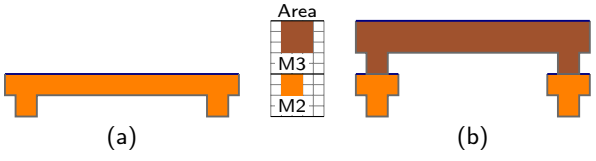

Figure 15: (a) The critical interconnect on M2 is shifted to M3 in (b), since a larger cross-sectional area is available on M3. This reduces the current density and thus the EM risk.

5.5. Reservoir insertion

It has been known for a long time that reservoirs on interconnects can have a positive influence on EM robustness. Three guidelines (derived from the basic rules given in [4]) can be followed to find the optimal reservoir (Fig. 16): (1) If the reservoir is to reduce tensile stress, it must be also located at a tensile stress location because the interconnect stress will be shifted towards compressive stress (and vice versa), (2) the higher the stress on the reservoir, the more effective it becomes, and (3) the longer the reservoir, the greater its influence. A calculation formula for the optimal reservoir length and further information can be found in [3].

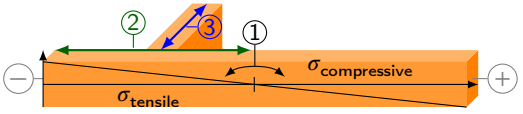

Figure 16: Reservoirs at tensile stress locations shift the interconnect stress towards compressive stress (and vice versa, 1). The influence of the reservoir increases with the stress at the reservoir location (2) and the reservoir length (3).

5.6. Redundant via insertion

Redundant vias can increase reliability by providing redundancies for an existing via, such as reduced current load. Usually the objective is to insert as many redundant vias as possible. For example, Pak et al. [36] consider the current density for EM compensation. However, this is insufficient because, as mentioned before, the length is not taken into account. Therefore, we propose to use the procedure from [2] to consider the EM danger in the form of "via load" which we define as the stress at the layer change location divided by the number of vias placed at this location.

The procedure consists of the following steps: (1) Determination of possible redundant vias, (2) transformation of these into a conflict graph as vertices and mark dependencies as edges, (3) weighting of each vertex regarding the improvement of the via load and (4) transformation of the conflict graph into an integer linear optimization to determine the most important redundant vias. We recommend to use a quadratic or even cubic weighting function, so that the focus lies on the reduction of high loads. In other words, the higher the stress on a via, the more likely it is to fail and the more important it is to provide redundancy. To demonstrate the general approach, Fig. 17 contains a simple layout example.

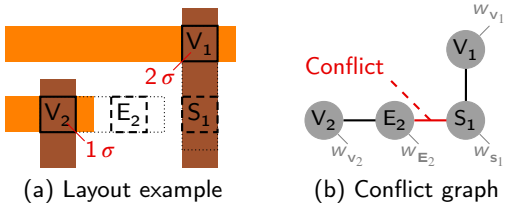

Figure 17: (a) It is possible to use either a redundant via in the south of via 1 or in the east of via 2. (b) Since the via load at via 1 is twice as high as at via 2, the weighting (w) of vertex S_1 is higher than E_2, so that S_1 is preferred over E_2.

6. Electromigration-robust routing

Next, we present an adapted routing procedure which increases the robustness of a layout against EM. It uses the presented EM analyses and measures from the previous sections. The increase in EM robustness in the layout is verified for each countermeasure, so that the strengths and weaknesses of the individual measures are identified.

6.1. Procedure steps

The developed EM-robust routing of this work relies on the established separation between global and detailed routing, whereby only the sequence of the detailed routing is changed to compensate EM (Fig. 18).

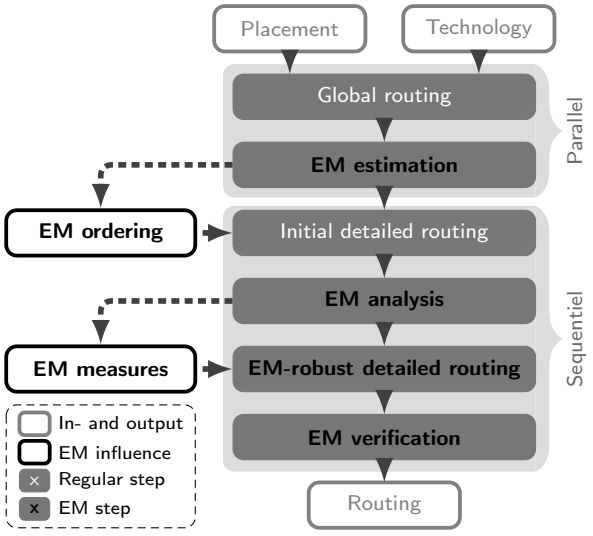

Figure 18: Modifications of the routing procedure to consider EM. Several steps like EM estimation, EM analysis or EM-robust detail routing are added. Additionally, the EM net ordering and the EM measures influence the routing step.

Starting point for the procedure are the placement and technology data, which are transferred to the global router. After the global routing is completed, a first EM consideration is made in the estimation step, which determines the order of the nets according to their EM danger. This order is subsequently used for the sequential routing of each net. The initial detailed routing delivers a valid routing result without EM consideration. The subsequent EM analysis determines the stress in this initial solution and compares it with the absolute stress maximum of all currently routed nets. If the analysis finds critical interconnects (i.e., the load is more than 90 % of the existing stress maximum), the EM-robust detailed routing uses countermeasures to reduce the EM danger. Finally, the reduction of stress is examined in the verification step (and changes are reversed if necessary). The reason for the existence of an initial routing is due to the fact that only a few interconnects are critical. Hence, only at these locations it is necessary to deviate from conventional routing.

6.2. Implementation details

The chosen routing concept is based on a sequential grid router, which determines the path of a net in a detailed graph by means of A* path search algorithm [15] following the preferred routing direction. The advantage of this concept is the good adaptability, e.g. by dynamic changes of the graph or adapting the path search by influencing the residual cost heuristic in the algorithm. If no path can be found, we try to solve the conflict by extending the search space, disregarding preferred directions, or by ripping-up and re-routing nets.

In this work, the routing resources are mapped in a detailed routing graph, which allows different track spacings on the individual layers (Fig. 19). The vertices in the graph represent points in the layout where two tracks from adjacent layers virtually cross. Each vertex knows its neighbors located above and below. The neighbors within a plane can be calculated based on the current location and the regularity of the graph. In addition, it is implicitly assumed that all edges between adjacent vertices exist as long as they are not explicitly excluded in a separate list. This saves memory, since considerably more edges exist than are missing.

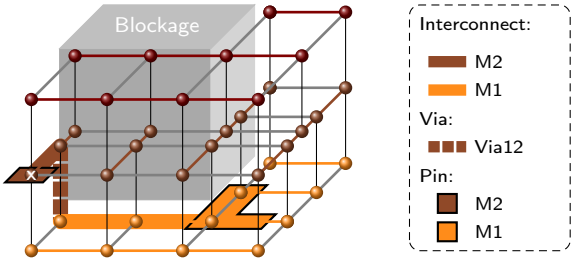

Figure 19: Representation of the routing resources by vertices and edges in the graph. Vertices are created at virtual intersections of two tracks on both levels and edges between adjacent vertices. Interconnects and vias of a net are determined using an A* algorithm between the pins.

The basis of our approach is a C++ implementation that integrates external libraries. One of these is the parser of [40], which is used to read and write the layout data. Furthermore the boost library is employed, which provides important basic functions [6], such as tests for overlaps of shapes. Especially the handling of layout geometries with the "boost::polygon" programming interface is highly efficient, because the geometric operations are already optimized for rectangular shapes. A single core of an Intel Xeon E5-2620 at 2.40 GHz with 48 GB of RAM has been used (and needed) to obtain our results.

6.3. Routing results

The routing results are given in the first three columns of Table 2. They are comparable to the state-of-the-art from [42]. The routing time, wiring length (WL), and via number are of the same order of magnitude. Deviations are comprehensible, since the objective here is to reduce the EM-induced stress by an EM-robust routing, whereas the works in [42] aims at reducing the routing time, wiring length, and via number. We do not claim to realize the shortest wiring length or number

Table 2
Change of wiring length (WL), via count and absolute stress maximum ($\sigma_{abs,max}$) from initial to EM-robust routing with the countermeasures. The delta values are given in percent.

Bench-mark	Initial routing Time in min	WL in m	Vias in 10^3	EM-robust routing: Net topology ΔWL	ΔVias	$\Delta\sigma^{abs,}_{max}$	Length limitation ΔWL	ΔVias	$\Delta\sigma^{abs,}_{max}$	Cross-section widening ΔWL	ΔVias	$\Delta\sigma^{abs,}_{max}$	Reservoir[1] ΔWL	ΔVias	$\Delta\sigma^{abs,}_{max}$
test1	1	0.2	51	7.48	3.45	-49.16	0.02	0.43	-68.49	0.00	0.00	0.00	0.60	0.67	-28.71
test2	26	3.8	540	3.03	1.65	-29.81	0.00	0.00	-59.80	0.00	0.01	-4.74	0.00	-0.03	-11.85
test3	28	3.6	521	1.18	0.09	-9.98	0.00	0.38	-76.29	0.00	0.00	0.00	0.02	0.02	-6.10
test4	190	5.4	1063	10.96	2.64	-49.36	0.01	0.12	-33.62	0.00	0.00	-33.62	0.00	-0.02	-2.61
test5	138	5.6	1202	14.14	3.71	-28.47	0.01	0.06	-43.33	0.00	-0.01	-26.84	0.01	0.00	-3.65
test6	169	7.3	1816	17.83	4.41	-61.77	0.00	0.00	-39.59	0.00	-0.06	-49.52	0.00	0.00	-2.67
test7	318	13.3	2925	2.04	0.01	-38.74	0.00	0.04	-36.55	0.00	0.00	-50.16	0.00	0.00	-5.60
test8	365	13.3	2943	0.62	0.13	4.20	0.00	0.04	-48.81	0.00	-0.01	-49.88	0.00	-0.01	-2.71
test9	358	11.1	2925	1.25	0.24	-24.42	0.01	0.08	-67.36	0.00	-0.06	-60.02	0.00	0.01	-6.66
test10	409	13.8	3308	0.22	0.22	-31.39	0.00	0.04	-66.43	0.00	-0.03	-53.95	0.00	-0.05	-2.83
Average:				5.88	1.66	-31.89	0.01	0.12	-54.03	0.00	-0.02	-32.87	0.06	0.06	-7.34

of vias but a much more EM-robust solution. We strongly believe that in the future more routing resources will have to be spent to ensure reliability.

The following sections contain the results obtained on the basis of the ISPD benchmarks [34]. The outcomes of the net ordering refer to the quality of the EM danger estimation. The results of the net topology improvement, length limitation, cross-sectional area widening, and reservoir insertion relate to the percentage changes in wiring length, via count, and absolute stress maximum given in Table 2. The first two metrics represent the price to pay to reduce the EM risk identified by the absolute stress maximum. The use of this term ($\sigma_{abs,max} = \max(|\sigma_{min}|, \sigma_{max})$) allows the improvement of EM robustness to be expressed by a single value. In addition to Table 2, an example net is shown in the initial and EM-robust routing. We would like to refer to [2] for the results of redundant vias, as they are obtained on a different benchmark set that is tailored for redundant vias. The via insertion is performed after the interconnect routing. It improves the via load by an average of around 4 % compared to [8].

6.3.1. EM net ordering

An important point in changing the routing order with respect to EM danger is the correlation between the rank of a net from the estimation and the rank after routing. A good correlation means that the net ordering reflects the EM danger well. This can be verified with the Spearman method [41], where a rank correlation coefficient (rs) close to one indicates a strong correlation. In the ISPD benchmark, the coefficient is always in the range between 0.973 and 0.982, which proves a good correlation, as can be seen in Fig. 20.

6.3.2. Net topology improvement

The values in Table 2 column 7 show that this measure significantly reduces the absolute stress maximum by an average of about 32 % and thus also the EM danger. However,

[1] Assumption of 200 MPa rest stress from manufacturing process.

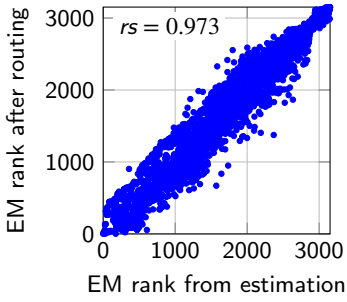

Figure 20: Correlation of the EM net order from the estimation before and the result after routing for test1.

columns 5 and 6 also indicate a growing demand for routing resources. The reason is the star net model, which increases the need for resources with the number of pins. Moreover, the improvement may vary between the benchmarks. In test8, the absolute stress maximum is increased. Here, the most critical net is mostly influenced by its length, which is increased by the EM routing. This indicates that this measure is more suitable when the current densities are decisive for the stress. From Fig. 21 can be seen that the EM routing visibly consumes more resources than the initial routing, but the stress is also significantly reduced.

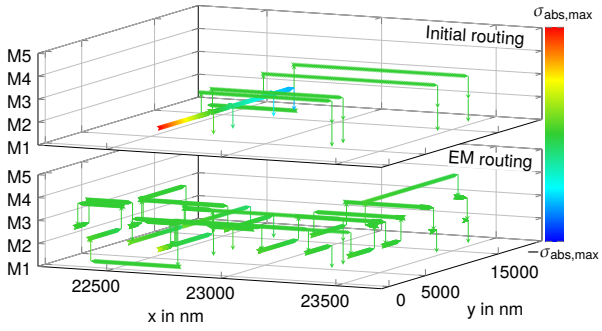

Figure 21: Stress in the example net for initial (top) and EM-robust routing (bottom) with improved net topology.

6.3.3. Length limitation

As shown in Table 2 column 10, limiting the interconnect length can greatly reduce EM-induced stress in the layout. This allows the absolute stress maximum in the ISPD benchmarks to be reduced on average by approx. 54 %, coupled only with a very small increase in the wiring length and via count (column 8 and 9). Figure 22 also shows that the initial and EM-robust routing differ only slightly. Only the most heavily stressed interconnect uses an additional track at two points. However, the absolute stress maximum can be significantly reduced by the introduced layer changes.

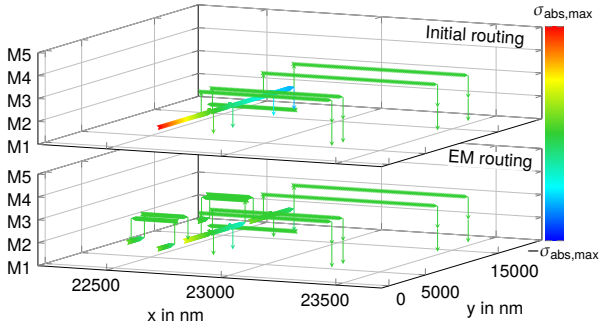

Figure 22: Stress in the example net for initial (top) and EM-robust routing (bottom) with limited length.

6.3.4. Cross-sectional area widening

The results in column 13 of Table 2 show that widening the interconnect significantly reduces the absolute stress maximum. However, the extent of the stress reduction is strongly dependent on the differences in the available cross-sectional areas in the metal stack. The stress improvement cannot be realized if the critical interconnect is already at the highest layer or the displacement is not possible due to blocked resources above. A positive aspect of using this EM measure is that the required routing resources remain largely constant. The slight decrease in the number of vias also indicates that, from a routing point of view, it may make sense to use the higher routing layer at an early stage. In the example net from Fig. 23, the reduction of stress can be clearly seen, which is due to the displacement of the critical interconnect by two layer upwards. However, one can also see that the vias have to be adjusted due to the displacement.

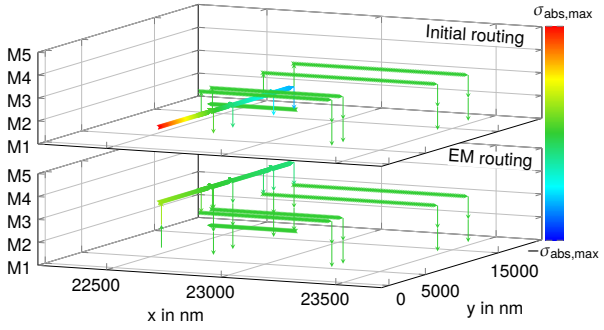

Figure 23: Stress in the example net for initial (top) and EM-robust routing (bottom) with a shifted interconnect.

6.3.5. Reservoir insertion

The values in column 16 of Table 2 show the improvement of the absolute stress maximum for the existence of 200 MPa rest stress from the manufacturing process. This perfectly illustrates the benefits of this countermeasure, as it can compensate for uneven stress profiles. Note that uneven stress profiles can also be created without rest stress, but occur much less frequently, since this requires the presence of an intersection on an interconnect. The columns 14 and 15 of Table 2 also show that the reservoir insertion needs more routing resources. The coloring of the EM-robust routing for the critical path from Fig. 24 indicates that the reservoir weakens the red tensile stress and increases the blue compressive stress. This leads to a reduction of the absolute stress maximum as the interconnect stress shifts towards compressive stress.

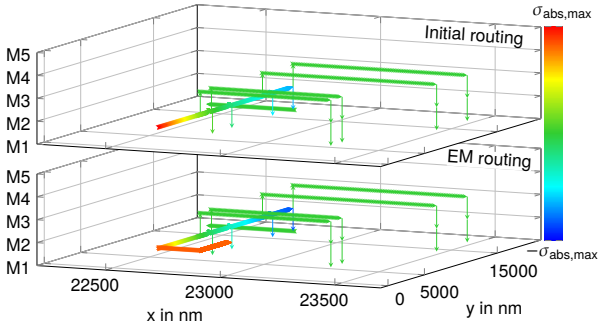

Figure 24: Stress in the example net for initial (top) and EM-robust routing (bottom) with a inserted reservoir.

7. Summary and outlook

As outlined in Sect. 1, the reliability of digital circuits and its interconnects is increasingly threatened by the occurrence of EM. It is therefore important to perform a paradigm shift in physical design, complementing the traditional EM verification step (after layout generation) with a proactive EM-robust physical design. The routing step offers the greatest potential for this, as it determines the geometry of the EM-critical interconnects. In this work, three steps are presented to achieve this goal: (1) The creation of an EM model for digital interconnect structures, (2) the derivation of EM measures from the model, and (3) the implementation of these measures in an EM-robust routing (Fig. 25). This approach proved to be extremely useful for increasing the EM robustness in digital layout as the results show a significant reduction of the hydrostatic mechanical stress, which is our indicator for EM-criticality. Thus, this work provides an important contribution to the interception of the emerging EM problems. At the same time, we would like to emphasize that EM compensation will never be free of charge, as other factors such as signal integrity or timing may suffer. Finding a compromise for these conflicting requirements remains the next step.

Future work should expand the proactive EM-robust physical design methodology developed here, so that layout reliability can be further improved. Examples are the consid-

eration of EM indicators in placement and the inclusion of thermal migration as well as other sources of (mechanical) stress, such as through-silicon vias (TSVs). The continuation of this work will also address the question of when to use which countermeasure and how these can possibly be combined. Besides a continued validation of our results with practical lifetime measurements, the task is to integrate these new adaptions into commercial design tools. We look forward to seeing this proactive approach towards better layout reliability adopted and extended by the physical design community.

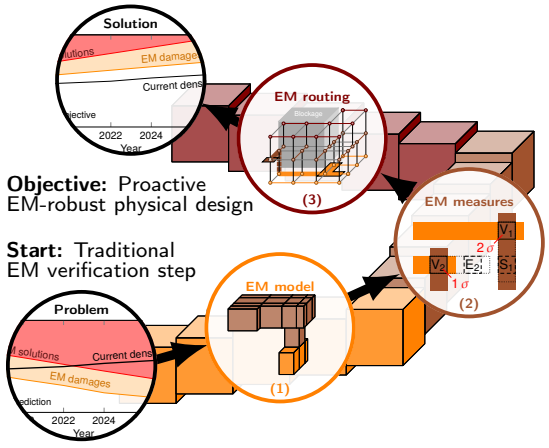

Figure 25: The three following (and presented) steps are the proposed approach to find a solution for the emerging EM problems by proactively increasing the EM robustness in the routing of digital circuits: (1) Setting up an EM model for digital interconnect structures, (2) deriving EM measures, and (3) using these countermeasures in an EM-robust routing.

CRediT authorship contribution statement

Steve Bigalke: Conceptualization, methodology, software, validation, investigation, writing – original draft, visualization. **Jens Lienig:** Writing – review & editing, resources, supervision.

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