Reliability by Design: Avoiding Migration-Induced Failure in IC Interconnects

Susann Rothe, Jens Lienig
Dresden University of Technology, Institute of Electromechanical and Electronic Design (IFTE), Dresden, Germany
susann.rothe@mailbox.tu-dresden.de, jens@ieee.org

***Abstract*—The reliability of integrated circuits is increasingly endangered by migration-induced degradation of metal interconnects. The risk of failure due to migration is not only rising in every new technology node, it is also constraining the miniaturization of interconnect structures. In addition to DC lines, such as power delivery networks, signal and clock lines are increasingly being degraded by migration. This paper summarizes our current knowledge in avoiding migration-induced integrated-circuit failures. After introducing and discussing migration mechanisms, we focus on the growing electromigration susceptibility and the increasing influence of thermal migration. Looking forward, we review novel IC design strategies that incorporate migration constraints and mitigation measures into layout synthesis.**

***Index Terms*—Electromigration, Stress Migration, Thermal Migration, Reliability, Physical Design, Migration Robustness**

I. Introduction

Designing reliable integrated circuits (ICs) without sacrificing performance and increasing power or area remains a key challenge in modern semiconductor technologies. Migration-induced degradation of metal interconnect lines is not a new concern but its severity is on the rise as technology nodes get smaller. This is because current densities are increasing while the boundary values for migration robustness are tightening, as shown in Fig. 1 [1]–[4]. Additionally, migration mechanisms are getting more complex and are affecting a wider range of nets. Hence, migration robustness has become a design issue and is addressed at various stages in IC design and fabrication nowadays. In physical design, which this paper focuses on, current density verification of power grids and DC lines is used to find any electromigration (EM) violations. However, this is not sufficient anymore to ensure migration robustness [2].

State-of-the-art research focuses on EM assessment of large power delivery networks (PDNs) [5]–[7]. PDNs are composed of a large number of branches and can include meshes as well, so that accurate and time-efficient EM modelling is extremely challenging here. Another issue is that in advanced technology nodes signal and clock nets also suffer from migration-induced failure [8]. Moreover, thermal effects are gaining in significance and must be considered [9]. To make matters worse, the growing migration susceptibility of interconnects also leads to a surge in the number of violations detected during verification.

The aforementioned problems show that accurate modelling methodologies for migration processes as well as novel design strategies are urgently needed. An important first step in this direction has been made recently with the paradigm shift from current density-based EM assessment to the physics-based calculation of hydrostatic stress evolution. However, more advances are needed as, for example, post-layout *repair strategies* will not be feasible for IC design in leading-edge technologies going forward. Hence, novel *proactive*, i. e., pre-layout, approaches for migration consideration, such as in [10], [11], are evolving (Fig. 2).

Successfully mastering these challenges requires sound knowledge of migration mechanisms and avoidance strategies in VLSI design. This is where this paper comes in. Its contribution is a thorough review of the state-of-the-art methodologies for VLSI migration avoidance in order to guide future research in achieving migration-robust and, hence, more reliable ICs.

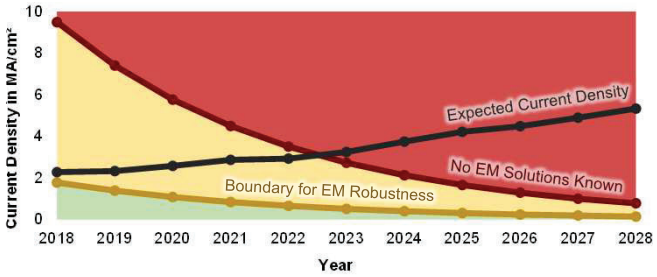

Fig. 1. Current densities and EM boundary values prognosticated by the 2015 ITRS [3]. There is no risk of EM degradation in the green area; and in the yellow area, EM degradation occurs but can be handled. As for the red area, there are no known solutions for EM-robust layout design.

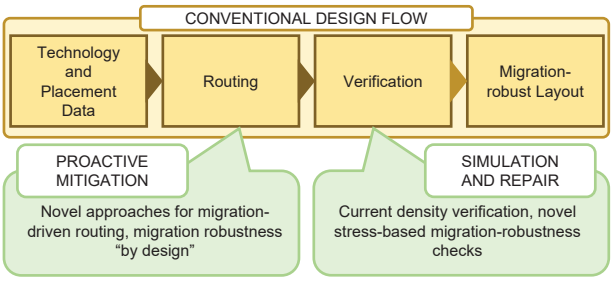

Fig. 2. Migration robustness can be addressed at various stages in the physical design flow: Traditionally, it is checked in the verification step. Novel approaches implement migration constraints earlier – that is, in layout synthesis, e. g., in the routing step.

978-1-6654-8128-1/22/$31.00 ©2022 IEEE

Please cite as: S. Rothe, J. Lienig: "Reliability by Design: Avoiding Migration-Induced Failure in IC Interconnects," Proc. Symposium on Integrated Circuits and Systems Design (SBCCI), August 2022, Porto Alegre, Brazil

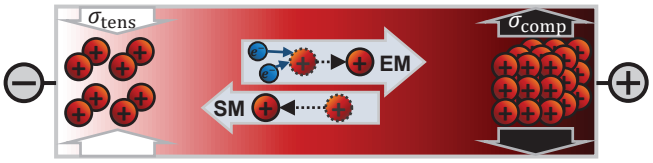

Fig. 3. Atomic motion due to EM leads to tensile stress at the cathode and compressive stress at the anode of an interconnect. The counteracting SM partly reverses this process.

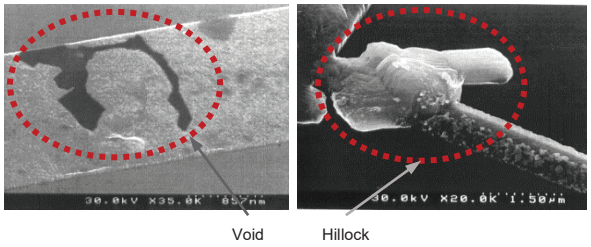

Fig. 4. Voids (left) and hillocks (right) can cause interconnects to fail (photographs courtesy of G. H. Bernstein und R. Frankovic, University of Notre Dame).

II. Migration Mechanisms

There are three major migration mechanisms that determine material movement within metal interconnects in ICs: *Electromigration* (EM), *thermal migration* (TM), and *stress migration* (SM). EM was considered the main driving force behind wire degradation in the past. TM has been neglected up to a few years ago but is gaining importance in state-of-the-art IC design. SM is mostly taken into account as the counteracting force which partly reverses EM and TM. We also introduce *stress evolution* in interconnects in our final subsection II-D because of the importance of EM-induced hydrostatic stress as a key parameter in today's migration robustness assessment.

A. Electromigration (EM)

EM describes the flow of metal ions in an interconnect where an electrical field is present and current is flowing. The force that acts on the atoms and causes the migration is explained by the momentum transfer of electrons to atomic cores. The resulting atomic motion leads to tensile stress at the cathode and compressive stress at the anode of a wire, as depicted in Fig. 3. This stress gradient causes SM which partly reverses the EM-induced differences in atom concentration.

The atomic flow $\vec{J}_{\mathrm{EM}}$ caused by EM can be described by

$$\vec{J}_{\mathrm{EM}} = \frac{c}{k_{\mathrm{B}}T} \cdot D_0 \cdot \exp\left(-\frac{E_{\mathrm{a}}}{k_{\mathrm{B}}T}\right) \cdot Ze\rho\vec{j} \qquad (1)$$

where c is the metal concentration, k_{B} Boltzmann's constant, T the temperature, D_0 the diffusion constant, E_{a} the activation energy, Z the effective charge of copper, e the elementary charge, ρ the specific electrical resistance, and j the current density [1].

EM in electrical interconnects greatly impacts their time to failure and, thus, their reliability. Specifically, tensile stress at the cathode of a metal line can cause voids. In rare cases, compressive stress at the anode leads to the formation of hillocks [12]. Both voids (that can result in opens) and hillocks (which can form shorts to other wires) are critical in terms of IC reliability (Fig. 4).

B. Thermal Migration (TM)

TM is caused by temperature gradients in wires. Atoms move from hotter to colder regions of the interconnect. This results in tensile stress at hot, and compressive stress at cold, locations in a wire (Fig. 5). Temperature gradients can arise

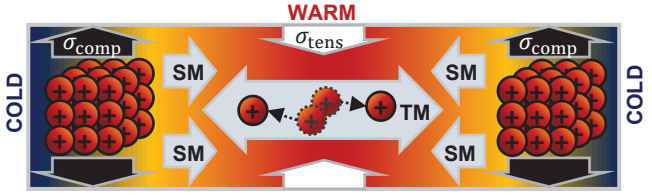

Fig. 5. Atomic motion due to TM leads to tensile stress in hot, and compressive stress in cold, regions of an interconnect. The resulting stress gradient causes SM which, in part, reverses the effects of TM.

(1) from Joule heating caused by high current density and (2) from external heat sources such as active devices with high power dissipation.

The atomic flow $\vec{J}_{\mathrm{TM}}$ caused by TM can be represented as

$$\vec{J}_{\mathrm{TM}} = -\frac{cQ}{k_{\mathrm{B}}T^2} \cdot D_0 \cdot \exp\left(-\frac{E_{\mathrm{a}}}{k_{\mathrm{B}}T}\right) \cdot \mathrm{grad}\ T \qquad (2)$$

where Q is the specific heat of transport [1].

C. Stress Migration (SM)

SM is driven by stress gradients within interconnects. Atoms leave regions that are exposed to compressive stress and move toward regions under tensile stress. The atomic flow $\vec{J}_{\mathrm{SM}}$ caused by SM can be calculated as

$$\vec{J}_{\mathrm{SM}} = \frac{c\Omega}{k_{\mathrm{B}}T} \cdot D_0 \cdot \exp\left(-\frac{E_{\mathrm{a}}}{k_{\mathrm{B}}T}\right) \cdot \mathrm{grad}\ \sigma \qquad (3)$$

where Ω is the atom volume and σ is the hydrostatic stress [1].

Stress gradients can result from initial residual stress that originates in the fabrication process, thermal expansion and thermal mismatch, and other migration processes (EM and TM). In the latter case, SM will partly reverse the atom dislocation caused by EM and TM and, thus, limit wire degradation. However, today's low-k dielectrics are "softer" than the dielectrics used in older technologies, which diminishes this compensating effect of SM [13].

D. Stress Evolution Within Interconnects

The total atomic flux $\vec{J}$ within a wire can be described as

$$\vec{J} = \vec{J}_{\mathrm{EM}} + \vec{J}_{\mathrm{SM}} + \vec{J}_{\mathrm{TM}} \qquad (4)$$

and leads to a hydrostatic stress profile that is built up along the interconnect. This process is called *stress evolution*. It

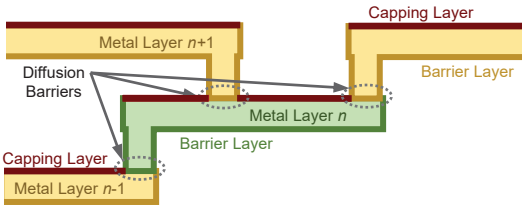

Fig. 6. Stress evolution can be calculated for metal structures that are bordered by diffusion barriers, such as the segment depicted in green in this example. Note that diffusion barriers are located below the vias in dual-damascene copper technologies.

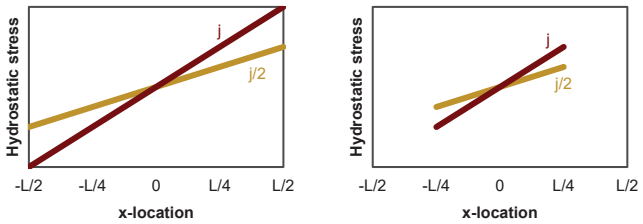

Fig. 7. The Blech product describes the influence of current density j and wire length L on EM robustness, which is represented by the maximum occurring stress. Reducing either j or L will moderate the EM risk.

is important because the stress arising in an interconnect is considered the critical parameter for migration robustness in modern migration models.

The stress evolution in a straight interconnect line caused by EM and SM can be modelled by the Korhonen equation [14]. Expanding the equation by the effect of TM [15] results in:

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}\left[\frac{DB\Omega}{k_\mathrm{B}T}\left(\frac{\partial \sigma}{\partial x} - \frac{e\rho Z j}{\Omega} - \frac{Q}{\Omega T}\frac{\partial T}{\partial x}\right)\right] \tag{5}$$

where B is the effective bulk modulus and D is the diffusion coefficient with $D = D_0 \cdot \exp\left(-E_\mathrm{a}/(k_\mathrm{B}T)\right)$. If both current density and temperature distribution are constant over time, the stress profile will reach a steady state, where the total atomic flux (4) becomes zero.

Stress evolution is always calculated for wire segments that are bordered by diffusion barriers [16]. In modern dual-damascene technologies, those barriers are located on top of each metal layer (i. e., below the vias). Consequently, a wire segment (sometimes referred to as an *interconnect tree*) consists of a metal structure within one routing layer and the vias connecting to the routing layer below (depicted in green in Fig. 6).

III. EM Consideration in State-Of-The-Art Design Flows

A. EM Verification Techniques

EM checking is a well-established verification step in today's IC design flows. It is usually performed after layout synthesis and is based on current densities occurring in the wires. This current density-based approach has its origins in the traditional EM models by Black [17] and Blech [18]. Black's model is an empirical estimation of a wire's lifetime considering temperature and current density. However, its results are proven to lack precision. Blech's model is derived from the atomic flux equations (1) and (3) for EM and SM, respectively. It defines a critical product $(jL)_\mathrm{Blech}$ of current density and wire length (the so-called *Blech product*), which is considered a boundary value for "immortal" wires (Fig. 7). Blech's model only applies to straight interconnect lines that can be approximated by the one-dimensional case.

Both models fail to accurately determine the EM risk of real interconnect structures because of the above limitations. Consequently, they lead to pessimistic EM constraints and large safety margins. Multiple novel approaches relying on the calculation of hydrostatic stress distribution have been developed to overcome this issue. For example, the transient stress evolution for any interconnect structure can be simulated by FEM analysis. FEM is very accurate and can include multiple physical domains [19], [20]. Layout-driven discretization enables relatively fast EM checks for huge layout designs [21]. Still, FEM requires excessive simulation time and, thus, is not applicable for full-chip analysis. Recently published methods to estimate the steady-state stress distribution include voltage-based EM analysis (VBEM method) [5], [22]; the transformation of the interconnect trees into equivalent RC-networks [6]; and machine learning-based approaches [23], [24]. PDNs can be verified with them at acceptable speeds and to a reasonable degree of accuracy.

B. Handling EM Violations

If EM violations are detected, a repair step is initiated. The most common repair strategy is widening the wire segments that are at risk of suffering EM-induced failure. The current density is thereby decreased. A larger wire width can be achieved without sacrificing routing resources by shifting the interconnect to a higher metal layer where structure sizes are bigger. Another well-known technique is the use of redundant vias. The EM susceptibility of a wire segment can also be limited by short wire lengths. Hence, a metal layer change is very efficient in terms of EM robustness as it will introduce a diffusion barrier into the current path, thereby shortening the wire segment(s).

More advanced EM mitigation techniques include the use of cathode reservoirs and via-below (also referred to as "upstream") configurations. Cathode reservoirs are passive metal structures that reduce the danger of void nucleation by limiting the tensile stress. However, they increase the compressive stress.

The via configuration influences the EM susceptibility of a wire as voids usually nucleate below the capping layer. Via-below configurations cause void nucleation at the top of the metal line. The void can become much bigger here before causing a critical rise in line resistance. In contrast, via-above (also referred to as "downstream") configurations are susceptible to voids that are located directly below the via. Those voids are critical even when they are small (Fig. 8).

For a detailed description of those EM countermeasures as well as their efficiencies, please refer to [1], [10], [25].

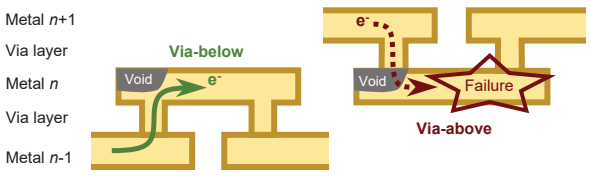

Fig. 8. Via-below vs. via-above configuration with their void locations.

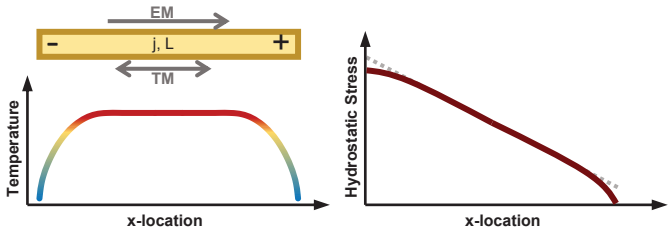

Fig. 9. A straight interconnect line and its relation between current density j and length L. Note the typical temperature profile caused by Joule heating (left) and the stress profile resulting from EM, TM, and SM (red) compared to the stress profile without TM consideration (grey, right).

IV. Consideration of Thermal Effects

As described in Sec. II, the effect of TM on interconnect reliability has widely been neglected up to now. Moreover, temperature differences across the chip have only partly been considered for EM and SM simulation. In order to meaningfully assess the migration robustness of metal interconnects both aspects are highly relevant, however.

A. Temperature Influence on EM and SM

Both the transient stress evolution and the steady-state stress profile are highly dependent on the interconnect temperature. Higher temperature leads to faster wire degradation and higher stress values [14]. EM analysis is typically performed for a constant chip temperature. A first step for more precise results would be to use the thermal characteristics of the chip and assign an approximate individual temperature to each net.

In a more advanced approach, the authors of [26] consider the temperature rise due to Joule heating and assess its influence on EM and SM. Both the simulations and the experimental validation show that Joule heating has a significant impact on the migration-induced degradation of metal lines. In [27], EM and SM are modelled under time-varying temperature. This study is limited to three-terminal interconnects due to the complexity of the problem. Nevertheless, it concludes that temperature changes over time (e. g., resulting from different operation modes) cannot be neglected as they have an impact on the stress evolution and, thus, the time to failure.

Even though there are methods to consider different temperatures for migration analysis, a key challenge remains to obtain accurate chip thermal characteristics. The temperature in an interconnect is highly dependent on its surroundings and its current load. For example, transistor power dissipation can be the source of external interconnect heating; vias can improve heat transmission to other metal layers; and the choice of chip package will determine the external heat dissipation efficiency. Obviously, multiple studies have been carried out and multiple tools exist for the thermal simulation of chips. Notably, the authors of [28] provide a method for obtaining the temperature distribution within the metal stack and additionally review the effect of the results on EM.

B. Considering TM in IC Design

The growing influence of TM, driven by thermal gradients, further exacerbates verification complexity. Temperature gradients within interconnects can arise from Joule heating (also referred to as self-heating) and from external heat sources, such as transistors. Most academic publications focus on Joule heating. The power of heat that is produced within an interconnect is proportional to j^2.

Current density j is increasing with shrinking feature sizes and recent studies [9] have shown that for small technology nodes the atomic flux caused by TM is of the same order of magnitude as the atomic flux driven by EM. Thus, TM needs to be considered by the verification tools. The authors of [29] derive equations to calculate the mean time to failure of wires for EM, TM and SM, respectively. A first combined approach to consider EM and TM in the verification of multi-segment interconnects is presented in [15]. The authors show that TM indeed has significant impact on the EM failure process.

On the other hand, TM consideration leads to a serious increase in problem complexity. This makes both modelling and simulation of the migration process very challenging. Additionally, for TM consideration, the temperature profile along the wire must be known as TM is very sensitive to temperature gradients. Thus, inaccuracies in the temperature profile (e. g., due to linearization) have significant impact on the stress result. The temperature model introduced in [30] is commonly used and has been adapted to multi-segment interconnects. The problem with this model is that it relies on interconnect terminals that have a known constant temperature and on homogeneous wire surroundings. This is too simplistic for real-world conditions.

However, TM could also relax EM constraints as the hottest regions are often located in the middle of a wire [9], [31]. Consequently, TM forces atoms to move toward anode and cathode. This increases the compressive stress at the anode but reduces the tensile stress at the cathode (Fig. 9) and thereby the risk of voiding. Increased compressive stress is less critical as voids are the most common migration-induced failure mechanism. Exploiting this effect in layout designs could help in meeting migration robustness constraints.

V. Toward Migration-Robust Layout Synthesis

A. Problem Formulation

Migration robustness can be addressed at various stages in IC design and fabrication. For instance, [4] outlines technological changes within the metal stack. New materials that are less susceptible to EM could replace copper in the first metal layers. In circuit design, currents can be minimized in order

to reduce current density and, thus, the EM risk and Joule heating.

In physical design (which is the focus of this paper), migration robustness can be improved at early stages, like placement [32]. However, most approaches are included in the routing procedure. The design measures mentioned in Sec. III-B promote EM robustness while minimizing the use of additional routing resources. Nevertheless, they are only partly included in up-to-date IC routing engines. Thus, their true potential is not really exploited – even though novel design strategies and EM inhibiting measures are urgently needed.

It is not only DC lines that are affected by EM in nanometric technologies, but clock and signal nets as well. The effect on these nets needs to be considered in layout design [33], [34]. Furthermore, TM is becoming more critical [9]. Consequently, the number of interconnects that must be verified for their migration robustness is rising and there is extra repair effort needed for a robust layout result [11].

Considerable design time is needed to assure migration robustness in ICs in leading-edge technologies. This challenge will grow with every new technology node. It is worth noting that scaling the structure sizes in the metal stack is inhibited today due to migration avoidance [4].

B. Existing Approaches for Proactive Routing

In order to face the challenges outlined in Sec. V-A, novel migration-robust routing strategies are required. The basic idea is to take migration-robustness constraints into account *proactively* and create a routing solution that is migration robust "by design". In other words, these approaches bound the design space to migration-robust routing topologies. It will be easier – and it may not even be necessary – to verify the layout for migration-robustness violations at a later stage. In any case, the number of violations will be cut sharply – reducing the required repair effort.

There are a few recently published design flows for (proactive) EM-robust PDN synthesis. These include machine learning-based approaches [35], [36] that incorporate EM-robustness constraints in the training step. Thus, the trained neural network will automatically generate EM-robust power grids. This reduces the simulation and optimization effort needed to obtain the final PDN design as the initial solution provided by the neural network is already optimized.

A proactive design flow for EM-robust signal lines is proposed in [10], [37]. Here, EM-driven net ordering is first performed by estimating the EM risk of each net based on the global routing results, as depicted in Fig. 10. This ensures that nets, which are especially susceptible to migration-induced degradation, will be routed first. After that, detailed routing and EM analysis are performed for each remaining net. If the stress within the currently considered net is high compared to the nets routed before, EM countermeasures (cf. Sec. III-B) are implemented to achieve improved EM robustness. Obviously, this is a promising strategy for layouts where only a small portion of the signal lines is affected by EM.

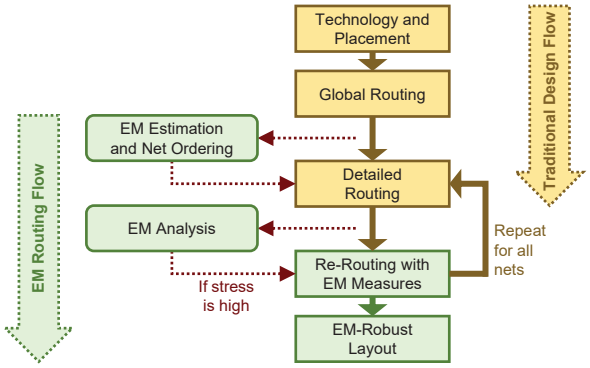

Fig. 10. The major steps of the proactive design approach proposed in [10].

In cases, where the migration susceptibility of signal lines is higher and, subsequently, more violations are expected, a routing approach based on constraints that consider migration robustness should be more favorable: As an example, we propose pre-simulating routing segments (i. e., interconnect structures that are bordered by diffusion barriers, see Sec. II-D) in order to derive general constraints that ensure migration robustness and that can be included in a design rule set for the routing engine. As the simulation of these routing segments is not part of the actual design process, it can be performed extensively. This will produce detailed and accurate results, which can include multiple factors (like temperature) that have a significant impact on migration robustness.

VI. Summary and Outlook

Atomic migration within metal interconnects threatens the reliability of integrated circuits. This problem is becoming more severe in every new technology node and limits the scaling of structures in the metal stack.

In this paper, we reviewed the fundamentals of the most important driving forces for hydrostatic stress evolution: Electromigration, thermal migration, and stress migration. We summarized strategies to avoid EM at the physical design stage and novel approaches to asses interconnects for their migration robustness. Recent studies show that migration robustness is significantly impacted by thermal effects, which need to be taken into account in future design and verification tools: they cannot be neglected anymore.

We suggest considering migration constraints in a pre-layout step in future design strategies in order to produce reliable ICs in leading-edge technology nodes. This will be a paradigm shift from the current *repair* strategy toward a *proactive* layout synthesis that will accomplish migration robustness "by design". This proactive design methodology should be integrated in design flows in future work by capturing migration robustness into constraints and applying them in the various layout synthesis steps. Migration robustness is thus ensured at a minimum of additional design and verification effort – and without sacrificing routing resources, power, or performance.

References

[1] J. Lienig and M. Thiele, *Fundamentals of Electromigration-Aware Integrated Circuit Design*. Cham: Springer, 2018, https://link.springer.com/book/10.1007/978-3-319-73558-0.

[2] ——, "The pressing need for electromigration-aware physical design," in *Proceedings of the 2018 International Symposium on Physical Design*, 2018, pp. 144–151, https://doi.org/10.1145/3177540.3177560.

[3] ITRS, International Technology Roadmap for Semiconductors 2.0 (ITRS 2.0). http://www.itrs2.net/itrs-reports.html, 2015.

[4] IRDS, IEEE International Roadmap for Devices and Systems (More Moore) https://irds.ieee.org/editions/2021/more-moore, 2021.

[5] S. X.-D. Tan, M. Tahoori, T. Kim *et al.*, *Long-Term Reliability of Nanometer VLSI Systems*. Cham: Springer, 2019, https://doi.org/10.1007/978-3-030-26172-6.

[6] F. N. Najm, "Equivalent circuits for electromigration," *Microelectronics Reliability*, vol. 123, p. 114200, 2021, https://doi.org/10.1016/j.microrel.2021.114200.

[7] S. Torosyan, A. Kteyan, V. Sukharev *et al.*, "Novel physics-based tool-prototype for electromigration assessment in commercial-grade power delivery networks," *Journal of Vacuum Science & Technology B*, vol. 39, no. 1, p. 013203, 2021, https://doi.org/10.1116/6.0000617.

[8] Z. Guan and M. Marek-Sadowska, "Atomic flux divergence-based ac electromigration model for signal line reliability assessment," in *2015 IEEE 65th Electronic Components and Technology Conference (ECTC)*, 2015, pp. 2155–2161, https://doi.org/10.1109/ECTC.2015.7159901.

[9] A. Abbasinasab and M. Marek-Sadowska, "Rain: A tool for reliability assessment of interconnect networks—physics to software," in *2018 55th ACM/ESDA/IEEE Design Automation Conference (DAC)*, 2018, pp. 1–6, https://doi.org/10.1109/DAC.2018.8465800.

[10] S. Bigalke and J. Lienig, "Avoidance vs. repair: New approaches to increasing electromigration robustness in vlsi routing," *Integration*, vol. 75, pp. 189 – 198, 2020, https://doi.org/10.1016/j.vlsi.2020.04.009.

[11] S. Bigalke, J. Lienig, G. Jerke *et al.*, "The need and opportunities of electromigration-aware integrated circuit design," in *2018 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2018, pp. 1–8, https://doi.org/10.1145/3240765.3265971.

[12] F. L. Wei, C. L. Gan, T. L. Tan *et al.*, "Electromigration-induced extrusion failures in cu/low-k interconnects," *Journal of Applied Physics*, vol. 104, no. 2, p. 023529, 2008, https://doi.org/10.1063/1.2957057.

[13] D. Shamiryan, T. Abell, F. Iacopi *et al.*, "Low-k dielectric materials," *Materials Today*, vol. 7, no. 1, pp. 34–39, 2004, https://doi.org/10.1016/S1369-7021(04)00053-7.

[14] M. A. Korhonen, P. Børgesen, K. N. Tu *et al.*, "Stress evolution due to electromigration in confined metal lines," *Journal of Applied Physics*, vol. 73, no. 8, pp. 3790–3799, 1993, https://doi.org/10.1063/1.354073.

[15] L. Chen, S. X.-D. Tan, Z. Sun *et al.*, "A fast semi-analytic approach for combined electromigration and thermomigration analysis for general multi-segment interconnects," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, pp. 1–1, 2020, https://doi.org/10.1109/TCAD.2020.2994271.

[16] S. Chatterjee, V. Sukharev, and F. N. Najm, "Power grid electromigration checking using physics-based models," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 37, no. 7, pp. 1317–1330, 2018, https://doi.org/10.1109/TCAD.2017.2666723.

[17] J. R. Black, "Electromigration—a brief survey and some recent results," *IEEE Transactions on Electron Devices*, vol. 16, no. 4, pp. 338–347, 1969, https://doi.org/10.1109/T-ED.1969.16754.

[18] I. A. Blech, "Electromigration in thin aluminum films on titanium nitride," *Journal of Applied Physics*, vol. 47, no. 4, pp. 1203–1208, 1976, https://doi.org/10.1063/1.322842.

[19] M. Thiele, S. Bigalke, and J. Lienig, "Exploring the use of the finite element method for electromigration analysis in future physical design," in *2017 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, 2017, pp. 1–6, https://doi.org/10.1109/VLSI-SoC.2017.8203466.

[20] ——, "Electromigration analysis of vlsi circuits using the finite element method," in *VLSI-SoC: Opportunities and Challenges Beyond the Internet of Things*. Cham: Springer, 2019, pp. 133–152, https://link.springer.com/book/10.1007/978-3-030-15663-3.

[21] S. Bigalke, J. Lienig, T. Casper *et al.*, "Increasing em robustness of placement and routing solutions based on layout-driven discretization," in *2018 14th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, 2018, pp. 89–92, https://doi.org/10.1109/PRIME.2018.8430323.

[22] Z. Sun, E. Demircan, M. D. Shroff *et al.*, "Voltage-based electromigration immortality check for general multi-branch interconnects," in *2016 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2016, pp. 1–7, https://doi.org/10.1145/2966986.2967083.

[23] W. Jin, S. Sadiqbatcha, Z. Sun *et al.*, "Em-gan: Data-driven fast stress analysis for multi-segment interconnects," in *2020 IEEE 38th International Conference on Computer Design (ICCD)*, 2020, pp. 296–303, https://doi.org/10.1109/ICCD50377.2020.00057.

[24] W. Jin, L. Chen, S. Sadiqbatcha *et al.*, "Emgraph: Fast learning-based electromigration analysis for multi-segment interconnect using graph convolution networks," in *2021 58th ACM/IEEE Design Automation Conference (DAC)*, 2021, pp. 919–924, https://doi.org/10.1109/DAC18074.2021.9586239.

[25] J. Lienig, S. Rothe, M. Thiele *et al.*, "Toward security closure in the face of reliability effects iccad special session paper," in *2021 IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, 2021, pp. 1–9, https://doi.org/10.1109/ICCAD51958.2021.9643447.

[26] K. Lee, J. Kim, T. Jeong *et al.*, "Effect of joule heating on electromigration in dual-damascene copper low-k interconnects," in *2017 IEEE International Reliability Physics Symposium (IRPS)*, 2017, pp. 6B–6.1–6B–6.5, https://doi.org/10.1109/IRPS.2017.7936344.

[27] H. Chen, S. X.-D. Tan, J. Peng *et al.*, "Analytical modeling of electromigration failure for vlsi interconnect tree considering temperature and segment length effects," *IEEE Transactions on Device and Materials Reliability*, vol. 17, no. 4, pp. 653–666, 2017, https://doi.org/10.1109/TDMR.2017.2746660.

[28] W. Ahn, H. Zhang, T. Shen *et al.*, "A predictive model for ic self-heating based on effective medium and image charge theories and its implications for interconnect and transistor reliability," *IEEE Transactions on Electron Devices*, vol. 64, no. 9, pp. 3555–3562, 2017, https://doi.org/10.1109/TED.2017.2725742.

[29] K. N. Tu and A. N. Gusak, "Mean-time-to-failure equations for electromigration, thermomigration, and stress migration," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 10, no. 9, pp. 1427–1431, 2020, https://doi.org/10.1109/TCPMT.2020.3003003.

[30] T.-Y. Chiang, K. Banerjee, and K. C. Saraswat, "Compact modeling and spice-based simulation for electrothermal analysis of multilevel ulsi interconnects," in *IEEE/ACM International Conference on Computer Aided Design. ICCAD 2001. IEEE/ACM Digest of Technical Papers*, 2001, pp. 165–172, https://doi.org/10.1109/ICCAD.2001.968613.

[31] A. K. Singh and J. Kumar, "Electrical characteristics, stability, electromigration, joule heating, and reliability aspect of focused ion beam fabricated gold and copper nanobar interconnects on sio_2 and glass substrates," *Journal of Vacuum Science & Technology B*, vol. 38, no. 6, p. 062805, 2020, https://doi.org/10.1116/6.0000514.

[32] W. Ye, Y. Lin, X. Xu *et al.*, "Placement mitigation techniques for power grid electromigration," in *2017 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, 2017, pp. 1–6, https://doi.org/10.1109/ISLPED.2017.8009178.

[33] G. Posser, S. S. Sapatnekar, and R. Reis, *Electromigration Inside Logic Cells*. Springer, 2017, https://link.springer.com/book/10.1007/978-3-319-48899-8.

[34] L. de Paris, G. Posser, and R. Reis, "Electromigration aware circuits by using special signal non-default routing rules," in *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2016, pp. 2795–2798, https://doi.org/10.1109/ISCAS.2016.7539173.

[35] S. Dey, S. Nandi, and G. Trivedi, "Powerplanningdl: Reliability-aware framework for on-chip power grid design using deep learning," in *2020 Design, Automation Test in Europe Conference Exhibition (DATE)*, 2020, pp. 1520–1525, https://doi.org/10.23919/DATE48585.2020.9116536.

[36] V. A. Chhabria, A. B. Kahng, M. Kim *et al.*, "Template-based pdn synthesis in floorplan and placement using classifier and cnn techniques," in *2020 25th Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2020, pp. 44–49, https://doi.org/10.1109/ASP-DAC47756.2020.9045303.

[37] S. Bigalke and J. Lienig, "Flute-em: Electromigration-optimized net topology considering currents and mechanical stress," in *2018 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, 2018, pp. 225–230, https://doi.org/10.1109/VLSI-SoC.2018.8644965.

Please cite as: S. Rothe, J. Lienig: "Reliability by Design: Avoiding Migration-Induced Failure in IC Interconnects," Proc. Symposium on Integrated Circuits and Systems Design (SBCCI), August 2022, Porto Alegre, Brazil