

# Interface Optimization for Improved Routability in Chip-Package-Board Co-Design

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**Abstract**—The simultaneous optimization of both pin assignment and pin routing for different hierarchy levels (chip, package, board) of an electronic system is a bottleneck in today’s hierarchical co-design flows, typically requiring manual optimization strategies and multiple iterations. Specifically, a fast and fine-grained evaluation of routability that considers all requirements between the different hierarchy levels is missing. In this paper we provide a comprehensive, fast method to evaluate the routability of interfaces in hierarchical systems based on a new probabilistic routability prediction. We implemented our methodology in an industrial design flow and achieved significant improvement in overall routing, including reduced manufacturing costs of chip-package-board co-designs.

## I. INTRODUCTION

An important step in the co-design of integrated circuits (ICs) and printed circuit boards (PCBs) is the definition of the interfaces between different hierarchy levels (chip, package, board). One seeks to assign signals (nets) to pin locations (*pin assignment*) on both the component ICs and the PCB such that the subsequent *pin routing* of the overall system design optimizes system performance, and is achieved in reasonable time (Fig. 1).

In many practical examples, however, the interface configuration of devices is dictated by the internal physical structure of the component. While this simplifies the internal routing task, it does so at the expense of more complex routing between the external pins of the various hierarchical levels. On the other hand, optimizing the interface based only on the (external) pin routing task may result in an internal routing problem that is difficult to solve.

Connecting pins among different hierarchy levels has become an increasingly difficult task as a result of the preference given to internal IC routing. Recently, routing algorithms tackling the problem of pin routing [1]–[5] have been published. However, they do not address what we consider to be the main factor contributing to the difficulty: the gap that exists between levels of a design that is developed hierarchically. Specifically, the internal IC design (i.e., chip routing and “internal” pin assignment) is not synchronized with the task of connecting external pins at the system-design level. As we demonstrate, bridging this gap not only eases the design flow, it also improves the overall system performance.

It is clear that optimization of the overall routability across different hierarchy levels demands an integrated pin assignment step that is synchronized with the design of the internal

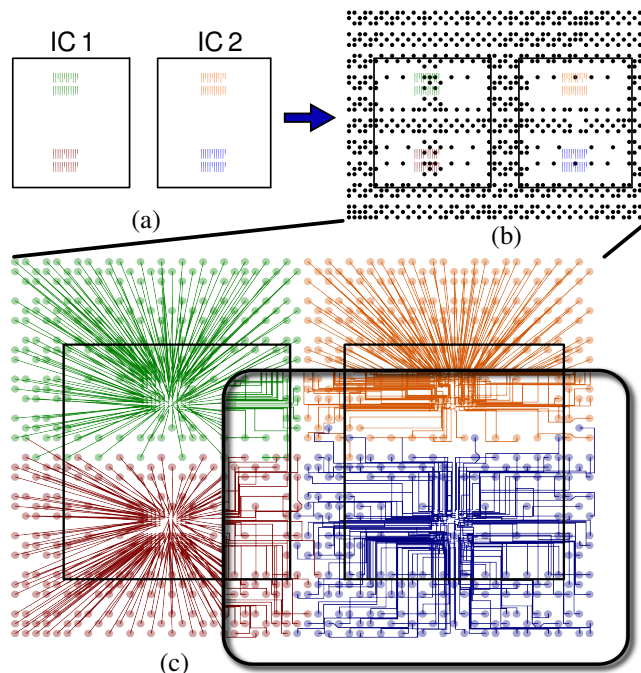


Fig. 1. The pin assignment and routing problem of a simple chip-package co-design. External pins of two ICs (a) with superimposed signal pins of the chip carrier (b), the optimized pin assignment illustrated by flylines (c), and the final pin routing (inset).

chip and the PCB. This requires early, concurrent optimization of pin assignment at all hierarchy levels to enable the best routability. Such optimization must be fast, must work on an abstraction level that is available early in the design flow, and must provide fine-grained, detailed information about the quality/routability/congestion.

The contributions of this paper are:

- a new methodology based on probabilistic congestion prediction that determines the routability of a design similar to global routing, yet with significantly shorter computation times,
- a time-efficient approach to evaluate and, hence, improve the pin assignment and pin routing of interfaces in hierarchical designs on all hierarchy levels, thereby,
- enabling concurrent optimization of the I/O interfaces of all system levels (chip, package, and board) for the first time.

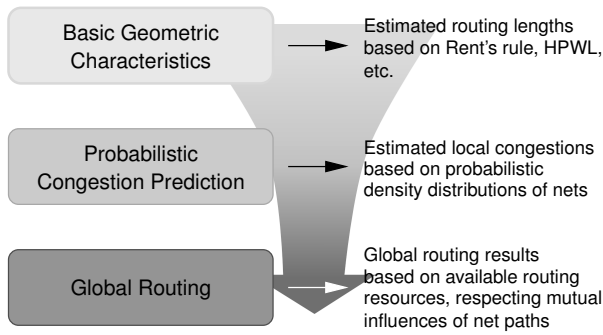


Fig. 2. Classification of routability prediction methods sorted by their granularity from coarse (top) to detailed (bottom).

## II. RELATED WORK

### A. Pin Assignment Optimization

Pin assignment is an essential part of interface optimization between different hierarchy levels. The pin assignment problem is to assign all nets (signals) to unique, valid pin locations so that the overall design is optimized. In most cases, pin assignment optimization aims to maximize routability. So far, pin assignment algorithms have evaluated routability based on either basic geometric characteristics [6], [7] (such as net lengths, signal skew and the count of flyline intersections) or principles of global and detailed routing [1]–[5], [8] (e.g., min-cost max-flow optimization).

### B. Methods of Routability Prediction

Routability prediction methods differ in granularity, accuracy, sophistication, required input data, and computational effort. A basic classification of routability prediction methods (as relevant to pin assignment) is depicted in Fig. 2.

As will be shown in Sec. V-B, routability prediction based on probabilistic congestion prediction provides pin assignment optimization with an improved accuracy compared to routability prediction based on basic geometric characteristics (such as net lengths, signal skew or flyline intersections). Obviously, prediction methods based on global routing provide even better accuracy. However, they are impractical for optimizing pin assignment due to two reasons. First, their higher computational effort is significant, since many different pin assignment configurations have to be evaluated during the optimization of one design. Second, global routing requires known detailed routing resources – an input not yet available during pin assignment. Consequently, probabilistic congestion prediction is best suited for early interface optimization.

### C. Probabilistic Congestion Prediction

As discussed above, probabilistic methods of congestion prediction estimate routability at an intermediate accuracy, i.e., between the accuracy of basic geometric characteristics and that of global routing (Fig. 2). They provide detailed, local routability measures similar to global routing with shorter computation times. This faster computation is achieved because possible routing conflicts are not resolved in detail. Yet,

probabilistic congestion prediction has not been used for pin assignment optimization so far.

Evaluation and optimization of the routability of pin assignment requires adapted probabilistic congestion prediction (see below), using methods originally developed to guide strategic decisions of global routing algorithms. These probabilistic prediction schemes include methods for routing paths with an unlimited number of bends [9], [10] and methods for routers using up to two, four, or five bends per routing path [11]–[14]. Finally, a combination and extension of the approaches in [15] and [16] was recently presented in [17]. It differs from all of the afore mentioned works by not assuming probabilities for specific possible routing paths. Instead, local routing density distributions are deduced from distances between pins.

## III. PROBABILISTIC CONGESTION PREDICTION

Pin assignment optimization regarding routability strictly depends on the availability of a quantitative measure of routability. This measure can only be calculated most accurately if the time-consuming process of detailed routing was actually completed before. However, the effort required for routing is prohibitive for effective pin assignment optimization processes. Therefore, pin assignment at an early stage of physical design, like during interface definition and optimization, should be based on estimates that can be determined quickly and are known to resemble routability of the design appropriately. These estimates typically are: predicted routing lengths, signal skew, and signal intersections. In practice, however, these measures are not precise enough for an effective routability optimization. For example, several different pin assignments for the same design might have identical estimated Manhattan routing lengths and, consequently, cannot be distinguished by this method.

Pin assignment optimization based on global routing avoids this problem. However, global routing is slower and requires knowledge of locally available routing resources. Unfortunately, these resources depend on technological decisions which, in practice, are often still pending, during early interface optimization. Moreover, it is desirable to optimize pin assignment with regard to routability first and only subsequently evaluate the required routing resources. This allows technological requirements to be derived from the optimization results.

As global routing does not provide this option, we adapt *probabilistic congestion prediction* to evaluate and optimize pin assignments with regard to routability.

### A. Routing Density Distribution

A probabilistic congestion prediction is based on a statistic density distribution  $u_n(x, y)$  for a single net  $n$ , which depends on the routing width and pitch of the net and reflects the statistic average of the final routing geometry for the net. Typically, values for such distributions equal zero outside of the smallest rectangle enclosing all pins of the net. Multiple density distributions are used in practical applications [9]–[17] because different routing strategies are resembled best by

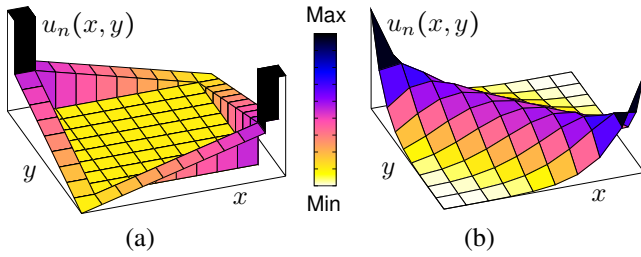


Fig. 3. Probabilistic routing density distribution for a two-pin net resembling (a) Z-shape routing geometry (two bends per routing path) and (b) routing with an unlimited number of bends [10]. Pins are located in the upper-left and lower-right corner.

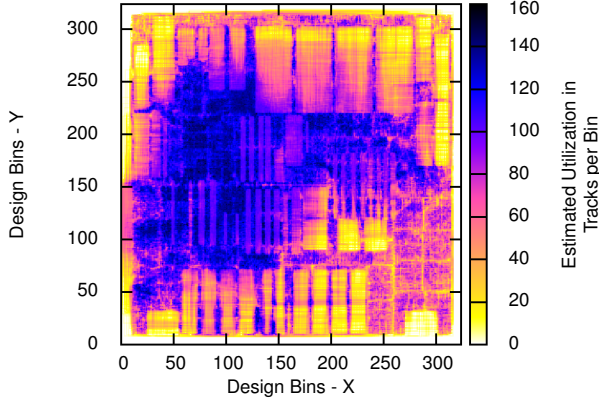


Fig. 4. Overall estimated utilization  $\mathcal{U}_{\text{chip}}(x, y)$  for chip *adaptec1* of the ISPD global routing benchmark suite [18].

different density distributions. Fig. 3 illustrates two example distributions.

The overall estimated utilization  $\mathcal{U}_l(x, y)$  for hierarchy level  $l$  is determined by superimposing the density distributions of all individual nets (Fig. 4).

$$\mathcal{U}_l(x, y) = \sum_{n \in N_l} u_n(x, y), \quad (1)$$

with  $N_l$  denoting the set of all nets in hierarchy level  $l$ .

### B. A New Approach to Over-Congestion

When used to guide global routing, the overall utilization estimation  $\mathcal{U}_l(x, y)$  is typically “smoothed” based on the locally available routing resources. During this post-processing step, utilization is shifted away from regions exceeding the available routing resources (*over-congested*) into adjacent regions with free capacities. This resembles constrained routing resources that force routers to detour nets around over-congested regions. As illustrated in Fig. 5, such a post-processing step erases local congestion information and prevents detailed analysis within over-congested and adjacent regions. For that reason and because routing resource constraints are not known during pin assignment (as discussed above), such a post-processing step is impractical for pin assignment optimization.

Instead, we introduce the *critical net length*  $C(n)$  of a net  $n$  as a new metric to interpret probabilistic prediction in over-congested regions. It allows an improved evaluation within

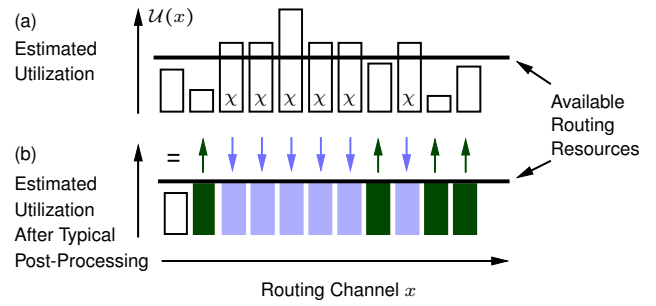


Fig. 5. Local features of the overall utilization prediction (a) are erased to imitate the behavior of global routers in over-congested regions  $\chi$ . Utilization is shifted away from over-congested regions into adjacent regions (b).

congested regions during pin assignment optimization since local utilization does not have to be shifted by any post-processing step.  $C(n)$  is calculated by

$$C(n) = \sum_{(x, y) \in \mathcal{A}_l} [\mathcal{U}_l(x, y) - u_n(x, y)] \cdot u_n(x, y), \quad (2)$$

with  $l$  denoting the hierarchy level of net  $n$  and  $\mathcal{A}_l$  denoting the region of that hierarchy level. According to Eq. 2, the critical net length  $C(n)$  of net  $n$  is the sum of products of estimated utilization for  $n$  and overall estimated utilization over all bins (Fig. 6). Consequently,  $C(n)$  results in higher values if more probable routing paths of net  $n$  traverse highly utilized regions and thus, provides a detailed measure of routability for net  $n$ .

We chose to refer to  $C(n)$  as *critical net length* because the factor  $\sum_{(x, y) \in \mathcal{A}_l} u_n(x, y)$  of Eq. 2 is proportional to net  $n$ 's Manhattan length.

### C. Adapted Probabilistic Prediction Model

In order to improve the accuracy of probabilistic prediction, we developed a probabilistic net model which includes modeling of detoured routing and thus renders a smoothing post-processing step redundant. In contrast to any previous work, such as [17], we model detours depending on the angle of a net. As shown later, this improves the prediction accuracy in all system levels.

Let  $P_{n1}$  and  $P_{n2}$  denote two pins of a net  $n$ . Further let  $(x_{n1}, y_{n1})$  denote the coordinates of pin  $P_{n1}$  and let  $(x_{n2}, y_{n2})$  denote the coordinates of pin  $P_{n2}$ . Subsequently the Manhattan window  $\mathcal{MH}_n$  of net  $n$  is located as illustrated in Fig. 7 and has the horizontal size  $\delta x_n$  and vertical size  $\delta y_n$ , calculated as follows:

$$\delta x_n = |x_{n1} - x_{n2}| \quad (3)$$

$$\delta y_n = |y_{n1} - y_{n2}| \quad (4)$$

We define the *wave front*  $w_n(d)$  to be a line segment within the Manhattan window  $\mathcal{MH}_n$  with each point having the same Manhattan distance  $d$  to pin  $P_{n1}$ . In other words, a wave front  $w_n(d)$  is a diagonal line segment that is Manhattan distance  $d$  away from pin  $P_{n1}$  at any point. We define the length  $l_{wn}(d)$

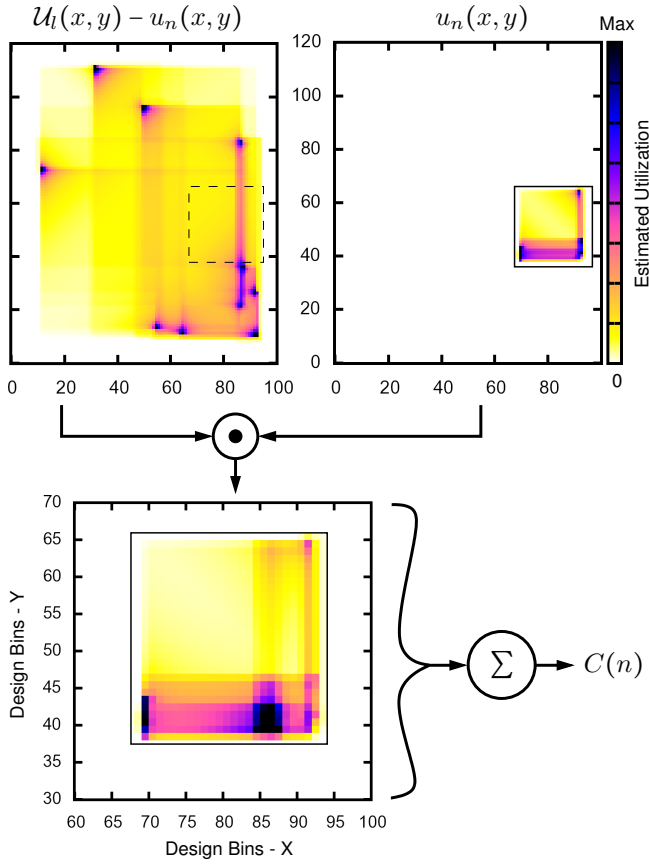


Fig. 6. Illustration of critical net length (see Eq. 2). The overall estimated utilization reduced by estimated utilization of net  $n$  is shown at the top left. The utilization of net  $n$  is shown at the top right. The resulting product of both utilizations is shown at the bottom. The sum of products over all bins is the critical net length  $C(n)$  of net  $n$ .

of a wave front  $w_n(d)$  for  $d \in [0, \delta x_n + \delta y_n]$  as follows:

$$l_{wn}(d) = \begin{cases} d & d \leq \min(\delta x_n, \delta y_n) \\ \delta x_n + \delta y_n - d & d \geq \max(\delta x_n, \delta y_n) \\ \min(\delta x_n, \delta y_n) & \text{else} \end{cases} \quad (5)$$

The estimated utilization  $u_n(i, j)$  of point  $(i, j)$  is calculated as defined in Eq. 6, based on the wave front length  $l_{wn}(i + j)$  with  $t_n$  denoting the routing pitch of net  $n$ . Fig. 8 illustrates the wave front length and the utilization for the example of Fig. 7 along the dotted cut line.

$$u_n(i, j) = \frac{t_n}{t_n + l_{wn}(i + j)} \quad (6)$$

According to Eq. 6, the probability that a routing path will pass through a certain point is evenly distributed along a wave front. Furthermore, the estimated utilization is 50% at a distance of one routing pitch  $t_n$  away from the pins of net  $n$ .

#### D. Adapted Probabilistic Prediction Model Including Detoured Routing Paths

We define a *routing detour region*  $\mathcal{S}_n$  in the proximity of the Manhattan window  $\mathcal{MH}_n$  to include routing detours in the probabilistic prediction of a single net. This region

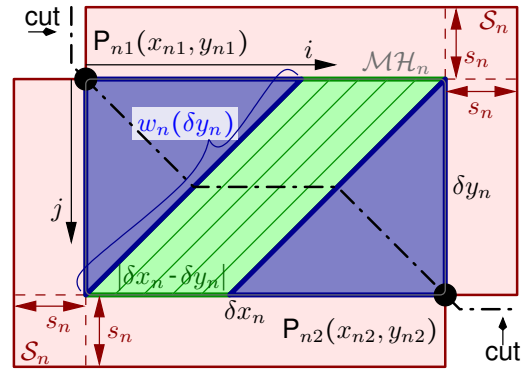


Fig. 7. Illustration of our net model for  $\delta x_n > \delta y_n$ . Refer to Fig. 8 for the plot of the wave front length and the estimated utilization along the dotted cut line.

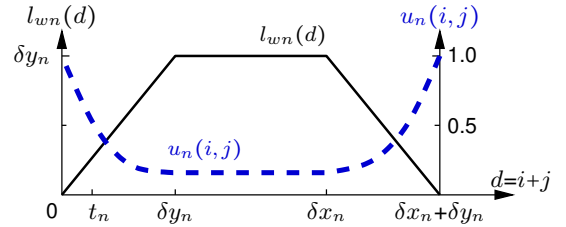


Fig. 8. Wave front length and utilization estimation along dotted cut line of Fig. 7 for  $\delta x_n > \delta y_n$ .

is defined by the distance  $s_n$  spreading orthogonally away from the Manhattan window into all directions except into the “shadow” behind the two pins (as illustrated in Fig. 7).

The width  $s_n$  ( $s_n \geq 0$ ) of the routing detour region  $\mathcal{S}_n$  determines the longest possible routing path  $l_{s_n}$  that is included in the routing prediction. This longest path follows the outer border of  $\mathcal{S}_n$ . We introduce the factor  $\eta_\alpha$  ( $\eta_\alpha \geq 0$ ) to describe the relation between the length of the shortest possible rectilinear routing path ( $\mathcal{HPWL}_n$ ) and the longest routing path included in the prediction.

$$l_{s_n} = 4 \cdot s_n + \delta x_n + \delta y_n \quad (7)$$

$$l_{s_n} = 4 \cdot s_n + \mathcal{HPWL}_n \quad (8)$$

$$l_{s_n} = \eta_\alpha \cdot \mathcal{HPWL}_n \quad (9)$$

Auto routers typically construct routing paths on rectilinear grids. According to experience, on average this gridded approach causes different amounts of routing detour for nets with different angles  $\alpha_n$  relative to the x-coordinate axis.

$$\alpha_n = \begin{cases} \arctan\left(\frac{y_{n2}-y_{n1}}{x_{n2}-x_{n1}}\right) & x_{n2} \geq x_{n1}, y_{n2} \geq y_{n1} \\ \arctan\left(\frac{y_{n2}-y_{n1}}{x_{n2}-x_{n1}}\right) + \pi & x_{n2} < x_{n1} \\ \arctan\left(\frac{y_{n2}-y_{n1}}{x_{n2}-x_{n1}}\right) + \pi & x_{n2} = x_{n1}, y_{n2} < y_{n1} \\ \arctan\left(\frac{y_{n2}-y_{n1}}{x_{n2}-x_{n1}}\right) + 2\pi & x_{n2} > x_{n1}, y_{n2} < y_{n1} \end{cases} \quad (10)$$

That is,  $\alpha = 0^\circ, 180^\circ$  for “horizontal” nets and  $\alpha = 90^\circ, 270^\circ$  for “vertical” nets. Routing these horizontal and vertical nets typically results in more detour length, in addition to  $\mathcal{HPWL}_n$ , than routing nets with other angles. Therefore, we chose to

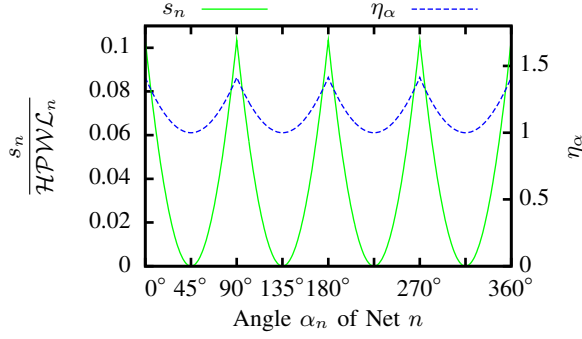


Fig. 9. Plot of  $s_n$  and  $\eta_\alpha$  against angle of net  $n$  (see Eq. 14).

define the width  $s_n$  of the routing detour region  $\mathcal{S}_n$  to depend on the angle  $\alpha_n$  of net  $n$ .

Our choice for values of  $\eta_\alpha$  is based on practical experience of design experts and experimental data gained by examining benchmarks of the ISPD 2008 global routing contest [18]. These data indicate that for horizontal and vertical nets, a suitable value for factor  $\eta_{90}$  is between 1.20 and 1.45. For nets with an angle of  $45^\circ$ ,  $135^\circ$ ,  $225^\circ$ , or  $315^\circ$ , the best value for factor  $\eta_{45}$  is 1.0.

From the above assumption, i.e.,  $\eta_{45} = 1.0$  for  $45^\circ$  nets, follows that the area of region  $\mathcal{S}_{45}$  is zero.

$$\mathcal{S}_{45} = 0 \quad | \quad \eta_{45} = 1.0 \quad (11)$$

Additionally, we state that the combined region  $\mathcal{S}'_n$  (which, for reasons of simplification, is region  $\mathcal{S}_n$  combined with the two “shadowed” regions behind the two pins) plus region  $\mathcal{MH}_n$  for any net  $n$  shall be equal to the region  $\mathcal{MH}_{45}$  of a diagonal net  $n_{45}$  ( $\delta x_{45} = \delta y_{45}$ ) of the same Manhattan length ( $\delta x_n + \delta y_n = \delta x_{45} + \delta y_{45}$ ).

$$\mathcal{MH}_n + \mathcal{S}'_n \stackrel{\text{by def.}}{=} \mathcal{MH}_{45} \quad (12)$$

$$(\delta x_n + 2 \cdot s_n) \cdot (\delta y_n + 2 \cdot s_n) = \delta x_{45} \cdot \delta y_{45} \quad (13)$$

Following the above assumptions and definition we calculate width  $s_n$  of the routing detour region  $\mathcal{S}_n$  as follows:

$$s_n = \sqrt{\frac{1}{8} (\delta x_n^2 + \delta y_n^2)} - \frac{1}{4} (\delta x_n + \delta y_n) \quad (14)$$

This results in  $\eta_{90} = \sqrt{2}$  and  $\eta_{45} = 1$ , i.e. no detour is allowed for the routing of diagonal nets. The longest detoured routing path for horizontal and vertical nets is factor  $\sqrt{2} - 1$  longer than their shortest possible Manhattan path. Consequently, for a specific desired maximum length  $\eta_{90} \cdot \mathcal{HPWL}_n$  of the detoured routing path, the value  $s_n$  can be adjusted by:

$$s'_n = s_n \cdot \frac{\eta_{90} - 1}{\sqrt{2} - 1} \quad (15)$$

If, for example, the maximum of an allowed detoured routing path length should be 120% of the shortest possible routing path length, then  $\eta_{90} = 1.20$  and  $s'_n = s_n \cdot \frac{0.20}{\sqrt{2}-1} \approx 0.4828 \cdot s_n$ . Please refer to Fig. 9 for a plot of  $\eta_\alpha$  and  $s_n$  depending on the angle  $\alpha_n$  of net  $n$  with  $\eta_{90} = \sqrt{2}$ .

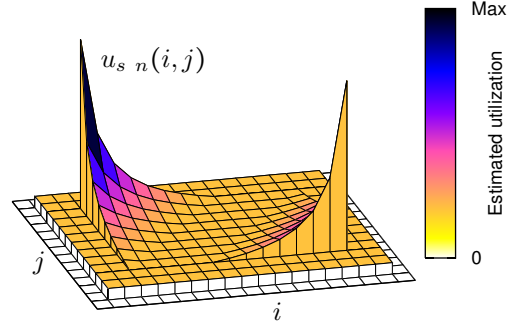


Fig. 10. Utilization estimation including routing detour.

For the estimated utilization in the routing detour region  $\mathcal{S}'_n$  we state:

- The utilization is evenly distributed within  $\mathcal{S}'_n$ .
- Any amount of utilization added to the detour region  $\mathcal{S}'_n$  has to be subtracted from within the Manhattan window  $\mathcal{MH}_n$ . This assures that the overall estimated utilization is linearly proportional to the net length and thus, comparable/summable for several nets.
- The minimum of the estimated utilization within  $\mathcal{MH}_n$  is equal to the utilization value in the routing detour region  $\mathcal{S}'_n$ .

Let the minimum of the estimated utilization within the Manhattan window be  $u_{min\ n}$ , which is for example equal to  $u_n(\delta x_n, 0)$ , then the estimated utilization  $u_{s\ n}(i, j)$  considering detoured routing is

$$u_{s\ n}(i, j) = \begin{cases} u_n(i, j) - u_{corr\ n} & | \text{ within } \mathcal{MH}_n \\ u_{min\ n} - u_{corr\ n} & | \text{ in } \mathcal{S}'_n \end{cases} \quad (16)$$

where  $u_{corr\ n}$  has to be calculated as follows in order to fulfill the above listed statements:

$$u_{corr\ n} = u_{min\ n} \cdot \frac{4s_n^2 + 2s_n\delta x_n + 2s_n\delta y_n}{(2s_n + \delta x_n) \cdot (2s_n + \delta y_n)} \quad (17)$$

The resulting utilization prediction that includes routing detours through region  $\mathcal{S}'_n$  is illustrated in Fig. 10.

#### IV. ROUTABILITY EVALUATION OF PIN ASSIGNMENTS

In this section, we describe how to apply the above presented congestion prediction method and the deduced critical net length to determine routability for pin assignments. This evaluation can then be the basis for any heuristic to optimize pin assignment of interfaces between all hierarchy levels (Fig. 11).

To the best of our knowledge, our work is the first to propose probabilistic congestion prediction and using the cost term *critical net length* for pin assignment optimization. We combine new, congestion-based cost terms with the established terms net length, signal skew and signal intersections, to accomplish a comprehensive detailed routability evaluation. The individual terms are separately determined for the different hierarchy levels of the design and are subsequently combined into one value using weighted sums.



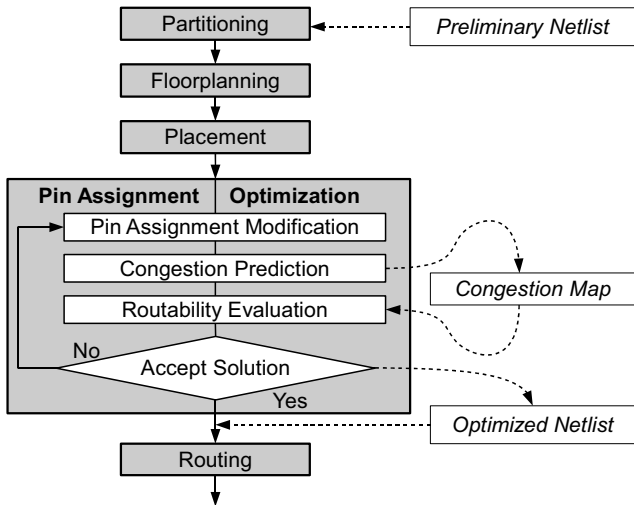


Fig. 11. Integration of pin assignment optimization into the layout synthesis process. Related input and output data are indicated on the right.

For all hierarchy levels  $l$  of system  $\mathcal{L}$ , we determine the following terms based on the adapted probabilistic congestion prediction described in Sec. III:

- The maximum utilization  $\hat{U}_l$ , which allows evaluating the severity of the most congested spots:

$$\hat{U}_l = \max_{\forall (x,y) \in \mathcal{A}_l} U_l(x,y) \quad (18)$$

- The overall utilization  $\bar{U}_l$ :

$$\bar{U}_l = \sum_{(x,y) \in \mathcal{A}_l} U_l(x,y) \quad (19)$$

- The utilization's standard deviation  $\sigma_{U_l}$ , which evaluates how evenly utilization is spread:

$$\sigma_{U_l} = \sqrt{\frac{1}{|\mathcal{A}_l| - 1} \sum_{(x,y) \in \mathcal{A}_l} [U_l(x,y) - \bar{U}_l]^2} \quad (20)$$

- The average  $\bar{C}_l$  of the introduced critical net length, which allows evaluating the routability of all individual nets in detail (see Eq. 2):

$$\bar{C}_l = \frac{1}{|N_l|} \sum_{n \in N_l} C(n) \quad (21)$$

Furthermore, we determine the overall net length  $r_l$ , signal skew  $s_l$ , and the number of signal intersections  $\mathcal{I}_l$ . For that purpose, net lengths are estimated using minimum spanning trees, signal skew is calculated using the variation of the respective net lengths, and signal intersections are estimated as intersections of the nets' flylines [7].

The overall routability cost  $\mathcal{R}$  of a hierarchical system  $\mathcal{L}$ , as required for pin assignment optimization, is calculated based upon the mentioned individual cost terms:

$$\mathcal{R} = \sum_{l \in \mathcal{L}} \Psi_l \cdot \left\{ \psi_{l1} \cdot \hat{U}_l + \psi_{l2} \cdot \bar{U}_l + \psi_{l3} \cdot \sigma_{U_l} + \psi_{l4} \cdot \bar{C}_l + \psi_{l5} \cdot r_l + \psi_{l6} \cdot s_l + \psi_{l7} \cdot \mathcal{I}_l \right\} \quad (22)$$

Weights  $\Psi_l$  define the importance of the individual hierarchy levels  $l$ , while weights  $\psi_{l1} \dots \psi_{l7}$  define the preferences of the individual cost terms and allow prioritization of specific optimization targets. Varying routing widths of individual nets in different hierarchy levels are indirectly included in the routability cost  $\mathcal{R}$  through cost terms  $\hat{U}_l$ ,  $\bar{U}_l$ ,  $\sigma_{U_l}$ , and  $\bar{C}_l$ , since they are based on probabilistic congestion prediction, which in turn depends on individual routing widths and pitches.

## V. EXPERIMENTAL RESULTS

### A. Probabilistic Congestion Prediction

In general, any probabilistic prediction scheme based on a reasonable routing density distribution can be used to support the cost function presented in Sec. IV. To prove the prediction accuracy of our net model (Sec. III-C and III-D), we evaluated seven density distributions using data of the ISPD 2008 global routing contest [18]. Using 16 real-world routing benchmarks (with up to 1.6 million nets), we compared the real global routing results created by 12 different global routers with seven different probabilistically predicted congestion maps (Fig. 4). We considered the following probabilistic net models:

- 1) *Even* density distribution within the Manhattan window,
- 2) *Lou's* net model [10] (Fig. 3 b),
- 3) *Z-Shape* density distribution (Fig. 3 a),
- 4) *Westra's* net model [11], [12],
- 5) *L-Shape* density distribution,
- 6) *Sham's* net model [17], and
- 7) our net model "WF" (Sec. III-C and III-D) using four different parameters  $\eta_{90} = \{1.00, 1.15, 1.30, 1.45\}$ .

Considering all seven probabilistic prediction methods, we determined the average absolute estimation error for all routing bins and the Pearson product-moment correlation coefficient between estimated and real global routing results. We performed this analysis for all 16 benchmarks and all available global routing solutions (which were created by 12 different routers). The results are summarized in Fig. 12. Compared with each other, a prediction is better if the average error is lower and if the correlation coefficient is closer to 1.

The results show that our net model using parameter  $\eta_{90} = 1.45$  provides the best prediction accuracy. The results also reveal that a simple even density distribution achieves surprisingly good prediction accuracy, while distributions of Z-shape routing, L-shape routing, and the approaches in [10] and [11] are more sophisticated but provide less accurate predictions.

Please note that values larger than roughly 1.45 for  $\eta_{90}$  have no practical background.  $\eta_{90} = 1.45$  means horizontal and vertical nets may detour up to a length of 45% of their shortest possible Manhattan path. In practice, only rarely nets are routed using a longer detour. Consequently, we did not further increase  $\eta_{90}$  even though the results shown in Fig. 12 imply this could further improve prediction accuracy.

Runtimes for probabilistic congestion prediction range between 2 s and 40 s. This underscores its efficiency compared with global routing which, despite its accuracy in routability

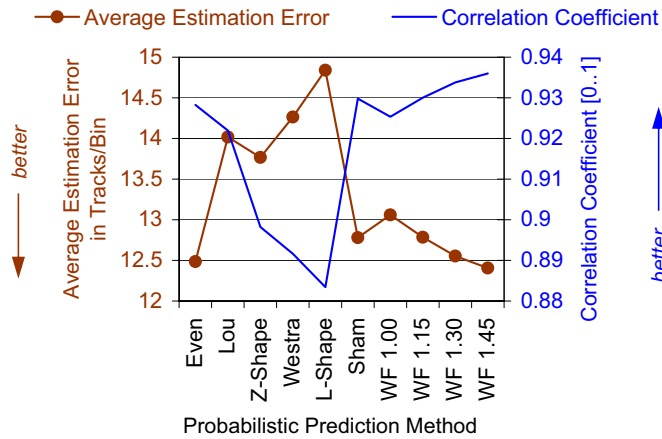


Fig. 12. Comparison of probabilistic congestion prediction methods. Six probabilistic prediction methods and our prediction method “WF” using four values for parameter  $\eta_{90} = \{1.00, 1.15, 1.30, 1.45\}$  are compared with global routing results. Our interface optimization uses the most accurate congestion prediction method “WF 1.45” (“predicted local congestion” in Tab. II).

TABLE I  
CHARACTERISTICS OF THREE CHIP-PACKAGE CO-DESIGNS.

Design	# of Chips in Package	# of Signal Nets
module (Fig. 13)	1	329
mcm2 (Fig. 1)	2	786
mcm7	7	2400

prediction, would be too runtime expensive to be used in interface optimization. (According to the ISPD benchmark data, global routers require from 2 minutes up to several hours to route the same benchmarks.)

### B. Hierarchical Pin Assignment

Having verified the accuracy of the probabilistic congestion prediction method in the previous section, we now show how this local probabilistic congestion prediction can effectively be used for routability evaluation. To illustrate the effectiveness of our evaluation terms, we present the results of three chip package designs (Tab. I). These designs consist of an interposer (chip carrier, package) that carries one, two, and seven flip-chips, respectively. We assume the pin assignment for the chip pins to be fixed and that the interface of the package must be optimized for routability.

As shown in Tab. II, we first use the conventional routability metrics Manhattan net length, signal skew, Euclidean net length, and signal intersections to optimize pin assignment. (Please note that it is not possible to optimize design “module” for a minimal overall Manhattan length because obviously all possible pin assignments result in identical lengths.) We then compare these pin assignments to a pin assignment that is optimized based on our local congestion prediction as described in Sec. IV. To report the actual routability of the different pin assignment solutions in Tab. II, we use the Cadence Spectra auto router to obtain the detailed routing solutions (see also Fig. 13).

TABLE II  
ANALYSIS OF THE ROUTABILITY OF PIN ASSIGNMENTS OPTIMIZED ON THE BASIS OF BASIC GEOMETRIC CHARACTERISTICS OR OUR CONGESTION PREDICTION METHOD (ROUTING RESULTS ACHIEVED WITH CADENCE SPECTRA AUTO ROUTER).

Design	Routability Optimization	Required # of Routing Layers	Wiring Length	Vias	Manufacturing Cost
module	Manhattan length	Optimization not possible			
	Euclidean length	6	40.1	746	100%
	Signal skew	6	40.1	723	100%
	Flyline intersections	4	40.0	739	67%
	Predicted local congestion	2	40.0	668	33%
mcm2	Manhattan length	8	9.9	842	100%
	Euclidean length	8	9.9	836	100%
	Signal skew	8	10.1	882	100%
	Flyline intersections	6	9.9	822	75%
	Predicted local congestion	6	9.9	801	75%
mcm7	Manhattan length	8	88.1	3364	100%
	Euclidean length	6	87.9	3078	75%
	Signal skew	8	88.9	3232	100%
	Flyline intersections	6	88.0	3062	75%
	Predicted local congestion	4	88.1	2962	50%

The routability of a pin assignment is considered to be better if the detailed routing can be completed in less routing layers and with less overall routing length and vias. The results show that the achieved overall routing lengths are virtually identical for all pin assignments, while the numbers of required routing layers and vias differ significantly.

The pin assignments optimized based on local congestion prediction provide the best routability. For example, design “module” can be completely routed in two layers only when using our methodology. For this example we achieved a reduction by four and two routing layers, respectively, by introducing the critical net length, our new local congestion-prediction-based term, to evaluate routability. Since manufacturing costs for modules and boards are dominated by the number of required routing layers, this is equivalent to a reduction of the manufacturing costs by approximately 67% and 50%, respectively [19].

The above results affirm the efficiency of the improved cost function in one hierarchy level of chip-package-board co-design, namely package routing. Moreover, the presented cost function equally enables a concurrent optimization of several hierarchy levels (overall routability of package and board). Thus, for pin assignment tasks with multiple hierarchy levels, two characteristics of our approach support the overall goal of improved routability: Firstly, a fast and detailed routability evaluation achieved by local congestion-based terms. Secondly, the ability to concurrently optimize all system levels, i.e. being able to find a trade-off of the routabilities in the individual system levels such that the overall routability is maximized in a time-efficient manner.

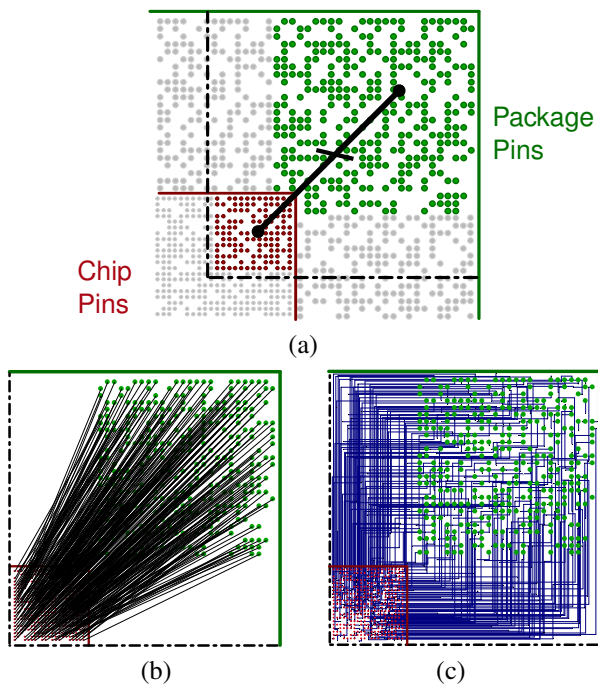


Fig. 13. Pin assignment task of chip-package co-design (a). Sample pin assignment (flylines) (b) and the respective detailed routing solution (c). Only a subset of all chip and package pins is illustrated.

## VI. SUMMARY

We presented an efficient methodology to evaluate the overall routability of a hierarchical system during pin assignment optimization of the interfaces between hierarchy levels. Our quantitative evaluation enables detailed manual and automatic optimization of the interfaces. It provides a more detailed routability evaluation than previous approaches because we include local-congestion-based terms for each hierarchy level. At the same time, it is faster than global-routing-based methods since potential routing conflicts are not resolved in detail. Ignoring the details of specific routing conflicts is furthermore beneficial because resolving them requires detailed knowledge of routing resource constraints. However, often this information is not yet available during the early optimization of interfaces. Consequently, probabilistic congestion prediction is inherently better suited for early routability evaluation of interfaces than global routing.

To achieve the improved evaluation, we adapted probabilistic congestion prediction to the special requirements of interface routability evaluation at early stages of physical design. We validated the accuracy of our adaptation by comparing it to six other prediction methods using data of the ISPD 2008 global routing contest.

Thereupon we introduced metrics like the critical net length, which are based on adapted local congestion prediction and reflect details of routability in all levels of a hierarchical design. We illustrated their efficiency for routability optimization during interface definition using three co-designs. For this purpose, we applied different routability metrics during pin assignment optimization and compared the resulting detailed routing results.

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