Electromigration Analysis of VLSI Circuits Using the Finite Element Method

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Abstract. Addressing electromigration (EM) during physical design has become crucial to ensure reliable integrated circuits. Simulation methods, such as the finite element method (FEM), are increasingly overwhelmed by the complexity of the task. With further technology scaling, it is predicted that FEM will not be usable anymore for a full-chip EM analysis due to complexity reasons. To address this bottleneck, we present a new methodology enabling an FEM-based full-chip EM analysis for future technologies down to 10 nm feature sizes. Our solution reduces analysis costs significantly by establishing pre-validated layout patterns without losing accuracy of the verification results. We thoroughly evaluate the necessary pattern geometries, pattern library size and the calculation time savings. We show that a number of 10 to 20 different patterns is sufficient for generation and analysis of layouts provided that the same pitch is used for each metal layer. Our full-chip meta-model EM analysis allows speedups of at least 10X compared to current FEM-based verification methods.

Keywords: FEM · Electromigration · Interconnect · Reliability · Physical verification · Routing

1 Introduction

Excessive current density within interconnects is a major concern for integrated circuit (IC) designers because it causes electromigration (EM). Due to smaller feature sizes, this is a growing reliability issue in modern ICs [1]. While analog designers have been aware of this issue for some time, digital designs are now being affected as well [2–4].

EM is a migration process mostly driven by momentum transfer between electrons and metal ions of the wire. It causes damage through formation of voids and hillocks. While directly depending on current density, damage takes place mostly in locations of inhomogeneous electric currents, such as vias or non-linear wiring shapes.

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EM analysis by simulation helps to find excessive current densities in the layout. Hence, current-density verification has emerged as an important verification step in VLSI physical design. The most common method of analysis is the finite element method (FEM). While it has been widely accepted in analog layout verification, using FEM in significantly more complex digital circuits faces numerous challenges.

FEM uses meshes for discretization of arbitrary shapes of continuous matter (Fig. 1). Each node and element of the mesh has its degrees of freedom to contribute to a linear system of differential equations. Therefore, the size of this system of equations and the calculation time depends on the number of nodes in the mesh.

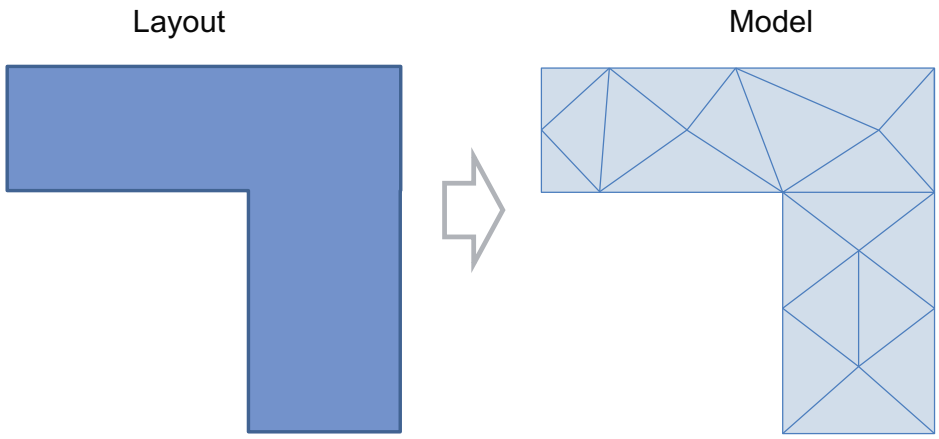

Fig. 1. Example for meshing of a model for FEM simulation.

Digital integrated circuits usually contain a large number of transistors and nets. Additionally, current densities are growing with decreasing feature sizes [1]. To make matters worse, current density limits are also shrinking due to smaller structure sizes (Fig. 2 and Sect. 2).

As stated by [1], all minimum-sized wires in integrated circuits have been EM-affected since 2018. Subsequently, all wiring elements (segments, vias) of these circuits must be subjected to EM verification and analysis; totaling billions of elements for some circuits.

As FEM is commonly used for detailed analyses, the complexity of future circuits will demand excessive calculation cost. For full-chip analysis, other simulation methods are more time-efficient, but with the drawback of less detailed results and information loss in terms of potential void locations, for example. To the authors' knowledge, only FEM and similar methods, such as the finite-difference method (FDM), possess the capability of spatially resolved analysis to visualize excessive current densities.

The FDM is numerically very simple and therefore well suited for theoretical analysis or very fast calculations. Due to its simplicity, its results are not as accurate as with FEM. As its name suggests, the system of equations is based on the differences in the degrees of freedom.

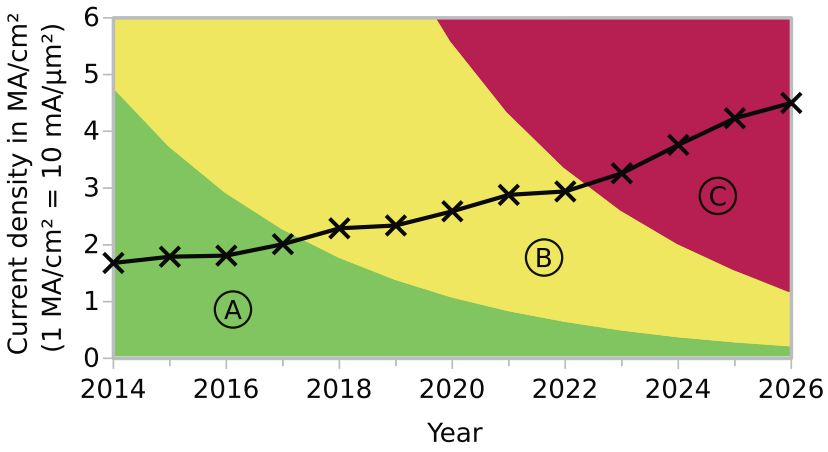

Fig. 2. Evolution of the required current density for driving four inverter gates for leading edge technologies according to ITRS roadmap [1]. As also shown, the maximum tolerable current density limits are shrinking due to smaller structure sizes. Region A/green: local EM issues, region B/yellow: all wires EM-affected, region C/red: no EM-solutions known yet. (Color figure online)

A similar methodology exists in the finite volume method (FVM). It uses polyhedrons to divide the given geometry, while solving the equations only at the center of each polyhedron. The FVM is best suited for conservational equations, such as mass flow calculations for fluid and gas transport. It can be applied to migration when modeling atomic flux similar to gas diffusion.

FDM and FVM are less favorable for EM simulations then FEM due to their reduced accuracy and the missing availability of simulation tools. FEM-based verification will only be usable in the future if we achieve a significant reduction in simulation time. To meet this demand, we proposed in [5] a new methodology that reduces simulation time at least tenfold by using FEM for pre-layout pattern analysis without accuracy loss.

This chapter extends our previous work [5] significantly by describing in detail the implementation of the pattern generation process (Sect. 6). We also performed a more elaborate quantification of the benefits of our approach. Furthermore, the basic simulation methods are discussed in detail.

The remainder of this chapter is structured as follows. We first discuss the EM challenges of future VLSI design (Sect. 2), introduce the FEM as a method for EM analysis (Sect. 3) and formulate its limitations (Sect. 4). A solution for the complexity problem is presented in Sect. 5, accompanied by an implementation of the pattern generation method in Sect. 6 and a verification of its benefits in Sect. 7. Section 8 summarizes our results.

2 The Need for EM Analysis

Size reduction of semiconductor structures is mainly driven by the need for higher circuit performance, efficiency at higher frequencies and smaller footprints. Furthermore, line widths and wire cross-sectional areas decrease over time to meet

routing requirements of semiconductors. Table 1 shows that the cross-sectional area of Metal 1 shrinks from 1600 nm^2 in 2016 to roughly 600 nm^2 in 2020. Although currents are decreasing as well due to shrinking gate capacitances and supply voltages (see Table 1), current densities increase because of the significantly larger decrease of cross-sectional areas.

To make matters worse, smaller feature sizes limit the maximum tolerable current densities, because small material defects will cause a dramatic change in resistance or even damage of the wires. As a result, maximum tolerable current densities must decrease to maintain a constant reliability [1,2]. The ITRS [1] indicates that all minimum-sized interconnects have been EM-affected since 2018. Therefore, any further downscaling of wire sizes is increasingly restricted by current density constraints (marked by the yellow region B in Fig. 2).

Taking into account that the total interconnect length per IC will continue to increase, reliability requirements per length unit of the wires need to increase in order to maintain overall IC reliability. However, the future decrease in interconnect reliability due to EM – as noted above – conflicts with these requirements. As the ITRS states that there are no known solutions to meet the EM-related reliability requirements of technologies in the near future (Fig. 2, red region C), there is a strong need for time-efficient, full-chip EM analysis.

3 Finite Element Method for EM Analysis

3.1 General Approach for EM Analysis

The finite element method can help analyzing the EM susceptibility by different approaches. The most obvious application of FEM in EM analysis is the calculation of current densities. As it is impracticable to calculate current densities analytically, the use of finite elements enables to lower the calculation costs. Current densities are calculated by solving the linear field equation for the electric field under voltage or current boundary conditions [6].

Nevertheless, not only current density influences migration. Also temperature and, especially at small feature sizes, mechanical stress must be considered in the simulation. This multi-physics problem is described by the diffusion equation [7] and results in an atomic flux under electromigration, thermomigration and mechanical stress as in

$$J_{\text{total}} = J_{\text{EM}} + J_{\text{TM}} + J_{\text{SM}}, \tag{1}$$

where J_{total} is the whole mass flux, and J_{EM}, J_{TM}, J_{SM} describe the mass flux caused by electromigration, thermomigration and stress migration, respectively.

Diffusion can be determined using quasi-static simulation by calculating the initial atomic flow. Lifetime and robustness will be estimated by extrapolation of this flow.

The applicability of finite element models for simulating migration processes and void growth until failures occur has been shown in [8,9]. However, those simulations are very time-consuming and therefore not applicable to a full-chip EM analysis in VLSI physical design.

Table 1. Technology parameters based on the ITRS, 2013 edition [1]; maximum currents and current densities for copper at 105 °C

Year	2016	2018	2020	2022	2024	2026
Gate Length (nm)	15.34	12.78	10.65	8.88	7.4	6.16
On-chip local clock frequency (GHz)	4.555	4.927	5.329	5.764	6.234	6.743
DC equivalent maximum current (μA)[a]	29.09	23.19	16.52	12.40	10.00	7.90
Metal 1 properties						
Width – halfpitch (nm)	28.35	22.50	17.86	14.17	11.25	8.93
Aspect ratio	2.0	2.0	2.0	2.1	2.1	2.2
Layer thickness (nm)[a]	56.70	45.00	35.72	29.76	23.63	19.65
Cross sectional area (nm^2)[a]	1607.4	1012.5	638.0	421.7	265.8	175.5
DC equivalent current densities (MA/cm^2)						
Maximum current density without EM degradation[b]	3.0	1.8	1.1	0.7	0.4	0.3
Maximum current density (solution unknown)[b]	15.4	9.3	5.6	3.4	2.1	1.2
Required current density for driving four inverter gates	1.81	**2.29**	**2.59**	**2.94**	**3.76**	**4.50**

[a] Calculated values, based on given width W, aspect ratio A/R, and current density J in [1], as follows: layer thickness $T = A/R \times W$, cross-sectional area $A = W \times T$ and current $I = J \times A$.
[b] Approximated values from the ITRS Figure INTC9 [1].
All remaining values are from the ITRS 2013 edition [1].

3.2 Benefits of FEM

As already indicated, FEM has great benefits compared to faster techniques. In contrast to lumped element simulations, FEM offers simulation results with spatial resolution. This information is especially important when dealing with problems like EM, which cause failures by local damage. At the same time, FEM is more flexible and less time-consuming than analytic or continuous methods, when dealing with complex geometries. By scaling of the elements' size, calculation effort can be optimized depending on accuracy requirements.

3.3 Application in Physical Design

Current physical design tools such as [10–12] have built-in functionality for current density and, thus, EM analysis. Most analysis tools are based on the finite element method for calculating current density and temperatures. Still, those practical CAD applications only implement a small portion of the capability FEM tools used in other disciplines possess. Mostly, they use single-physics elements due to limitation of computing time. These tools cannot consider all effects connected with EM, such as mechanical stress and temperature gradients.

Analog designers make extensive use of the offered analysis tools. In digital designs, the available tools are increasingly limited to power and ground nets due to the excessive number of signal nets. Some authors, e.g. in [13], propose filter functions to address this complexity problem. Those filters rely on the availability of current information for all nets. This, and the fact that all nets become potentially critical in future digital designs, limit the use of the mentioned filters. As a result of this increase in verification complexity, FEM will no longer be usable for full-chip current density calculation.

4 Problem Formulation: Limitations of FEM

4.1 Model Size Restriction

More and more nets are becoming EM-affected in digital designs [1], while at the same time design complexity increases due to down-scaling. It is practically impossible to use FEM for digital full-chip analysis. Based on the ITRS roadmap, Fig. 3 shows a prediction of the analysis problem complexity for current and future digital circuits.

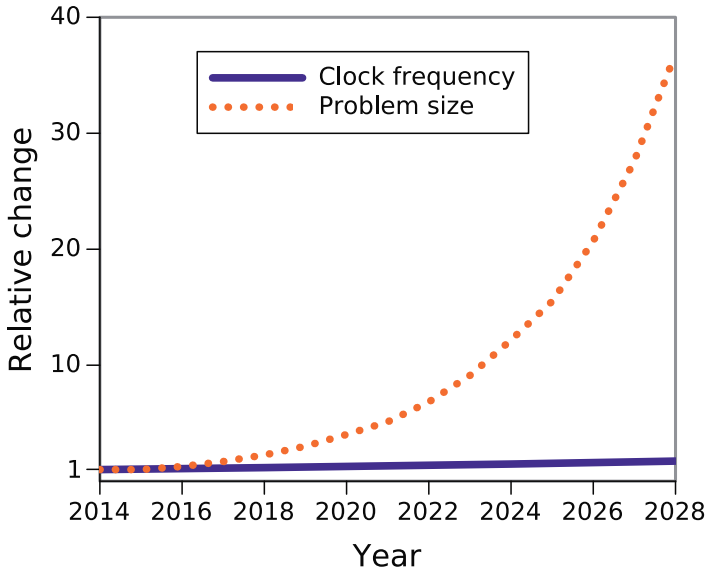

Fig. 3. Complexity of finite element simulations of all signal nets in current and future technologies, as predicted by the ITRS relative to 2014. The respective clock frequency of CPUs is also depicted for comparison. Calculated from ITRS [1].

FEM works with meshed geometric models, where physical properties are assigned to discrete nodes and elements. Generally, precision and calculation time of FEM problems depend on model size, i.e. on the number of nodes and elements of the mesh. To gain a result in a given time, model size has to be limited. Precision demands a certain number of nodes per volume, therefore, the simulated volume per FE model has to be restricted.

FEM is limited to small portions of a layout. Hence, critical layout areas have to be identified and filtered. However, filters, like those proposed in [13], will no longer mitigate the complexity problem. Hence, FEM will not be usable anymore, as simulation cost would grow enormously.

Due to the large scale of whole chip models, the number of sub-models used in FEM will increase with technology progress. To limit this increase, we suggest the use of re-usable sub-models. That means, *standardized* sub-units of the interconnect structure have to be established and re-used. This leads to a layout composed of a large number of few, pre-determined basic building blocks in terms of interconnect structures that would facilitate the FEM analysis. The gained efficiency for EM verification from our approach increases with growing layout complexity.

4.2 Atomic Scale Restriction

Further downscaling imposes limitations due to influences of the atomic scale. At feature sizes in the range of 4 to 5 nm, single atoms affect the failure probability, i.e., if there is a failure or not. Hence, the wire cannot be regarded as a continuum. The violation of this fundamental demand for FEM disallows further use of this method in those size ranges. When going near this point, strong inhomogeneities may occur. These can be dealt with by using non-linear models for EM calculation as it has been applied to different other inhomogeneities on a micro scale. Hence, our approach is restricted to all technologies with a metal pitch not smaller than 10 nm.

5 Our Approach: Pattern Verification

Our approach uses the advantages of FEM without the necessity of large models or a great number of smaller FE models consuming a lot of computing power. The basic principle is to simulate patterns of wire structures that are used for routing afterwards. Layout patterns with a high repetition rate in layout, i.e., that are common, have to be determined and pre-simulated. Hence, simulation costs of the final layout verification can be significantly reduced (see Sect. 7.3).

5.1 Basic Principle

We propose a pre-layout simulation of metalization patterns and the restriction of routing to those simulated patterns. Our method is based on the following (Fig. 4):

- Technology restrictions will be taken into account for FE simulation.
- All common patterns needed for interconnection analysis are generated and simulated by FEM.
- These pre-defined layout patterns comprise typical wiring elements, such as via connections, long and short wires, and in-layer junctions (T-shaped or crossing).

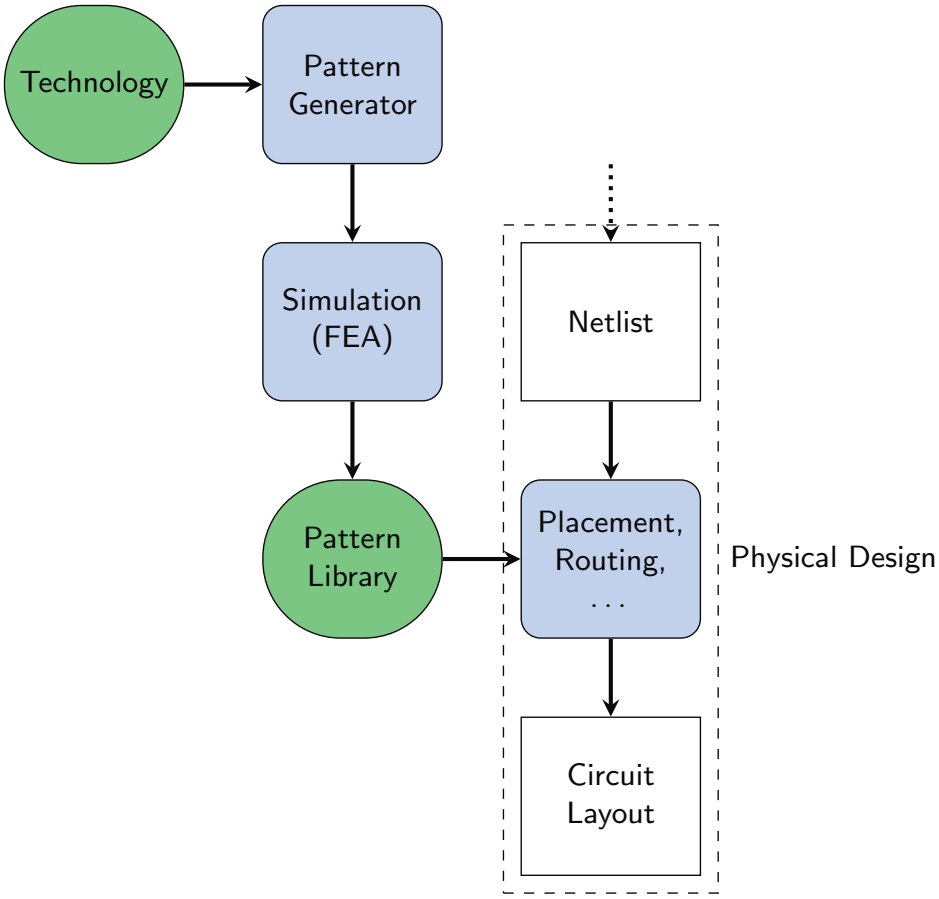

Fig. 4. Layout synthesis using our proposed pattern verification method.

- The EM robustness of the patterns for individual current constraints is verified by simulation.
- Routing is performed using wiring patterns suitable for particular currents of the nets.

While these measures alone cannot guarantee a reliable design, they are the foundation to enable a full-chip verification to ensure circuit reliability (see subsequent sections).

5.2 Pattern Choice

The requirements for deducing a full-chip verification from the verification of all its elements are as follows:

- currents should be equally distributed at model boundaries,
- temperature influences and mechanical stress from the neighborhood should be negligible, and
- diffusion at the boundaries should be known or zero.

The last point is easily satisfiable if model boundaries with current flow are always at the boundary between different materials, e.g. at tungsten plugs connecting to silicon or metal-via interfaces containing diffusion barriers. However,

the first requirement is not fulfilled in this case, as the interfaces are always near current crowding regions due to turns of the current direction from horizontal to vertical or vice versa. By adding geometric appendices to the model at such boundaries, the correct current distribution at the boundary can be achieved while the results inside the appendix are ignored.

Mechanical and thermal influences are harder to neglect, as they do not only influence a pattern or segment from two sides but they take effect from all around the simulation model. Both temperature and mechanical stress are transmitted through the surrounding dielectric material.

5.3 From Pattern Verification to Full Chip Verification

We will show how FE simulations can be performed without knowing the surrounding of a wiring pattern, as this is always the case when running a simulation prior to routing. A successful verification using a limited number of FE simulation is based on one of the following constraint assumptions:

1. A worst case analysis (all patterns are verified for the largest current in the circuit) is performed, where only the constraints have to be verified for the full-chip verification. This leads to robust, but over-sized designs.
2. An average estimation of constraints (FE simulations for typical loads) is performed. This can lead to partially unreliable systems.
3. The exact constraints are calculated. This is not feasible in pre-layout analysis.
4. New estimation metrics for constraints based on known current values are used. This approach works with meta-models of the design patterns that can be used in a full-chip analysis using concentrated elements.
5. Different variants of the same pattern type are simulated, where a certain pattern can be selected from the library depending on actual constraints.

The approach (4) using meta-models is the most promising. It demands some additional simulation time during or after routing, but this time is limited due to the use of simple models. The proposed meta-models are mathematical relations between FE model constraints and result quantities, e.g. maximum current density. Additional constraints to be implemented are current values (from circuit simulation) and hydrostatic stress. As a first implementation, both are only propagated at the electrically conducting boundaries between neighboring interconnect patterns. Therefore, a limited amount of additional simulation data is created.

When proceeding to smaller scale, it might also become necessary to propagate hydrostatic stress between wiring elements that are not electrically connected. Here lies the limitation of this approach, because the full-chip model complexity will then increase comparably to interconnect simulation models incorporating capacitive crosstalk.

Given the before mentioned circumstances, the pattern analysis allows a reliability prediction of the entire wiring structure.

6 Pattern Generation

6.1 Number of Needed Patterns

A large variety of patterns might be necessary to model the whole wiring of an integrated circuit. The number of needed patterns depends strongly on the metallization layer system and the technology/routing constraints of each interconnect layer. However, a small number of patterns is required if all considered metal layers have the same routing pitch and only single vias are used. This simplified case will be analyzed in the following section. Redundant vias and a variance in wire widths or interconnect pitches will increase the pattern number, while restrictions in routing direction or via pitch will decrease this number.

6.2 Generation of Sample Patterns

Using the above mentioned restrictions (i.e., only one wiring pitch for all layers, only single vias, and minimum wire widths), the number of possible patterns can be calculated. If we do not restrict the routing to certain directions on each layer, there are four ways (in a rectilinear or Manhattan routing fashion) to approach a via on a metal layer. We label these directions north (n), west (w), south (s), and east (e) as they can be represented by the directions of a compass. Every combination of directions, e.g. n, nw or we, can be allowed on a single layer, as the via of interest can be a Steiner or branching point in the net. We add the letter c to mark the center of our pattern, hence, we obtain *cn*, *cnw* or *cwe* as the names of our single-layer patterns. These combinations in one layer can be connected to each of these combinations on a second wiring layer, e.g. *cn_c_cnw* or *cnw_c_cwe*, where the c between the two underscores stands for a single via in the center, and the letters following the second underscore represent the directions on the second layer. This nomenclature also allows for redundant vias at either of the compass directions, e.g. *cn_cn_cnw*, which we do not consider in the remainder of this chapter. Figure 5 illustrates the nomenclature for some application-relevant patterns.

Theoretically, there are $2^8 = 256$ different patterns for a via structure if we assume that each wire direction can either be present or absent. The number of patterns can be dramatically reduced by looking for equal patterns, that can be transformed into each other only by rotation around the z-axis or mirroring at the xz or yz-plane. Obviously, up to eight different transformations are possible, while some of the transformation results end up in identical patterns. We developed a brute-force algorithm to calculate the number of distinct patterns (Algorithm 1).

Please note, that mirroring at the xy-plane leads to a different pattern, as the layer structure is not necessarily symmetric, e.g., there are usually diffusion barriers at the lower end of a via. This is especially the case when considering interconnects that are made by the dual-damascene technology.

The further naming convention for our distinct patterns is the following: We start on the lower metal layer in the north and continue counter-clockwise on the

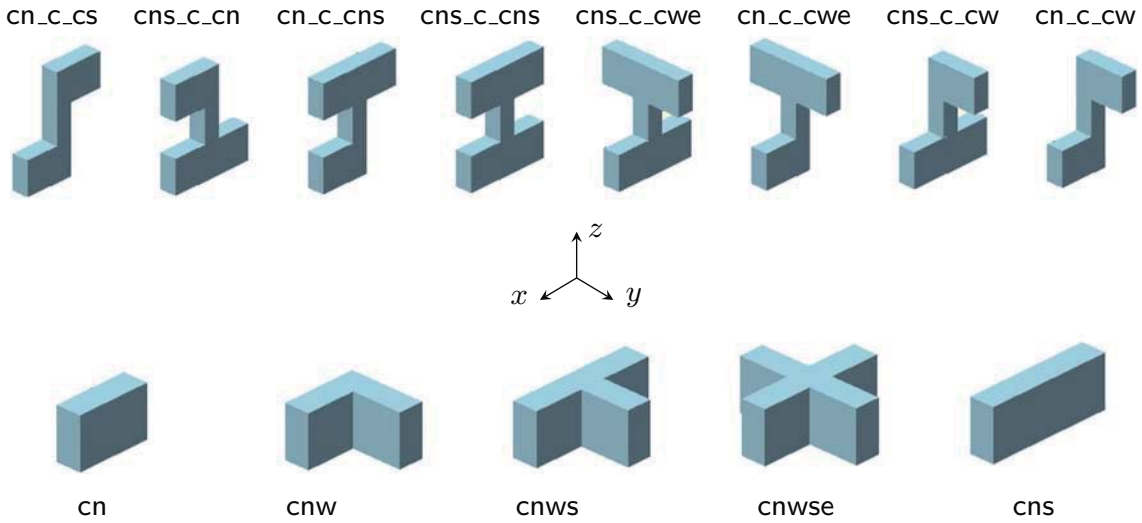

Fig. 5. Example patterns with their names; top: typical two-layer via patterns; bottom: all distinct single-layer patterns in rectilinear routing.

Algorithm 1. Generate a list of distinct patterns for single-via structures

```
1: for i=0 to 255 do
2:     pattern ← binary code of i
3:     variant[0..3] ← rotate(pattern)
4:     variant[4..7] ← rotate(mirror(pattern))
5:     if pattern not in variants_list then
6:         add pattern to pattern_list
7:         add variants to variants_list
```

lower layer and finish on the second metal layer. That is, *cnw* is preferred over *cne* and *cns_c_cw* over *cns_c_ce*. The 55 patterns, generated by Algorithm 1, are listed in Table 2. There are different numbers of equivalent patterns, that can be transformed into one distinct pattern. This number is 1, 2, 4 or 8, depending on the symmetry properties of each pattern.

In addition to the via patterns in Table 2, there are five single-layer patterns (see Fig. 5, lower line), of which only three (*cnw*, *cnws* and *cnwse*) are useful for FEM analysis. The electrical contacts of the pattern can either be at the ends of the wire segments that continue to certain compass directions or on the top or bottom surface of the centered via. The latter is obvious in the case of via pillars running across more than just two metal layers. Hence, more than the 55 patterns might be needed if we also consider branching of nets into some of the middle layers of a via pillar.

6.3 Restriction to Relevant Patterns

We searched our modified MCNC[1] benchmarks for all generated patterns and for the single-layer patterns to get a more application-oriented view on the necessary number of patterns and to see to which extend the simulation runtime can benefit from an increasing number of patterns. Patterns that are widely used in layout are best to include in a pattern library, while rarely used patterns may easily be excluded from the library and replaced by other patterns in the layout.

Table 2. List of generated distinct patterns for single via structures connecting two metal layers of the same pitch and the number of equivalent transformations N_{tr}.

Pattern	N_{tr}	Pattern	N_{tr}	Pattern	N_{tr}
cnwse_c_cnwse	1	cnw_c_cnwse	4	cn_c_cnwse	4
cnwse_c_cnws	4	cnw_c_cnws	8	cn_c_cnws	8
cnwse_c_cnw	4	cnw_c_cnw	4	cn_c_cnwe	4
cnwse_c_cns	2	cnw_c_cnse	8	cn_c_cnw	8
cnwse_c_cn	4	cnw_c_cns	8	cn_c_cns	4
cnwse_c_c	1	cnw_c_cne	8	cn_c_cn	4
cnws_c_cnwse	4	cnw_c_cn	8	cn_c_cwse	4
cnws_c_cnws	4	cnw_c_cse	4	cn_c_cws	8
cnws_c_cnwe	8	cnw_c_cs	8	cn_c_cwe	4
cnws_c_cnw	8	cnw_c_c	4	cn_c_cw	8
cnws_c_cnse	4	cns_c_cnwse	2	cn_c_cs	4
cnws_c_cns	4	cns_c_cnws	4	cn_c_c	4
cnws_c_cne	8	cns_c_cnwe	4	c_c_cnwse	1
cnws_c_cn	8	cns_c_cnw	8	c_c_cnws	4
cnws_c_cwe	4	cns_c_cns	2	c_c_cnw	4
cnws_c_cw	4	cns_c_cn	4	c_c_cns	2
cnws_c_ce	4	cns_c_cwe	2	c_c_cn	4
cnws_c_c	4	cns_c_cw	4	c_c_c	1
		cns_c_c	2		

The results in Tables 3 and 4 show clearly that only a fraction of the generated patterns is found in our benchmark layout. In the analyzed case, not even half of the patterns can be found, while some of them only exist in a small amount.

If we remove the rather *exotic* patterns, e.g., all patterns with a sum (last line of Tables 3 and 4) below 20, we can reduce the number of necessary patterns to 13 in our case. This will enable a compact pattern library. As an increase in library size is inevitable for more complex metalization systems, we should preemptively restrict the library size for our simplified case. A number of 10 to 20 distinct patterns is necessary for the analyzed case.

[1] The MCNC benchmark suite was originally obtained from [14] and adjusted to contain only single vias as outlined in [15].

Table 3. Counts of Patterns in the layouts of the MCNC benchmark suite (part 1/2). The first two columns contain single-layer patterns (cnw and cnws), the remainder shows different via patterns.

Benchmark	**Count per pattern**									
	cnw	cnws	c_c_c	c_c_cn	c_c_cns	c_c_cnws	c_c_cnw	cn_c_c	cn_c_cw	cn_c_cs
mcc1	552	0	146	1074	76	0	0	306	3988	2
mcc2	2704	1	1151	6601	45	0	0	1215	25175	1
primary1	1606	8	78	943	76	0	0	96	3936	13
primary2	5961	45	271	3475	445	0	0	372	16672	60
s13207	3937	28	205	1204	26	0	1	395	10631	9
s15850	4492	42	303	1544	39	0	0	523	12717	6
s38417	11362	124	599	3429	88	0	1	1002	31145	22
s38584	15649	140	957	4748	145	1	0	1550	41572	18
s5378	1537	9	132	685	15	0	0	243	5019	2
s9234	1480	19	93	486	4	0	0	155	4008	6
struct	3402	19	174	1478	146	0	0	242	5133	29
$\sum$	52682	435	4109	25667	1105	1	2	6099	159996	168

A larger number of patterns might be necessary for different interconnect technologies. This applies especially when different metal wire widths, vias of different sizes, or redundant vias are used. Hence, we conclude, that up to 200 different patterns will be sufficient to tackle interconnect structures with different pitches and redundant vias.

7 Verification

We choose the following method in order to verify our approach: Firstly (A), we show that partitioning FE models of the wiring is possible without losing accuracy of the current density results. Secondly (B), we present an application on full-chip examples to illustrate the scaling effect. Thirdly (C), the reduction in calculation time is estimated based on technology data.

7.1 Example Simulations for Patterns and Their Combination

It is important to verify that partitioning FE models of wiring is possible without losing accuracy of the current density results. This is done by comparing the simulation results of generic sample patterns calculated both separately and in combination. Different manually generated patterns from a generic technology have been analyzed. As an example, a T-shape inside one metal layer and a

Table 4. Counts of Patterns in the layouts of the MCNC benchmark suite (part 2/2). Some patterns are rarely used, e.g. *cnw_c_cn*, and, thus, can be easily removed from the pattern library without significantly changing the layout.

Benchmark	**Count per pattern**										
	cn_c_cwe	cn_c_cws	cn_c_cnw	cn_c_cnwe	cn_c_cwse	cns_c_c	cns_c_cw	cns_c_cwe	cnw_c_ce	cnw_c_cnw	cnw_c_cn
mcc1	148	0	0	0	0	4	198	3	3	0	0
mcc2	105	0	0	0	0	2	81	0	0	0	0
primary1	163	0	0	0	0	0	227	3	1	0	0
primary2	866	2	0	0	0	2	969	15	5	0	0
s13207	565	17	1	0	1	1	899	16	0	0	1
s15850	699	27	0	0	2	2	1038	19	3	0	0
s38417	1760	50	1	0	3	7	2790	43	2	0	0
s38584	2280	78	0	1	3	10	3941	70	5	2	0
s5378	213	5	0	0	0	1	417	7	0	0	0
s9234	260	8	0	0	2	1	337	5	0	0	0
struct	190	0	0	0	0	1	204	1	0	0	0
$\sum$	7249	187	2	1	11	31	11101	182	19	2	1

via connection are chosen. Figure 6 shows the current density results from two separate (distinct) simulations.

For comparison, the combination of these patterns is used in a second simulation (Fig. 7). The simulation results of the combined configuration are in good agreement with the separately calculated results.

Figure 8 indicates current density distribution at the interface between the two patterns in the common simulation, which is a measure for the error in the separate simulations. The maximum error is 3% in our case; this value has been verified for the other patterns (see Fig. 9) as well.

Hence, under the constraints mentioned in Sect. 5.3, simulation time can be significantly reduced by splitting an FE model into smaller parts while preserving the accuracy of the results.

7.2 Full-Chip Analysis

We chose layouts (Fig. 10) from the MCNC benchmark suite for verification and analyzed it in two ways:

1. FE simulation of the complete circuit *(full-chip, F)* and
2. partitioned simulation re-using repeated patterns *(partitioned, P)*.

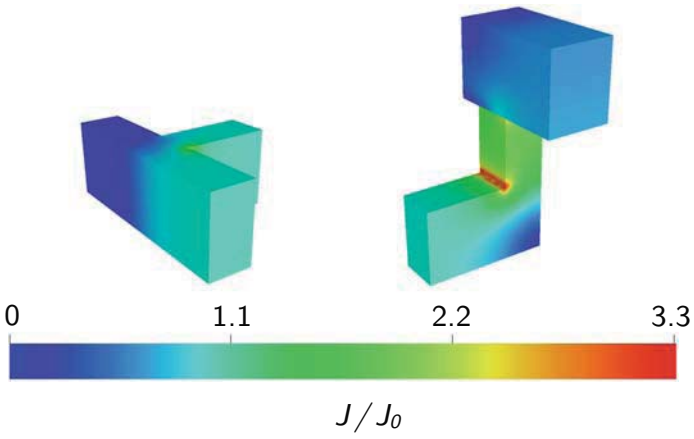

Fig. 6. Results of the separate simulations of single patterns with homogeneous constraints at the cut surfaces.

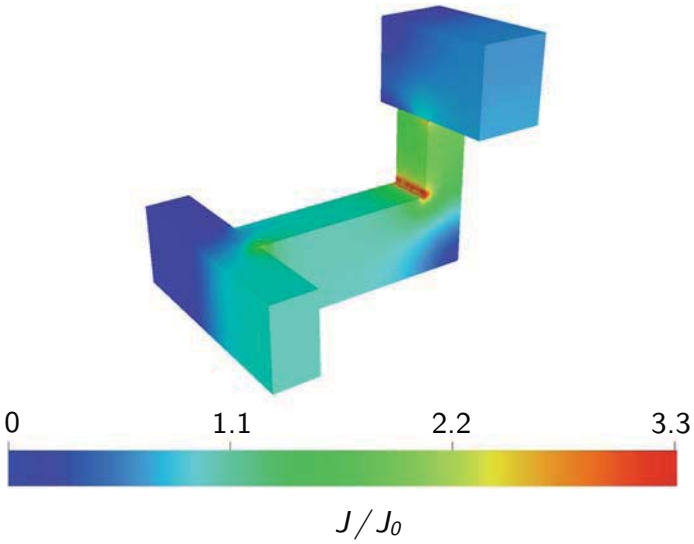

Fig. 7. The results of the common simulation of the two patterns are in good agreement with the results of the separate simulations from Fig. 6.

The first approach produces very large simulation models with $N_F > 10^7$ nodes and excessive simulation times $t_F > 70$ h. We can safely assume that FE simulation will be impossible with larger layouts in reasonable time. The second approach uses predefined and verified patterns (compare Figs. 6 and 9). An algorithm to localize the defined patterns has been implemented and applied to the benchmark layouts (Fig. 10). By reusing the patterns, the problem size is reduced to a significantly lower number of nodes N_P enabling a reduced simulation time t_P. Please note that by improving pattern choice, N_P can be reduced further.

Full-chip simulation time t_F is compared directly with simulation time t_P of the partitioned approach (Table 5).

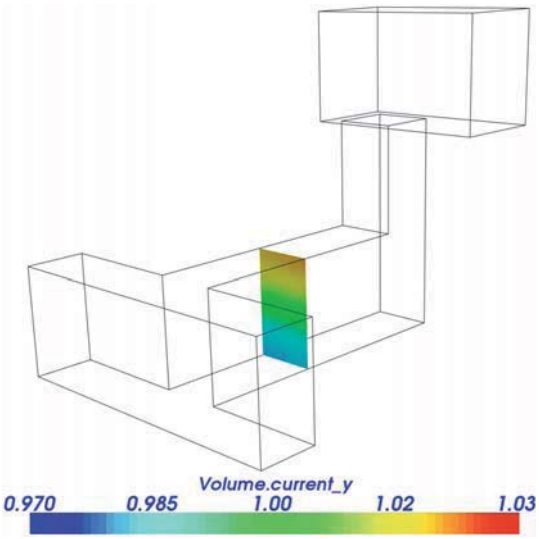

Fig. 8. Verifying homogeneity of the current density at the cut surface between the two sub-models (3 % maximum deviation here) ensures that distinct and combined simulations show matching results.

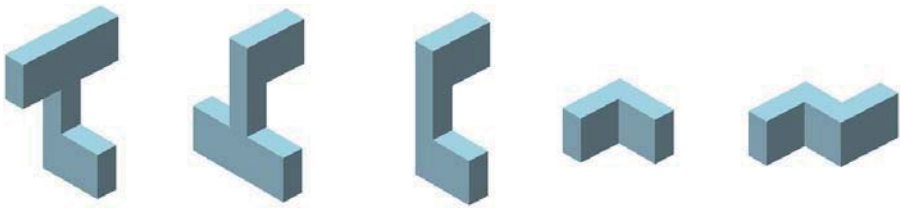

Fig. 9. Typical, pre-defined wiring and via patterns that have to be simulated by FEM in addition to those from Fig. 6.

The overall calculation time can be estimated by

$$t_{\mathrm{F}} \approx \quad P_{\mathrm{C}} \cdot t_1 \text{ and} \tag{2}$$

$$t_{\mathrm{P}} \approx P_{\mathrm{L}} \cdot t_1 + P_{\mathrm{C}} \cdot t_{\mathrm{m}}, \tag{3}$$

with the number of patterns per circuit P_{C}, the mean calculation time for FE simulation of a single pattern t_1, the number of patterns in a library P_{L}, and the mean calculation time for a pattern meta-model t_{m}.

All critical spots of the full-chip analysis can be detected using only 5 different patterns (see Fig. 9). As shown, simulation time can be reduced by a factor of at least 16 (Table 5). Please note that library buildup time, i.e., FE simulation of individual patterns, is included in our simulation time.

N_P is always 30,000 as similar pattern libraries are used for all benchmarks. Numbers of nodes and calculation times are estimated based on wire length and number of patterns in the layout (see Fig. 10). t_P includes the estimated meta-model evaluation time (see Eq. 3).

A larger pattern library can be worthwhile if a large number of layouts is to be analyzed, reducing the simulation time per layout even further.

7.3 Reduction in Simulation Time

The time needed for simulation using the pattern method comprises (a) the time needed for library buildup (FE simulation of individual patterns) and (b) the full-chip meta-model calculation time. The FE simulation of individual patterns (a) is only necessary once for a variety of similar circuits.

For a number P_L of patterns in a library, the proposed method results in a reduced simulation time compared to full chip analysis if $t_P(s) < t_F(s)$ or:

$$P_L \cdot t_1 + s \cdot P_C \cdot t_m < s \cdot P_C \cdot t_1, \tag{4}$$

with s the number of similar circuits to be analyzed.

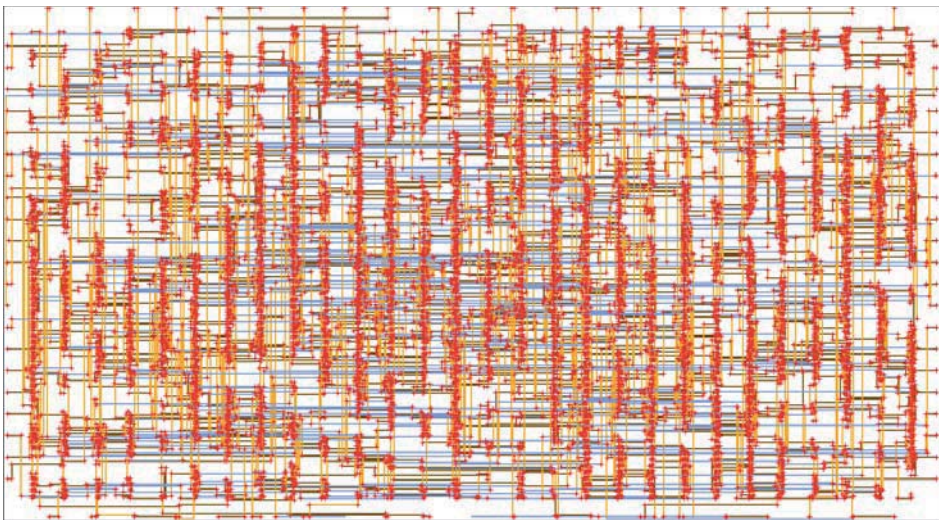

Fig. 10. Layout of the benchmark circuit *s5378*. Red crosses note the location of the example patterns of Fig. 9. (Color figure online)

That means, the approach accelerates the analysis if both the library contains much less patterns than a circuit and FE simulation time is greater than meta-model evaluation time. Due to increasing influences between model partitions with further downscaling of feature sizes, the number of patterns and the calculation time will rise. Figure 11 shows the difference in calculation time for $s = 1$, i.e., the pattern library is only used once (worst-case), illustrating nevertheless a speedup of at least 10 for current and future technologies.

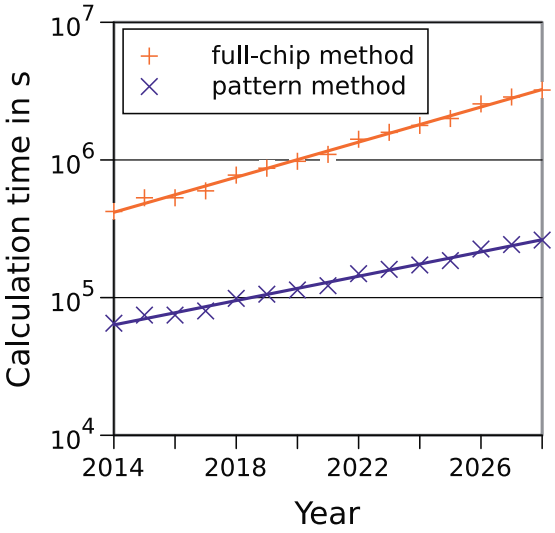

Fig. 11. Comparison of estimated calculation times between full-chip analysis and pattern method for $s = 1$ (one circuit verification per pattern library), calculated from technology parameters from [1].

Table 5. Experimental results of the layouts of the MCNC benchmark suite.

#	Benchmark name	Full-chip		Partitioned	
		N_F	t_F	t_P	Speedup
1	mcc1	3.8×10^7	106.2 h	3.4 h	31.6 ×
2	mcc2	4.0×10^8	1,106.8 h	19.5 h	56.6 ×
3	primary1	5.0×10^7	138.4 h	3.6 h	39.0 ×
4	primary2	2.0×10^8	569.8 h	14.5 h	39.2 ×
5	struct	5.6×10^7	154.6 h	5.5 h	28.2 ×
6	s13207	6.7×10^7	186.3 h	10.7 h	17.4 ×
7	s15850	8.0×10^7	221.9 h	12.7 h	17.5 ×
8	s38417	2.0×10^8	543.2 h	31.4 h	17.3 ×
9	s38584	2.6×10^8	728.1 h	41.8 h	17.4 ×
10	s5378	3.0×10^7	83.9 h	4.9 h	17.1 ×
11	s9234	2.5×10^7	70.1 h	4.2 h	16.7 ×

If the library models can be used multiple times for one circuit or if analyzing several similar circuits, i.e., $s > 1$, the difference between calculation times becomes even more significant. Specifically, when looking at the overall analysis time for large numbers of circuits, a speedup of at least 50 can be achieved, which nearly corresponds to the speedup of a meta-model calculation compared to an FE calculation.

8 Summary

Downscaling of the dimensions in integrated circuits leads to increasing problems with electromigration (EM) which needs to be tackled with greater awareness and more analyses. The finite element method (FEM) is well established in physical design and has proven itself in EM analysis.

Since FEM will struggle with circuit complexity, an alternative strategy is presented. Our approach uses FEM only for calculating generic layout elements (patterns) to build a meta-model library in advance. The layout will be created from a variety of library patterns, enabling a simple meta-model EM analysis. We verified our method using layouts of the MCNC benchmark suite and showed an acceleration of EM analysis by a factor of 16 and more. This acceleration factor will be (at least) the same when using parallel computing for FEM calculations, as our method provides good opportunities for parallelization.

Further work will investigate the practical implications of complex, nano-scale layout synthesis when using the proposed library patterns.

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