TECHNISCHE UNIVERSITÄT DRESDEN

ifte

Faculty of Electrical and Computer Engineering

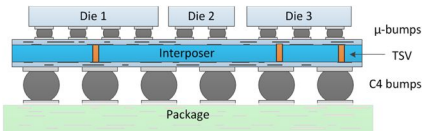
Optimal Die Placement for Interposer-Based 3D ICs

Sergii Osmolovskyi, Johann Knechtel,
Igor L. Markov and Jens Lienig

Jeju, Korea, Jan 24 2018

Outline

1. Motivation
2. Optimal placement framework (branch and bound)
3. Advanced pruning techniques
4. Results and Summary



https://www.ifte.de/mitarbeiter/lienig/ASP_DAC18.pdf

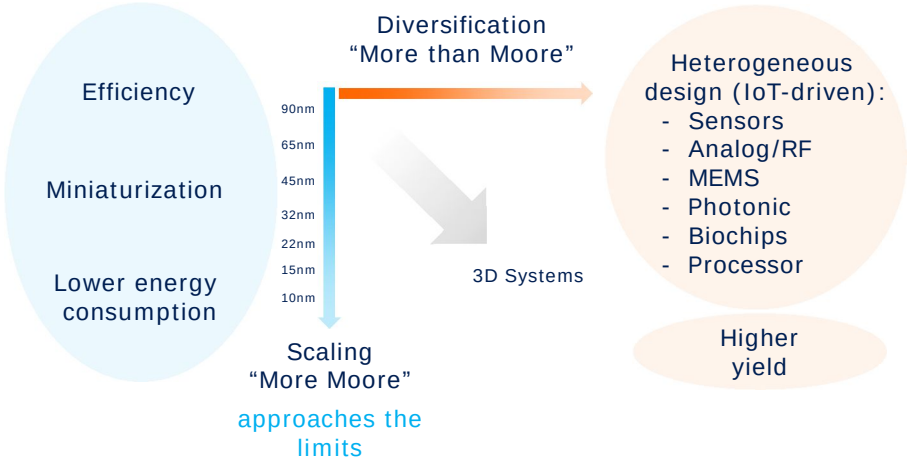
S. Osmolovskyi, J. Knechtel, I.L. Markov, J. Lienig "Optimal Die Placement for Interposer-Based 3D ICs," Proc. of the 23rd Asia and South Pacific Design Autom. Conf. (ASP-DAC 2018), pp. 513-520, Jan. 2018

Part 1

Why 3D Integration?
Why Interposer-based Chips and their Placement?

https://www.ifte.de/mitarbeiter/lienig/ASP_DAC18.pdf

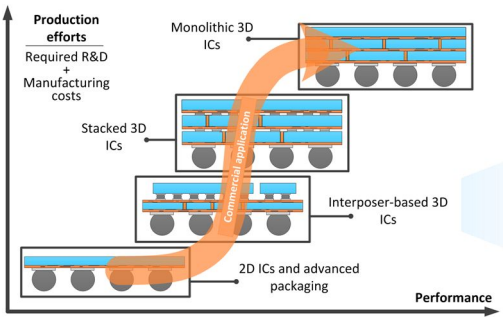
Modern Requirements for Chip Design



https://www.ifte.de/mitarbeiter/lienig/ASP_DAC18.pdf

S. Osmolovskyi, J. Knechtel, I.L. Markov, J. Lienig "Optimal Die Placement for Interposer-Based 3D ICs," Proc. of the 23rd Asia and South Pacific Design Autom. Conf. (ASP-DAC 2018), pp. 513-520, Jan. 2018

Advantages of Interposer-Based 2.5/3D ICs



Further advantages of interposer designs:

- Heterogeneous design
- Better heat dissipation
- Higher yield
- Existing / prefabricated chips can be mounted

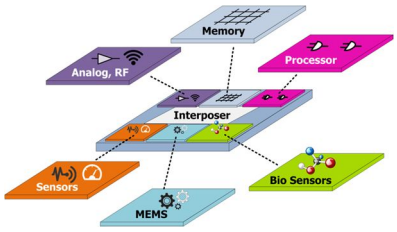
➢ Interposer-based 3D ICs are currently the most promising option for large-scale 3D integration

https://www.ifte.de/mitarbeiter/lienig/ASP_DAC18.pdf

Problem of Interposer Placement

Given:

- Prefabricated chips/dies with fixed pins
- Geometry of interposer with defined placement region
- Netlist



Goal:

- Placement with minimal wirelength

Only a few dies need to be placed
➢ optimal arrangement is accessible but challenging (combinatorial explosion)

https://www.ifte.de/mitarbeiter/lienig/ASP_DAC18.pdf

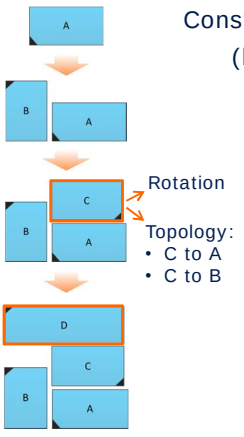
S. Osmolovskyi, J. Knechtel, I.L. Markov, J. Lienig "Optimal Die Placement for Interposer-Based 3D ICs," Proc. of the 23rd Asia and South Pacific Design Autom. Conf. (ASP-DAC 2018), pp. 513-520, Jan. 2018

Part 2

Optimal Placement Framework

https://www.ifte.de/mitarbeiter/lienig/ASP_DAC18.pdf

Placement Framework: Representation



Construct placement by adding dies one at a time

(based on constraint satisfaction problem, constraint graphs, and search trees)

For every new die we consider:

- Rotation: north (0°), west (90°), south (180°) and east (270°)
- Topological relation to already placed dies: left of / right of / above / below
- Optimal movement within deadspace

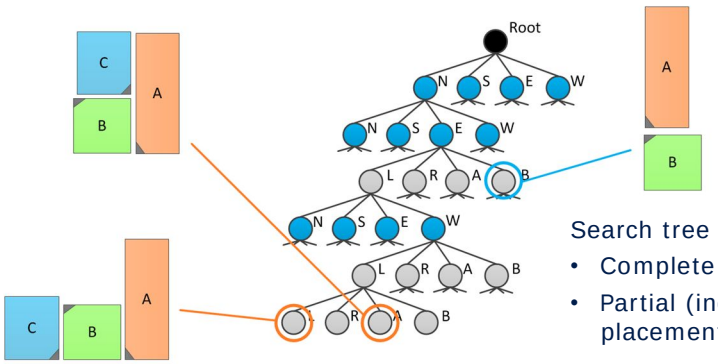
➢ All possible placement variations can be covered

https://www.ifte.de/mitarbeiter/lienig/ASP_DAC18.pdf

S. Osmolovskyi, J. Knechtel, I.L. Markov, J. Lienig "Optimal Die Placement for Interposer-Based 3D ICs," Proc. of the 23rd Asia and South Pacific Design Autom. Conf. (ASP-DAC 2018), pp. 513-520, Jan. 2018

Placement Framework: Search Tree

Incremental placement procedure is based on search tree



Search tree includes:

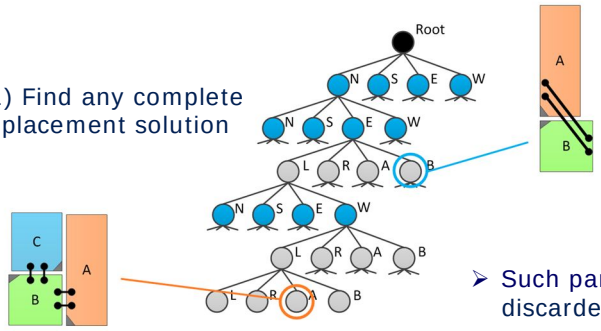
- Complete solutions
- Partial (incomplete) placements

https://www.ifte.de/mitarbeiter/lienig/ASP_DAC18.pdf

Placement Framework: Branch and Bound Approach

Discard partial placements if they cannot lead to optimal solutions

1) Find any complete placement solution



2) During traversal of tree: estimated WL of partial placement > WL of complete solution ?

➢ Such partial placements can be discarded w/o loss of optimality

https://www.ifte.de/mitarbeiter/lienig/ASP_DAC18.pdf

S. Osmolovskyi, J. Knechtel, I.L. Markov, J. Lienig "Optimal Die Placement for Interposer-Based 3D ICs," Proc. of the 23rd Asia and South Pacific Design Autom. Conf. (ASP-DAC 2018), pp. 513-520, Jan. 2018

Placement Framework: Branch and Bound Approach

Brute Force
~4,4·10^{12} nodes: ~43 days

Native Branch-and-Bound
263 million nodes: ~10 min

https://www.ifte.de/mitarbeiter/lienig/ASP_DAC18.pdf

Part 3

Advanced Pruning Techniques

https://www.ifte.de/mitarbeiter/lienig/ASP_DAC18.pdf

S. Osmolovskyi, J. Knechtel, I.L. Markov, J. Lienig "Optimal Die Placement for Interposer-Based 3D ICs," Proc. of the 23rd Asia and South Pacific Design Autom. Conf. (ASP-DAC 2018), pp. 513-520, Jan. 2018

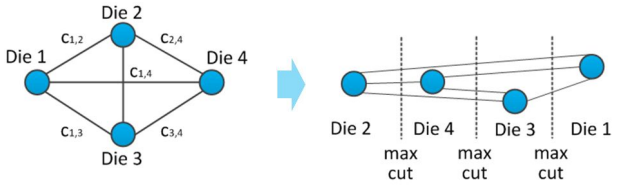
Advanced Pruning Techniques: Placement Schedule

Dies with large impact on total WL shall be considered early

(Previous works: schedule based only on die size)

Proposed:

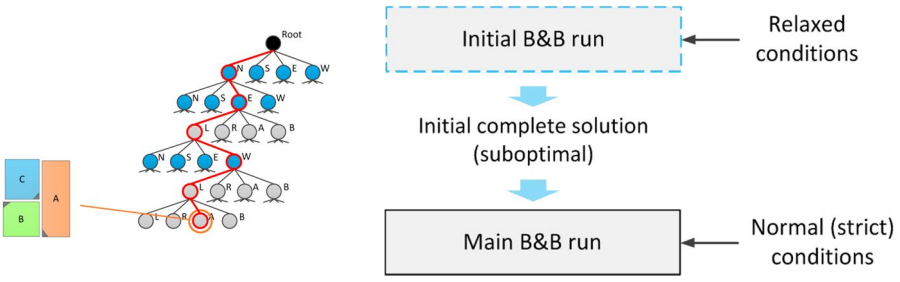
- Combined metric: size & number of interconnects
- Greedy graph-based algorithm



https://www.ifte.de/mitarbeiter/lienig/ASP_DAC18.pdf

Advanced Pruning Techniques: Initial Complete Solution

An initial solution (of good quality) helps with search efficiency



➢ Speed-ups of up to x50

https://www.ifte.de/mitarbeiter/lienig/ASP_DAC18.pdf

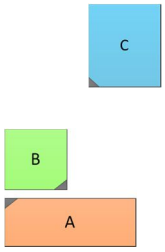
S. Osmolovskyi, J. Knechtel, I.L. Markov, J. Lienig "Optimal Die Placement for Interposer-Based 3D ICs," Proc. of the 23rd Asia and South Pacific Design Autom. Conf. (ASP-DAC 2018), pp. 513-520, Jan. 2018

Advanced Pruning Techniques: Forward Wirelength Checking

Before data allocation in tree, look ahead whether new node can become unpromising

Consider new die C

Estimated augmentations for rotations:
East? >= 40
West? >= 120
North? >= 140
South? >= 80



Estimated augmentations for topologies:
Die C is left of Die A? >= 70
Die C is above Die B? >= 200
...

- Predict the minimal WL augmentation incurred by new node in any case; ignore unpromising branches

https://www.ifte.de/mitarbeiter/lienig/ASP_DAC18.pdf

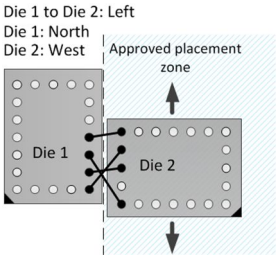
Advanced Pruning Techniques: Forward Wirelength Checking

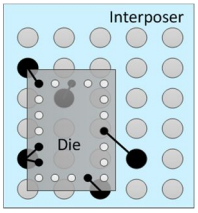
Topological nodes:

- Place two dies optimally "back-to-back" in all possible variations (rotations included)
- Calculate minimal WL of nets between the two dies

Rotational nodes:

- Align die (sitting alone) optimally to the interposer terminals
- Calculate minimal WL towards the terminals





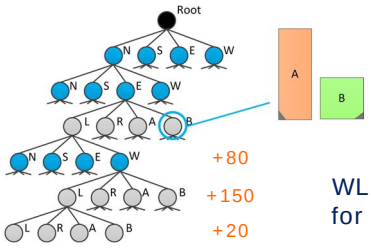
https://www.ifte.de/mitarbeiter/lienig/ASP_DAC18.pdf

S. Osmolovskyi, J. Knechtel, I.L. Markov, J. Lienig "Optimal Die Placement for Interposer-Based 3D ICs," Proc. of the 23rd Asia and South Pacific Design Autom. Conf. (ASP-DAC 2018), pp. 513-520, Jan. 2018

Advanced Pruning Techniques: Remaining Distances

Estimate how dies yet unassigned will impact wirelength

- We use data from previous techniques (Forward Checking)
- Consider minimal WL augmentations across all remaining levels in the search tree



Partial placement

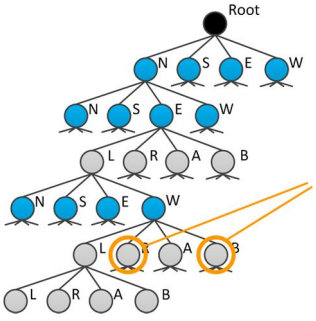
WL increases >= 250 for dies which are not assigned yet

➢ Better estimation of WL lower bound for partial placements

https://www.ifte.de/mitarbeiter/lienig/ASP_DAC18.pdf

Advanced Pruning Techniques: Dominated Configurations

Discard placements which appear much worse than others at the same level in the search tree



Is partial placement much worse than other ones?

Criteria: difference between WL estimations in same level >

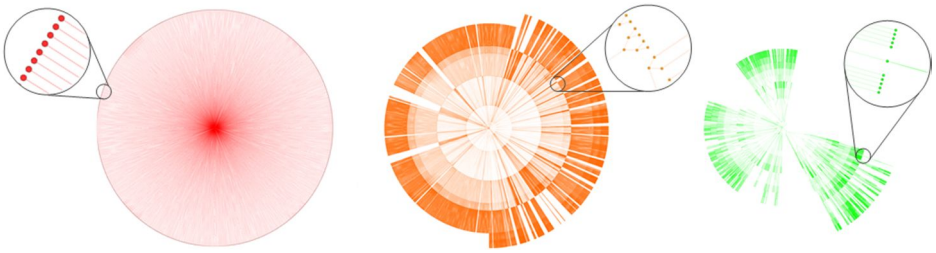
$$\frac{1}{dies\ number\ +\ 1} \times best\ TWL$$

Example: for 2 dies, difference has to be larger than 33% of the currently best total WL

https://www.ifte.de/mitarbeiter/lienig/ASP_DAC18.pdf

S. Osmolovskyi, J. Knechtel, I.L. Markov, J. Lienig "Optimal Die Placement for Interposer-Based 3D ICs," Proc. of the 23rd Asia and South Pacific Design Autom. Conf. (ASP-DAC 2018), pp. 513-520, Jan. 2018

Advanced Pruning Techniques: Key Result



Brute Force	Native Branch & Bound	Advanced B & B
~$4{,}4 \cdot 10^{12}$ nodes	263 million nodes	350 thousand nodes
~43 days	~10 min	~0.25 sec

- Speedup and scalability
- Up to 11 dies can be placed optimally with reasonable efforts

https://www.ifte.de/mitarbeiter/lienig/ASP_DAC18.pdf

Part 4

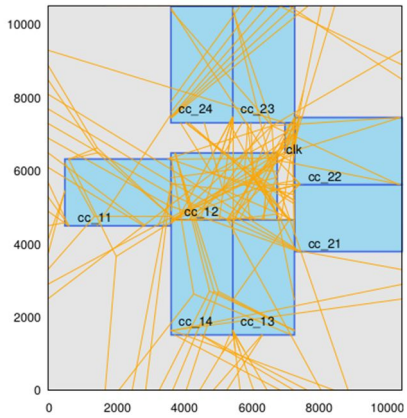
Results

https://www.ifte.de/mitarbeiter/lienig/ASP_DAC18.pdf

S. Osmolovskyi, J. Knechtel, I.L. Markov, J. Lienig "Optimal Die Placement for Interposer-Based 3D ICs," Proc. of the 23rd Asia and South Pacific Design Autom. Conf. (ASP-DAC 2018), pp. 513-520, Jan. 2018

Results

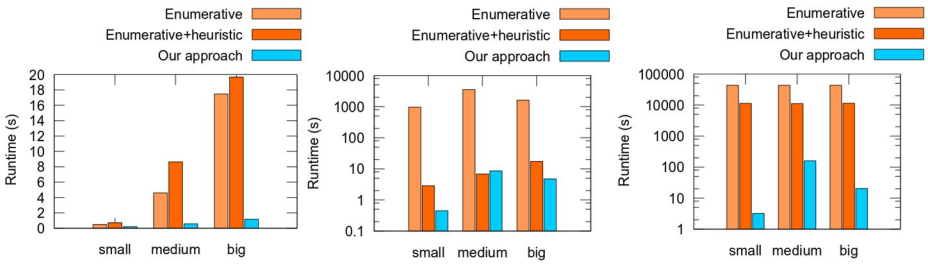
Layout example for MCNC benchmark apte



https://www.ifte.de/mitarbeiter/lienig/ASP_DAC18.pdf

Results

Comparison for runtime with optimal interposer placement [Liu14] on modified ISPD08 benchmarks



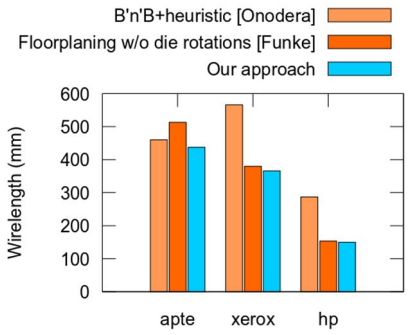
4 dies	6 dies	8 dies
Average speed-up:	Average speed-up:	Average speed-up:
x8.48/x11.8	x960/x3.58	x3756/x1380

https://www.ifte.de/mitarbeiter/lienig/ASP_DAC18.pdf

S. Osmolovskyi, J. Knechtel, I.L. Markov, J. Lienig "Optimal Die Placement for Interposer-Based 3D ICs," Proc. of the 23rd Asia and South Pacific Design Autom. Conf. (ASP-DAC 2018), pp. 513-520, Jan. 2018

Results

Comparison for wirelength with (sub-)optimal floorplaning [Onodera93, Funke16]



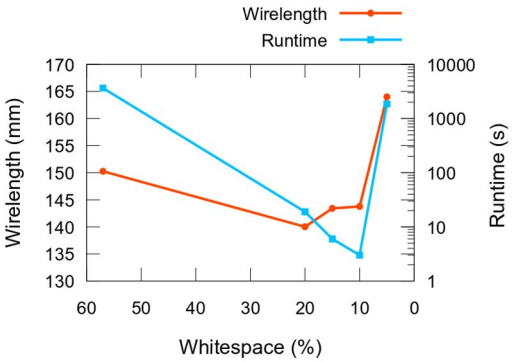
- We report the best WL values for MCNC benchmarks

https://www.ifte.de/mitarbeiter/lienig/ASP_DAC18.pdf

Results

Trends for practical benchmarks with less whitespace

hp benchmark as an example



- Better wirelength and runtime until some point; then placement becomes very constrained and challenging

https://www.ifte.de/mitarbeiter/lienig/ASP_DAC18.pdf

S. Osmolovskyi, J. Knechtel, I.L. Markov, J. Lienig "Optimal Die Placement for Interposer-Based 3D ICs," Proc. of the 23rd Asia and South Pacific Design Autom. Conf. (ASP-DAC 2018), pp. 513-520, Jan. 2018

Summary

- Branch-and-bound flow with advanced pruning techniques for optimal die placement on interposer
- We can optimally place up to 11 dies; prior art only 6 dies
- We consider die rotations and optimize dies within whitespace
- Ours is faster than other optimal methods and reports best WL result for classical MCNC benchmarks
- Binary of tool is publicly available, supports parallel execution: http://www.ifte.de/english/research/interposer-design

Thank you!

https://www.ifte.de/mitarbeiter/lienig/ASP_DAC18.pdf

S. Osmolovskyi, J. Knechtel, I.L. Markov, J. Lienig "Optimal Die Placement for Interposer-Based 3D ICs," Proc. of the 23rd Asia and South Pacific Design Autom. Conf. (ASP-DAC 2018), pp. 513-520, Jan. 2018