The Effect of Copper Trace Routing on the Drop Test Reliability of BGA Modules

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Abstract

The JEDEC drop test has become a popular method for the assessment of the dynamic mechanical reliability of 2nd level assemblies. It delivers repeatable results and is thus well suited for the development of a virtual lifetime model based on FEM simulations.

Detailed experimental studies showed PCB copper trace fractures as the dominating failure mode. The virtual risk assessment applied a two steps approach (sub-modeling technique). The overall PCB motion was computed by a global model of the entire JEDEC board. In the second step, the copper trace load was investigated with a single component. The resultant plastic strain showed a clear dependency on the relation between copper trace routing and dominating PCB deformation. A strain map was derived which indicates the strain level as a pre-factor to each trace routing condition.

The validity of the strain map concept was proven by comparison with experimental results. The strain map was able to precisely identify the failing interconnections at each component position. The combination of interconnection strain energy from the global model and the strain map was able to match the experimental sequence of failures across the JEDEC board exactly. A lifetime model was derived which is able to predict the cycles-to-failure of three different package types with less than 25% deviation to the tests. Hence, this lifetime model sets the ground for virtual prototyping that also includes the BGA drop test endurance.

Introduction

Virtual prototyping is capable of massively reducing time to market for new products without any reduction in case studies or robustness investigations. Based on precise numerical simulation instead of experimental tests, the design decisions can finally be made likewise safe but in a fraction of time. Of course, development and verification of the parametric numerical models requires extensive experimental work and a very close interaction between tests and simulation. Otherwise, no sufficient prediction accuracy will be achieved.

So far, lifetime models allowing trustworthy virtual prototyping have been created for thermal cycle tests. This work contributes to the deduction of such a model for mechanical drops of microelectronics components on a PCB (2nd level structures). The development is based on the JEDEC drop test [1], whose biggest advantage is its high failure reproducibility. This way, characteristic cycles-to-failure results can reliably be obtained for each of the 15 components on the well defined JEDEC board. The sequence, at which the components fail during repetitive drops, is used to select the proper failure criterion and to evaluate the simulation methodology. At this stage, the accuracy target has been set to ±50% for the predicted cycles-to-failure.

The next sections describe the experimental setup and the failure analysis followed by the details of the simulation study. Finally, the accuracy of the lifetime model is evaluated by comparing the predicted and the experimental cycles-to-failure results of three different packages.

Experimental setup

JEDEC standard JESD22-B111 [1] precisely specifies the experimental setup, the specimens, and the load condition of a drop test for 2nd level structures. The test setup consists of a base plate, two guiding rods, and a sledge (fig. 1). The base plate is covered with specific felt layers, which lead to quite well defined sinusoidal deceleration profiles in the sledge dropping onto it. The guiding rods assure constant impact angles and, hence, constant acceleration profiles in the specimen mounted on top of the sledge. In this study, JEDEC drop condition B was used, i.e., the 0.5 ms sinusoidal pulse had a peak acceleration of 1500 G on top of the sledge. The pulse was continuously measured proofing its repeatability during all tests. This pulse led to failures after some 10 to a few 100 drops depending on the support configuration chosen and the packages investigated. Two support configurations have been applied in this study, the fixation by 4-screws (one screw at each edge of the JEDEC PCB) as defined by the standard and a 6-screws configuration with additional clamping at the middle of both long PCB edges (fig. 2). The clamping conditions determine the eigenmodes and the eigenfrequencies of the PCB and, hence, the local acceleration fields, which generate the specific mechanical load at each component position.

Modal analyses done by ANSYS showed the first eigenfrequency at about 180 Hz in 4-screws configuration and at about 390 Hz in 6-screws configuration. The displacement shape also changed between the two clamping configurations causing different stress distributions and different sequences of failure occurrence among the 15 components on the JEDEC board.

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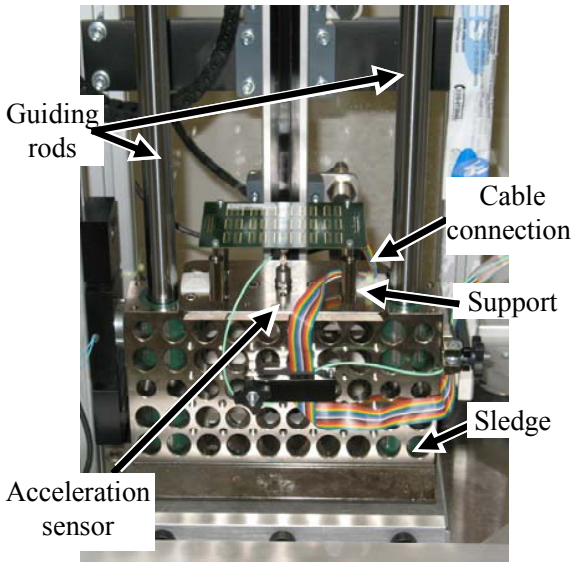


Figure 1: Drop Test setup with guiding rods, base plate, sledge, Jedec PCB, in situ resistance measurement and acceleration sensor

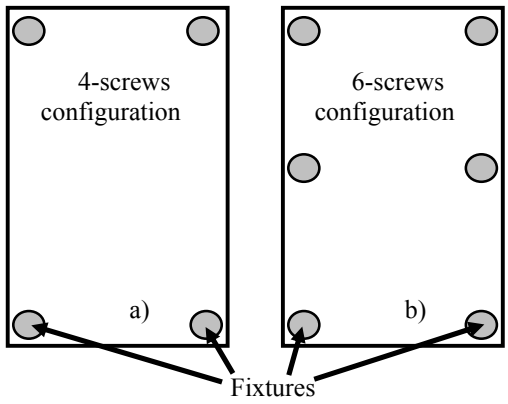


Figure 2: Boundary conditions of the JEDEC board: a) 4-screws configuration according to JEDEC standard; b) 6-screws configuration

Failure detection was done by in-situ resistance measurements of 15 daisy chains (one per component) continuously throughout the test. The failure flag is set when the event detector captured 1 kΩ or more in three consecutive drop cycles.

The investigations included three different packages. Table 1 lists their geometrical data. The solder joints were made of SnAg1Cu0.5. The copper pads of the components had electro-less nickel/gold finish, whilst PCB pads were covered with Cu-OSP.

Experimental results and discussion

During soldering, brittle intermetallic compounds including Cu_6Sn_5 or $(Ni, Cu)_3Sn_4$ are formed at the interfaces to either pads. Lead-free solders have higher Young's modulus than the lead containing alloys and show a strong dynamic hardening effect. This is why the brittle IMC cracks have been expected to be the dominating failure mode during drop testing [2 - 6].

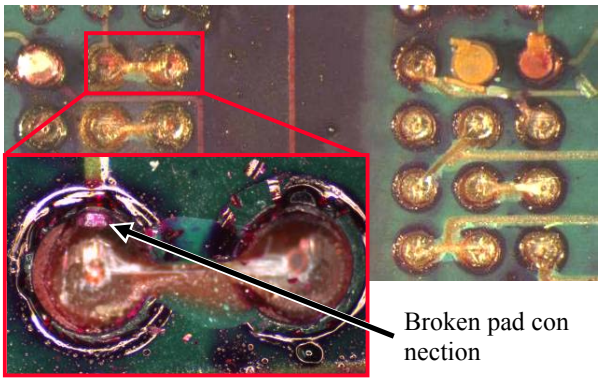


Figure 3: Failure analysis of a JEDEC board with TFBGA-60 packages tested in condition B with 6-screws fixture at component position #8 (see fig. 4b)

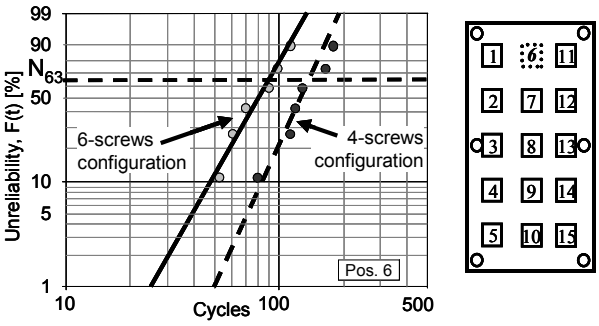
Surprisingly, the industrial drop experiments showed no failure caused by IMC cracks. Instead, dye and pry tests revealed the electrical opens to be caused by broken copper traces connected to lifted PCB pads.

Figure 3 shows a result of an experiment in JEDEC condition B with 6-screws clamping. The figure depicts lifted PCB pads and a broken pad connection at the upper edge of the ball-out (TFBGA-60 package, tab. 1). Clearly, this has caused the electrical failure and, hence, may be used as failure trigger in the lifetime model. However, the PCB pad lifts do not appear at all interconnections. Some IMC crack initiations and strongly colored component pads are also found.

The analysis of all failure sites shows the copper traces to fracture only when being aligned parallel to the short edge of the JEDEC PCB, i.e., when following the direction of highest PCB deformation. Copper trace with any other routing direction did not fail even after 500 drop cycles. On the other hand, it has been found that electrical failure can happen at any outer interconnection if its copper trace is routed in the critical direction. Obviously, the trace direction contributes to the conditions of failure occurrence quite heavily. Hence, it

Table 1: Geometrical properties of the investigated daisy-chain packages

Label	VFBGA-90	VFBGA-60	TFBGA-60
Height [mm]	0.8	0.8	1.2
Package area [mm]	12.5 x 9.5	10.0 x 9.5	10.5 x 8.0
Number of Balls	90	60	60
Ball-out size [mm]	11.2 x 6.4	7.2 x 6.4	8.0 x 6.4
Ball arrangement	15 x 6, full rows	10 x 6, full rows	11 x 6, partly populated



a) b)

Figure 4: a) Weibull plots of experimental cycles-to-failure of package TFBGA-60 at component position #6 in 4-screws and 6-screws configuration; b) Component positions

shall not be neglected in lifetime modeling as it usually would be done when IMC cracks are seen as dominant mode.

The components on the JEDEC board show a characteristic sequence of failure. This sequence was seen as a good parameter for a first accuracy assessment of the predictive simulation results. Consequently, the experimental cycles-to-failure were recorded separately for each component position. A minimum of six boards were tested until at least three components failed.

Weibull plots of the component failures at position #6 are shown in figure 4 for both kinds of tests. At this particular position, the 6-screws condition is more critical than the 4-screws fixation. The characteristic numbers of cycles-to-failure, N_{63}, are 69 cycles and 175 cycles, respectively. Despite the difference in magnitude, the slopes of the Weibull curves are almost identical. This indicates the failure mechanisms being very much the same in both tests.

Table 2 lists the N_{63} results of all investigated packages under 6-screws boundary condition and the corresponding sequence of failure. The component at the center position #8 (fig. 4b) always fails first. Moreover, the critical component positions are all situated in the middle row of the JEDEC board. This is caused by the 6-screws configuration, in which the PCB can only bend along its width, leading to high mechanical stress at the component positions 6 – 10. Differences among the tests occur with respect to the packages size. The VFBGA-90 fails earlier and shows a higher number of critical component positions than the 60 pin packages because it is bigger (tab. 1). Similarly, the slightly larger ball-out dimensions of the TFBGA-60 are responsible for its somewhat lower number of cycles to failure as compared to the VFBGA-60.

In case of the 4-screws fixture, a different failure sequence can be seen since the PCB is able to deform in both, length and width, directions. Therefore, the middle row is less critical while more stress is induced at the diagonal component positions 2, 4, 12 and 14.

Global FEM model for JEDEC drop test simulations

Within this study, the FEM simulations have focused on the 6-screws configuration. They were performed with the commercial code LS-Dyna™, which applies an explicit time integration scheme that is well suited for highly dynamic applications with large plastic deformations.

Table 2: Characteristic number of cycles to failure, N_{63}, and failure sequence of the most critical component positions for all 3 package types tested in 6-screws configuration

Package type	VFBGA 60	VFBGA 90	TFBGA 60
Comp 06	-	89 (4)	-
Comp 07	291 (3)	94 (5)	161 (3)
Comp 08	90 (1)	43 (1)	68 (1)
Comp 09	141 (2)	58 (2)	113 (2)
Comp 10	-	70 (3)	-

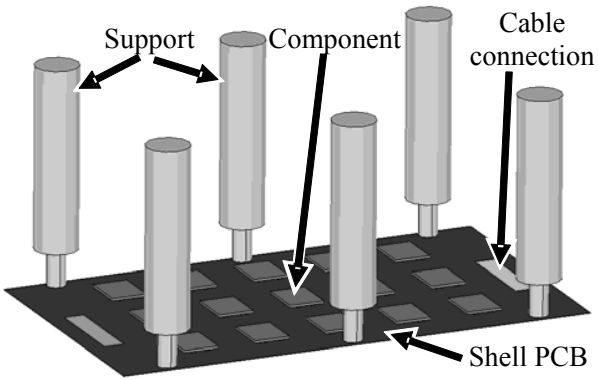


Figure 5: FEM global model of the JEDEC drop test

The global model is a complete representation of the JEDEC board with all 15 components and the supports columns (fig. 5). The PCB is modeled by shell elements, and applies LS-Dyna's material model #117 (*MAT_COMPOSITE_MATRIX) [7], which provides for the direct input of the PCB laminate matrix [8, 9]. This way, the tensile and bending properties of the PCB are captured adequately. Dependent on the laminate stack, they can be very different. In any case, they both determine the PCB motion and, hence, the stress induced into the component.

Extended efforts have been made to match the board vibration behavior realistically. Several acceleration profiles have been measured experimentally at different PCB positions, which were used for a sufficiently detailed FEM model of the JEDEC setup. Beyond the complete modeling of the PCB in order to eliminate the cut of eigenmodes and eigenfrequencies, sections of plated through hole (PTH) via arrays are included at both short edges of the board. These via arrays are used for the cable connection, which are required by the in-situ resistance measurement system. As mentioned in [10], the cables do not change the vibration frequency but they have a strong damping effect on the PCB region next to a connected via array. This behavior creates an unsymmetrical PCB motion slightly shifting the mechanical stress distri-

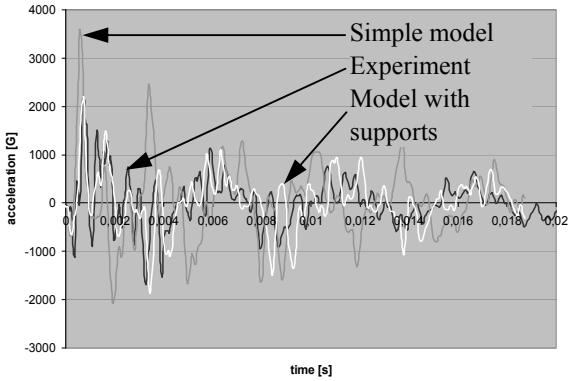


Figure 6: Comparison between experimental PCB vibration behavior and results of different simulation methodologies

bution at all component position. Based on this observation, the damping coefficients of the two via arrays have been adjusted to match the experimental vibration behavior.

Boundary conditions and load initiation need to be modeled precisely, too. The FE model is excited by an acceleration profile that was recorded during experiments on top of the sledge. This profile is applied to the constraint points of the model. In the simplest case, these points are directly placed at the mounting holes in the PCB. However, the PCB acceleration results achieved this way differ very much from the curves measured in the experiments. The computed peak acceleration value and the first eigenfrequency are higher than the measured values indicating the numerical model to behave too stiff. An adjustment of the PCB material properties is not the right way to counteract this problem. Only 10% of its original stiffness would have left, which is not realistic.

Another possibility to reduce the drop system stiffness can be achieved by shifting the constraint points to the bottom of the support legs. They are made of steel and consist of two sections. The bigger bottom part is 50 mm tall and has a diameter of 12 mm. The top tip is 10 mm high with 5 mm in diameter. These supports are modeled by solid elements that are attached to the PCB via contact definitions. As shown in figure 6, the support legs can effectively soften the PCB response. Now, the simulation model can follow the experimental acceleration curve very closely over a wide time span. The remaining root-mean-square difference between measured and simulated acceleration profiles is 70% lower as compared to the results of the simple model. Obviously, the support legs are not perfectly rigid. They contribute significantly to the deformation behavior of the JEDEC PCB.

The components have been modeled in a rather simple way. They have a hexahedral body with the outline of the according package and coarse 3-D solder balls that are arranged according to the specific package, see figure 7. The component body has effective elastic properties similar to those of mold compound. The solder balls have been modeled as simple cubes divided into 8 elements of equal size. The solder joints at the outer rows have been modeled in a more realistic barrel shape. These models closely replicate the experimental joint dimensions at both pads and at its equator level. The barrel joints are meshed by 24 elements, which still lead to a coarse mesh. The quality of this mesh however, seems to be sufficient for the first lifetime modeling step, which is attempted with this global model. The solder balls use a material model with strain-rate dependent hardening. The rate dependent data for this model from [11] is compiled in table 3. The solder balls are directly attached to the component body at one side, see fig. 7. At the other end the joints are connected to the Shell PCB via offset contacts.

Table 3: Strain-rate hardening effect of the solder material model

Strain -rate [1/s]	10^{-4}	10^{-3}	10^{-1}	10^{0}	10^{1}	10^{2}	10^{3}
Yield stress [MPa]	40	45	58	67	75	88	105

A solid basis was set with the material models and the simulation methodology at hand. This basis was applied for detailed stress analysis from component down to interconnection level.

Sub-model description

Sub-modeling is a typical feature of many simulation codes. Detailed stress analysis can be executed with this technique by supplementing the global mesh by a fine mesh at an interesting subsection. Failure analysis of experimental samples has identified the copper traces to be the most critical parts of the 2nd level interconnect system. In the global model covering the entire JEDEC board, these individual traces are not included explicitly.

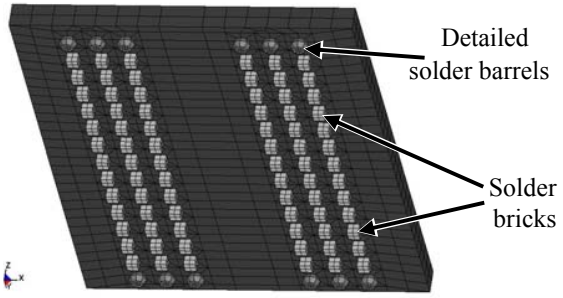


Figure 7: VFBGA-90 component of the global drop test model

The sub-model covers only one package. Therefore, all mechanically relevant parts can be considered as shown in figure 8. The component body consists of the substrate, the die attach film, the die, and the mold compound. The joints are modeled by the substrate pads, the solder ball, the PCB pads and the PCB copper traces. The solder resist leaves the PCB pad and a little bit of its trace uncovered since PCB side has a non-solder-mask defined configuration. The copper

traces may approach the PCB pad in any 45° direction, as depicted in figure 9. So, all routing options can be considered.

Again, die PCB is meshed by shell elements while all other parts of the sub-model are meshed by 3-D solid elements. The PCB solder mask and the bottom of PCB copper are connected to the PCB by offset contacts. The PCB model has about twice the length and the width of a package. This configuration allows the vibration to be modeled realistically with no critical mechanical parts being affected by model edge effects. According to the stress situation, the outermost solder balls have fine meshes while a more coarse mesh suffices for the inner joints.

The material models of the component parts are linear elastic. No large deformation is expected in these parts and no or negligible non-linear deformation. Similar to the global model, the direct laminate matrix is applied to the PCB shell elements. The solder material uses a strain-rate dependent bilinear elastic-plastic model with the hardening behavior as listed in tab. 3. The copper traces and pads account for isotropic hardening [7] by the power law coefficients provided by [12]. This set of material models has been found adequate for the investigation underway.

The copper trace strain map

A detailed stress analysis of the copper traces has been conducted applying the sub-model technique as described above. Because of its distinct failure distribution, the TFBGA-60 component was chosen for this investigation. The sub-model was set at the central position #8, as shown in figure 10. The global boundary condition applied the 6-screws configuration. Eight sub-models with changing copper trace routings at each of the outermost pads have been simulated using these conditions.

Different result criteria may be applied for assessing the copper trace stress. According to earlier work [10], the plastic strain accumulated in the copper trace between pad and solder mask was chosen. The simulation results show the maximum strain to appear at the edge of the solder ball.

The effect of the copper trace routing direction on the accumulated plastic strain at the joints A1 and L1 are shown in figure 11. The two strain curves are very similar – just offset by 180°. The highest plastic strain is created in the copper traces at the joints A1 and L1 positions when in 0° and 180° orientation, respectively. This fits to the experimental observation of the traces to fail most easily when routed parallel to the PCB width. The plastic strain declines the more the farther the traces are routed differently. It even sinks below 75% of the maximum magnitude when the trace is 60° or more off the critical orientation. The minimum strain is reached when the trace points towards the component center. Again, this fits to the observation of dramatically less risk of failure at most of the trace orientations. The slight difference in plastic strain magnitudes between A1 and L1 is the effect of missing K1 due to which the joints at position L1 is stressed more.

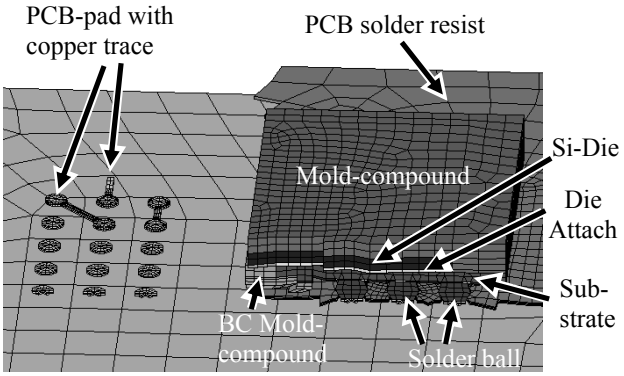


Figure 8: X-section through a TFBGA-60 sub-model with its characteristic features

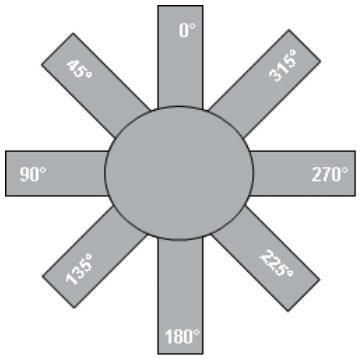


Figure 9: Copper trace orientations at the sub-model copper pads for the investigation of the routing effects

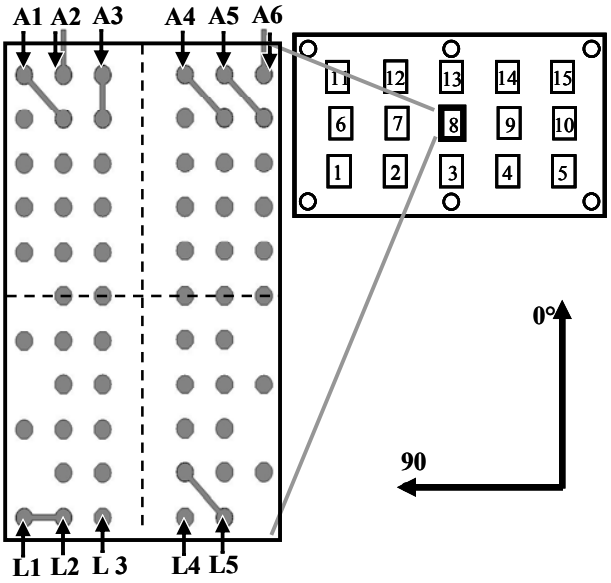


Figure 10: Component orientation and initial pad design at position #8

This investigation reveals that the copper traces at A1 and L1 positions of the real samples have a quite safe orientation.

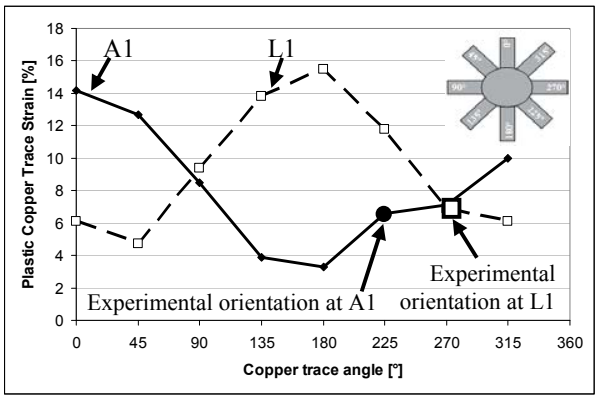


Figure 11: Routing dependent plastic strain of the copper trace at contact interconnection A1 and L1

They are only exposed to 46% and 44% of the maximum possible strain level, respectively.

Result evaluation at all of the outermost interconnections shows a trend of the copper trace routing effect. The relative stress distribution is similar at all component edges, which reduces the problem to one quarter of the complete ball-out. Within this symmetry condition, interconnections can be arranged into 2 groups with both outermost interconnections forming one group (e.g. A1 & A2) and the interconnection at the bond-channel as the second group (A3). The relative strain distribution S_α is simply calculated by setting the plastic strain at any trace orientation ε_α in relation to the according maximum plastic strain ε_{max} at this interconnection (1).

$$S_\alpha = \frac{\varepsilon_\alpha}{\varepsilon_{\max}} \qquad (1)$$

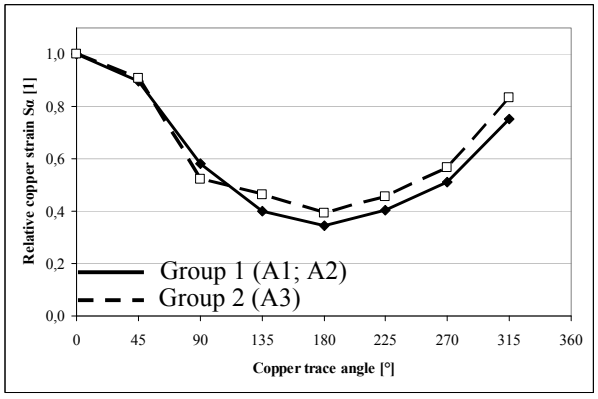


Figure 12: Copper trace routing effect on the relative strain distribution

The strain distributions depicted in figure 12 show slight differences of the routing effect. The differences, however, are less than 5% and thus negligible small. This way the routing effect at all interconnections of a package quarter can be combined into a single group. This routing effect is applicable to all other component edges as well. The distribution of interconnections A4 to A6 can be obtained applying a symmetrical reflection around the 0°-orientation. The corresponding distributions of row 'L' is than obtained by offsetting the curve by 180°.

The considerations presented above result in a strain map which is applicable to similar packages, failing with broken copper traces, see figure 13. The figure shows the strain distribution at the package edges of a single component. This strain map can be applied to all component positions of the middle row on the JEDEC board as well, since the relative strain distribution is similar at these positions under 6-screws boundary condition. The copper trace routing effect will be considered with the pre-factor S_α, which comes in addition to the interconnection stress calculated by the global model.

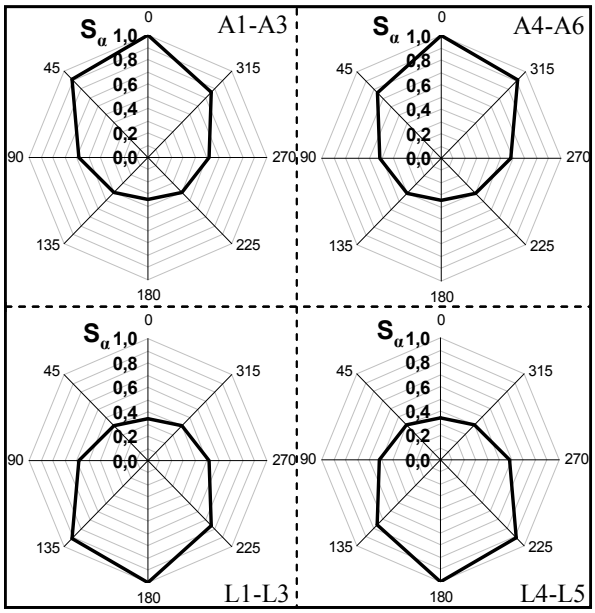


Figure 13: Strain map for copper traces attached to interconnections of middle row components (#6 – #10) in 6-screws boundary condition

Global result criteria application on the experimental failure arrangement

A lifetime model for drop tests can only be applied in practical life, if it has the ability to identify high stress components on the entire shock assembly. Global simulations are necessary for this purpose and a global failure criterion is required that works in addition to the copper trace routing effect. This simulation criterion can be assessed by the experimental failure sequence on the JEDEC board, see table 2.

Numerous publications suggest different FEM simulation criteria. The adequate criterion can quantify the effects triggering the experimental failure mode. This limitation reduces the amount of possible criteria to those which can quantify the individual interconnection stress. Result criteria can be grouped into the class of continuum mechanics and fracture mechanics criteria, respectively. Fracture mechanics criteria are e.g. the stress intensity factor, the energy release rate or Griffith's energy relation. This group of criteria, however, would require a simultaneous handling of 120 different crack positions with very fine meshes. The computational resources

required here would be excessively large. Therefore, this study focuses on continuum mechanics criteria.

Potential continuum mechanics criteria include the plastic strain in a solder ball, ε_p, [13-16], the plastic strain rate, $\dot{\varepsilon}_{pl}$, [17-19], the resultant force at the solder ball PCB interface, F, [20], the first principal stress, σ_1, [14, 21, 22], the van-Mises-stress, σ_{EQV}, [23], and mechanical energy, W, [20, 24, 25]. The evaluation of these criteria was presented in [10]. It turned out that none of the existing criteria was able to cover the whole sequence of failure on the JEDEC board. Only the new energy criterion SEND, equation (2)

$$SEND = \int \dot{\varepsilon}_{pl} \cdot \sigma_{Pad} dt \qquad (2),$$

which is a combination of the plastic strain rate and PCB-pad stress, was able to predict the failure arrangement most precisely. Still, the results could not be gained in general. The energy values taken into account were extracted at each package from critical interconnections, with disadvantageous copper trace orientation, only. The overall results suggested other interconnections to fail earlier, but they were linked to good-natured trace orientations and thus not considered during result evaluation.

The combination of the basic failure criterion $SEND_{bas}$, eq. (2), and the sub-model strain map S_α should be able to overcome these limitations and deliver a generally applicable lifetime model, equation (3)

$$SEND_{corr} = S_\alpha \cdot SEND_{bas} \qquad (3).$$

Again the TFBGA-60 component was chosen due to its copper trace routing, see fig. 10. The outcome for both criteria is condensed in table 4.

Table 4: Corrected and uncorrected values of SEND at critical interconnections of a TFBGA-60 package at board position #8

Interconnection (fig. 10)	$SEND_{bas}$ [mJ/mm^3] eq. (2)	$SEND_{corr}$ [mJ/mm^3] (S_α) eq. (3)	Experimental failure analysis
A1	26.6	10.6 (0.40)	Pass
A2	22.6	**22.6** (1.00)	**Fail**
A3	23.7	12.3 (0.52)	Pass
A4	23.9	11.0 (0.46)	Pass
A5	23.3	9.3 (0.40)	Pass
A6	28.4	**28.4** (1.00)	**Fail**
L1	36.7	18.7 (0.51)	Pass
L2	30.5	17.7 (0.58)	Pass
L5	42.3	16.9 (0.40)	Pass

Based on the uncorrected energy values of $SEND_{bas}$, failure should occur at interconnection row L. Highest energy was identified at position L5, which would be treated as the most critical interconnection triggering the components failure. The pre-factors S_α of the strain map, however, are able to outbalance these high interconnection energies and to highlight interconnections A2 and A6, which failed in experiments. The corrected or effective energies $SEND_{corr}$ at other interconnections, especially row L, are much lower due to their good-natured copper trace orientations.

Similar observations can be made at other component positions and for other package types. With the stress-map and the energy criterion $SEND_{corr}$ at hand, a more robust lifetime model is available, which can be applied, if copper trace crack is the dominating failure mode.

A lifetime model for JEDEC drop tests

The combination of $SEND_{bas}$ and the strain map was applied to all of the components listed in tab.1 with experimental cycles-to-failure given in tab.2. Simulations were executed with the global model only, since the strain map should not alter dramatically due to constant boundary conditions of the JEDEC board. Typically an inverse power law, equ.4, is the basis for such kind of lifetime models.

$$N_{63} = C_1 / \left(S_\alpha \cdot SEND_{bas}\right)^{C_2} \qquad (4)$$

The pre-factor C_1 and the exponent C_2 were determined by fitting the characteristic cycles-to-failure N_{63} from experiment and the according corrected simulation energy values. All available experimental and simulation data of the investigated packages were assembled for this purpose. The comparison of simulated cycles-to-failure and the characteristic N_{63}-values of the experiments is shown in figure 14.

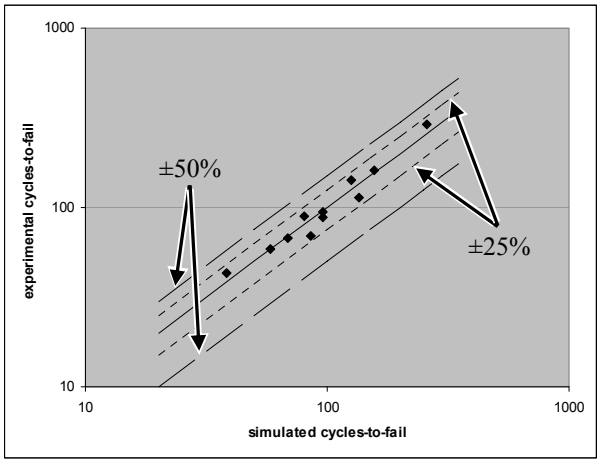


Figure 14: Comparison of simulated and experimental lifetimes

Both lifetime values are matching very close. The scatter between prediction and reality is less than ±25%, which is in the range of advanced lifetime models for temperature cycling. This result clearly satisfies the original target of ±50% scatter. When assessing each data point in detail, the difference of simulated prediction is completely within the experimental scatter. This result proves the sufficient accuracy of the combined criterion $SEND_{corr}$. This criterion is a robust way to assess the lifetime of 2nd-level assemblies under drop test conditions.

Conclusion

The paper presents the results of 2.5 years industrial methodology effort for the development of a virtual lifetime model for the JEDEC drop test. Detailed experimental studies were executed with three different memory components. These components were dominantly tested under JEDEC condition B with a PCB fixture at six points instead of four, see fig.2. At least six JEDEC boards assembled with one package type were tested under these conditions, in order to determine the characteristic number of cycles-to-failure at each component position for each of the packages.

The analysis of all failed components revealed copper trace cracks as the failure mode triggering the electrical cuts. This failure appeared only if the copper traces were routed along the direction of highest PCB deflection. This way, electrical failures did not always occur at the most stressed interconnections, which were typically located at the corners of the package. The failure position was defined by the PCB boundary condition and the copper trace routing at the PCB pads.

The new simulation methodology was validated by a comparison of simulated and experimentally measured acceleration profiles at different PCB positions. The validated motion of the global model was the input for a detailed sub-model investigation. The routing effect of the copper traces was proven by a stress analysis of different routing directions at the outermost interconnections of a package. Simulation results clearly highlighted those routing directions as most stressed, which always failed in the experiments. The outcome of this analysis was a strain map, which ranks the routing directions according to their stress potential.

Finally the global lifetime assessment was done using a combination of the sub-model strain map S_α and the global energy criterion $SEND_{bas}$ [10]. The combination of both criteria ($SEND_{corr}$) was able to correctly identify the failed interconnections at each package type and position, respectively. With this information the experimental sequence of failing component positions on the JEDEC board were followed correctly by the simulations. Furthermore a lifetime model was derived, which has the ability to predict the experimental number of cycles-to-failure for the investigated packages with an inaccuracy of less than ±25%. This accuracy is lower than experimental scatter and is beyond the original target.

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