The Pressing Need for Electromigration-Aware Physical Design

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ABSTRACT

Electromigration (EM) is becoming a progressively intractable design challenge due to increased interconnect current densities. It has changed from something designers "should" think about to something they "must" think about, i.e., it is now a definite requirement. The on-going IC-down-scaling is producing physical designs with ever-smaller feature sizes, which can easily lead to current densities that exceed their maximum allowable values. This invited talk introduces the fundamentals of EM, its interactions with thermal and stress migration, and presents appropriate modelling and simulation methodologies. Following a summary of EM-inhibiting effects in physical design, we propose ways of facilitating EM-compliant layout design in future technology nodes.

CCS CONCEPTS

• **Hardware → Physical verification** • **Hardware → Electronic design automation** → Methodologies for EDA

KEYWORDS

Electromigration; current density; layout; interconnect reliability; short-line rules; short-length effects; Blech length; reservoir effect

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1. INTRODUCTION

Excessive current density within interconnects – which if not effectively curtailed causes electromigration (EM) – is a growing reliability issue in modern integrated circuits (ICs) as a result of smaller feature sizes. Accordingly, the latest edition of the ITRS roadmap [1] indicates that all of today's minimum-sized interconnects are EM-affected (Fig. 1).

The trends towards smaller line widths and smaller cross-sectional areas will continue over the coming years (Table 1). These trends will be accompanied initially by a reduction in currents (Fig. 1, left and Table 1) due to lower supply voltages and shrinking gate capacitances. Given that current reduction is constrained by rising frequencies and will even be reversed beyond 2022, we witness an alarming trend towards increased current densities $\mathcal{J}$ in ICs going forward (Fig. 1, right and Table 1, bottom).

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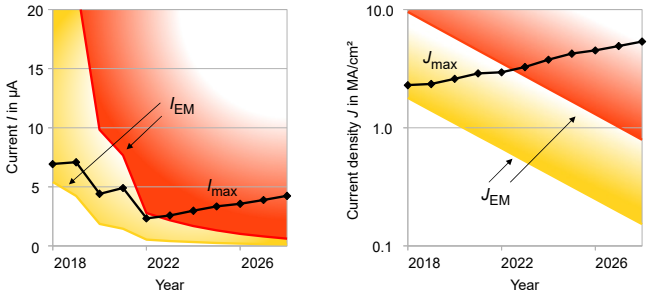

Figure 1: Projected development of currents (I_{max}, left) and current densities (J_{max}, right) needed for driving four inverter gates, according to ITRS [1,2] and Table 1. EM degradation must be considered inside the yellow areas for currents (I_{EM}) and current densities (J_{EM}). As of now, there are no known manufacturable solutions for the red areas.

Table 1: Predicted technology parameters based on the ITRS, 2015 edition [1]; maximum currents and current densities for copper at 105°C.

Year	2018	2020	2022	2024	2026	2028
Gate length (nm)	12.8	10.65	8.87	7.39	6.16	5.13
On-chip local clock frequency (GHz)***	6.69	7.24	7.83	8.47	9.16	9.91
DC equivalent maximum current (µA)*	6.92	4.41	2.33	2.98	3.56	4.24
Metal 1 properties						
Width – half-pitch (nm)	12	9	6	6	6	6
Aspect ratio	2.1	2.1	2.2	2.2	2.2	2.2
Layer thickness (nm)*	25.2	18.9	13.2	13.2	13.2	13.2
Cross-sectional area (nm²)*	302.4	170.1	79.2	79.2	79.2	79.2
DC equivalent current densities (MA/cm²)						
Maximum tolerable current density (w/o EM degradation)**	1.8	1.1	0.7	0.4	0.3	0.2
Maximum current density (beyond no known solutions)**	9.5	5.8	3.5	2.1	1.3	0.8
Required current density for driving four inverter gates***	2.29	2.59	2.94	3.76	4.50	5.35

*) Calculated values, based on given width W, aspect ratio A/R, and current density $\mathcal{J}$ in [1], calculated as follows: layer thickness $T = A/R \times W$, cross-sectional area $A = W \times T$ and current $I = \mathcal{J} \times A$.
**) Approximated values from the ITRS 2015 figure INTC6 [1].
***) Values from the ITRS 2013 edition [2].
All remaining values are from the ITRS 2015 edition [1].

Due to smaller structure sizes, maximum tolerable current densities are shrinking, as well – giving further cause for concern. (Small voids and other material defects, which would have been tolerated in earlier technology nodes, increasingly cause dramatic damage to, or resistance change in, wires with shrinking metal structures.) Thus, the ITRS [1] states that all minimum-sized interconnects are EM-affected by 2018 (Fig. 1, yellow barrier).

Furthermore, the total length of interconnects per IC will continue to increase. As a consequence, reliability requirements per unit length of wire need to be *increased* in order to *maintain* overall IC reliability. But, as noted above, this accepted wisdom is set to be compromised by the prospective *drop* in interconnect reliability due to EM. And indeed, the ITRS states that no known solutions are available for the EM-related reliability requirements that we will face approximately 5 years from now (Fig. 1, red barrier).

Increased interconnect resistivity caused by scattering effects in small wires will raise further challenges [3]. Coupled with a rise in current densities, this will lead to large local temperature gradients inside the wire caused by Joule heating. This in turn will accelerate temperature-dependent EM and introduce additional thermal migration [4-5].

The tendency to replace SiO_2 with low-k dielectrics [1] with lower stiffness coefficients reduces the stress-induced atomic backflow [6] that counteracts EM in short lines. Another consequence of using low-k dielectrics is the increased likelihood of EM-induced compressive failures (extrusions) [7].

As already mentioned, the surge in current density is also driven by an increase in clock frequencies (Table 1), in response to the demand for enhanced performance and made possible by transistor miniaturization. Although higher frequencies will neither worsen nor improve EM issues in signal or clock nets [8], they will increase currents (and thus current densities) in (DC) supply nets, which are already sensitive to EM in state-of-the-art technologies.

As a consequence of these dramatic developments, any up-to-date physical design methodology must be EM-aware; how to achieve this is the subject of this paper. In Sect. 2, we introduce the physical EM process, followed by an outline of how EM interacts with thermal and stress migration (Sect. 3). Section 4 presents appropriate simulation approaches. Section 5 summarizes all known EM-inhibiting effects that can be exploited in physical design in order to reduce the negative impact of EM on circuit reliability. Section 6 sets out ways of facilitating EM-compliant layout design in the future.

2. ELECTROMIGRATION

Current flow through a conductor produces two forces to which the individual metal ions in the conductor are exposed. The first is an electrostatic force F_{field} caused by the electric field strength in the metallic interconnect. This force can be ignored in most cases, as the positive metal ions are shielded to some extent by the negative electrons in the conductor. The second force F_{wind} is produced by the momentum transfer between conduction electrons and metal ions in the crystal lattice. This force acts in the direction of current flow and is the main cause of EM (Fig. 2).

Hence, there is interaction between the moving electrons – a sort of "electron wind" – and the metal ions in the lattice structures. Atoms at the grain boundaries especially will be impacted by the electron wind, that is, they will be forced to move in the direction of the flow of electrons. Thus, in time, metal atoms will accumulate at individual grain boundaries, forming so-called "hillocks" in the direction of the current. At the same time, so-called "voids" can appear at grain boundaries (Fig. 3).

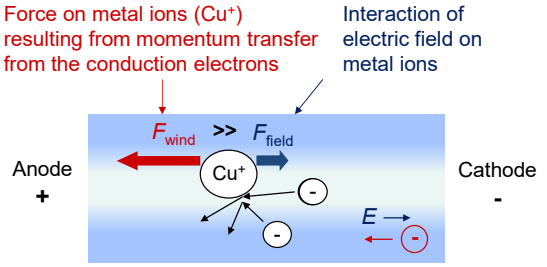

Figure 2: Two forces act on metal ions that make up the lattice of the interconnect material. EM is the result of the dominant force, that is, the momentum transfer from the electrons which move in the applied electric field.

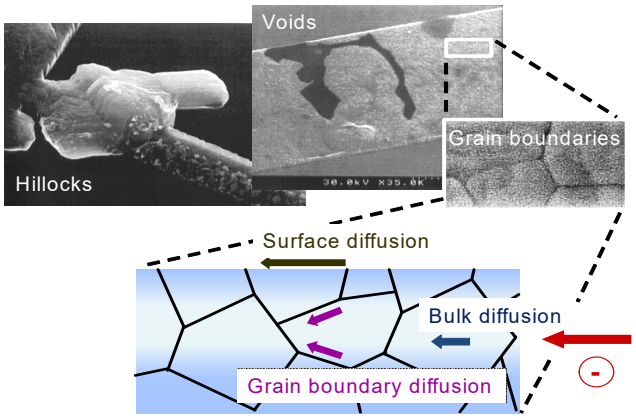

Figure 3: Hillock and void formations in wires due to EM, and illustration of various diffusion processes within the lattice (Photos courtesy of G. H. Bernstein und R. Frankovic, University of Notre Dame)

If the direction of an excessive current is constant over a longer period, these voids and hillocks appear in the wire. Analog circuits, or power supply lines in digital circuits, are therefore particularly susceptible to EM. In digital circuits, on the other hand, where the current direction varies with alternating capacitive charging and discharging in conductors, a certain amount of compensation occurs due to material backflow (self-healing effect). Nonetheless, interconnects can fail, with thermal migration playing a critical role.

There are three types of diffusion caused by EM: grain-boundary, bulk and surface diffusion (Fig. 3). In general, grain boundary diffusion is the main migration process in aluminum wires [9,10]; surface diffusion predominates in copper interconnects [11-13]. Detailed studies of the various EM failure mechanisms can be found in [10,11,14,15].

Many electronic interconnects in integrated circuits have a design median time to failure (MTF) of at least 10 years [16]. The failure of a single interconnect caused by EM can result in the failure of the entire circuit. At the end of the 1960s, the physicist J. R. Black developed an empirical model to estimate the MTF of a wire segment, taking EM into consideration [17]:

$$\text{MTF} = \frac{A}{J^n} \cdot \exp\left(\frac{E_a}{k \cdot T}\right) \quad (1)$$

where A is a constant based on the cross-sectional area of the interconnect, J is the current density, E_a is the activation energy (for example, 0.7 eV for grain boundary diffusion in Al [15,17], 0.9 eV for surface diffusion in Cu [18]), k is the Boltzmann constant, T is the

temperature and n a scaling factor. Studies on Al and Cu interconnects show that void-growth-limited failure is characterized by $n = 1$, while void-nucleation-limited failure is best represented by $n = 2$ [11,19].

Equation (1) indicates that current density $\mathcal{J}$ and (to a lesser extent) the temperature T are deciding factors in the physical design process that affect EM.

3. INTERACTION OF EM, THERMAL AND STRESS MIGRATION

EM rarely acts alone. IC designers must also be aware of thermal and stress migration; both are introduced and described in this section in terms of their interaction with EM.

3.1 Thermal and stress migration

Temperature gradients produce *thermal migration*. In this case, high temperatures increase mean atomic speeds. The number of atoms diffusing from areas of high temperature to areas of lower temperature is greater than the number diffusing in the opposite direction. There is thus a net diffusion in the direction of the negative temperature gradient, which can lead to significant mass transport.

Stress migration describes a type of diffusion that balances mechanical stress. While there is a net atomic flow into areas subjected to tensile forces, metal atoms flow out of areas under compressive stress. Similar to thermal migration, this leads to diffusion in the direction of the negative mechanical tension gradient. The result is a balanced vacancy concentration that matches the mechanical tension.

3.2 Mutual interaction

Migration processes can produce an equilibrium state, where the limiting (or counteracting) process is another type of migration. For example, the equilibrium between electromigration (EM) and stress migration (SM) is named *Blech effect* as described next.

EM interacts directly with SM, as the dislocation of metal atoms induces mechanical stress, which is the driving force behind SM. SM works against EM, as its flow is directed from compressive to tensile stress, which is opposite to the EM flow direction. The resultant net flow is thus reduced and the damaging dislocation due to EM is abated or even halted (Blech effect).

Thermal migration (TM), on the other hand, is not a dedicated EM countermeasure, as it is less dependent on the current direction than EM. It may follow a different path than EM, depending on the temperature gradient, which may stem from sources other than current density.

While temperature accelerates EM as well as the other migration types, we are most likely to observe a mixture of all three types in a current-density hotspot. To effectively apply countermeasures, the dominant migration force must be known.

EM, TM and SM are closely coupled processes as their driving forces are linked with each other and with the resultant migration change, as discussed next.

Current density raises the temperature through Joule heating, and temperature change modifies mechanical stress through differences in expansion coefficients. Furthermore, temperature and mechanical stress affect the diffusion coefficient, which expresses the magnitude of the atomic flux. This, in turn, modifies the behavior of all three migration types. In addition, the mechanical stress is influenced by the change in atomic concentration caused by all migration types individually. These complex interactions are visualized in Fig. 4.

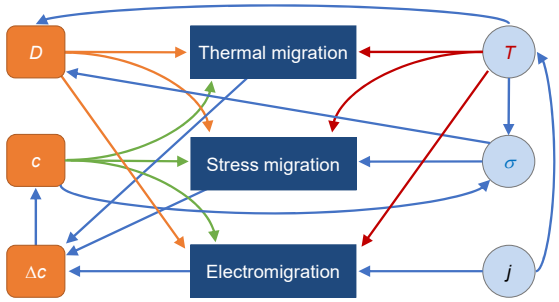

Figure 4: Interaction between TM, SM and EM through their driving forces temperature (T), mechanical stress (σ) and current density (j). The related migration parameters diffusion coefficient (D), concentration (c) and concentration change (Δc) are also shown

The effects of different combinations of EM, TM and SM are depicted in Figs. 5 and 6. Depending on the origins of the driving forces, several different amplifying and compensating results are observed.

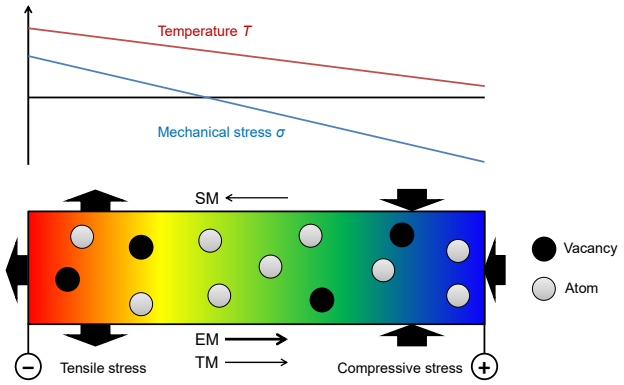

Figure 5: Example of coupled migration processes in a wire segment, where electromigration (EM) and thermal migration (TM) proceed from left to right, while stress migration (SM) flows in the opposite direction

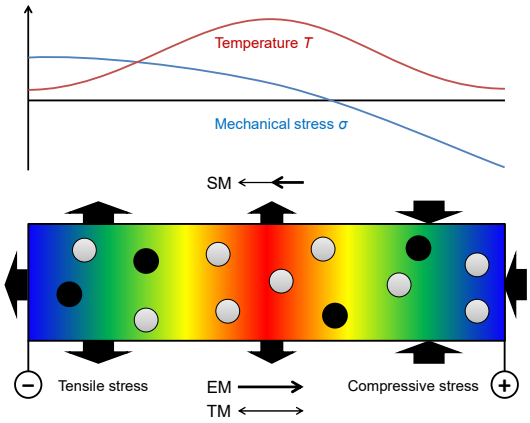

Figure 6: Another example of coupled migration processes. Here, thermal migration is induced through a hotspot in the middle of the segment, while the mechanical stress is a combination of tensile stress in the middle and EM-induced stress. This situation may occur near thermal vias or TSVs

Clearly, the causes and effects of migration are interrelated and at times self-reinforcing. For example, the void growth acceleration caused by positive feedback from a temperature rise is well known [20]. In general, the effects of different migration modes should be considered as interdependent. In particular, the material flows $\mathcal{J}_E$ (from EM), $\mathcal{J}_T$ (from TM), and $\mathcal{J}_S$ (from SM) can be calculated as follows [21]:

$$\vec{J_E} = \frac{c}{kT} \cdot D_0 \cdot \exp\left(-\frac{E_a}{kT}\right) \cdot z^* e \varrho \vec{j}\,, \tag{2}$$

$$\vec{J_T} = -\frac{cQ}{kT^2} \cdot D_0 \cdot \exp\left(-\frac{E_a}{kT}\right) \cdot \operatorname{grad} T\,, \tag{3}$$

$$\vec{J_S} = -\frac{c\Omega}{kT} \cdot D_0 \cdot \exp\left(-\frac{E_a}{kT}\right) \cdot \operatorname{grad} \sigma\,. \tag{4}$$

In these equations, c is the atomic concentration, k the Boltzmann constant, T the absolute temperature, D_0 the diffusion coefficient at room temperature, E_a the activation energy, z^* the effective charge of the metal ions, e the elementary charge, ϱ the specific electrical resistance, j the electrical current density, Q the transported heat, Ω the atomic volume, and σ the mechanical tension (stress).

The resultant diffusion flux, defined as follows:

$$\vec{J_a} = \vec{J_E} + \vec{J_T} + \vec{J_S}\,, \tag{5}$$

is the net effect of the combined driving forces.

In order to prevent EM effects, the net diffusion flow must be reduced to zero. For example, the EM diffusion flow and its associated SM flow (in the opposite direction) can cancel each other out (Blech effect).

3.3 Differentiation

The cause of a specific damage cannot be established by its appearance, as all damage, regardless of its origin, materializes as voids caused by diffusion processes. However, the locations and surroundings of these different damage types are pointers to their possible origin(s); this is exemplified in Fig. 8.

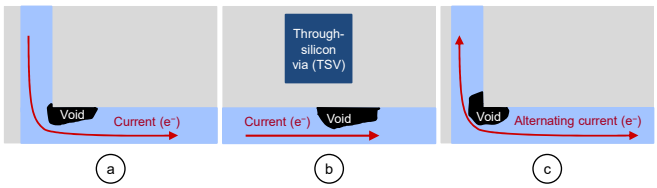

Figure 8: Different types of damage typically caused by EM (a), SM (b) and TM (c) (top view). In most cases, the cause of damage cannot be ascertained by its appearance, but rather by its location and surroundings

As discussed earlier, EM takes place inside wires and is driven by electric currents. Therefore, EM damage is most likely to be found in areas of high current density, that is, high currents and small cross-sections. Current crowding at wire bends and vias is a strong EM indicator.

TM correlates somewhat with EM, as large temperature differentials occur near locations of high current densities. Therefore, current crowding spots are also high temperature spots that are a potential TM driver. Here, large temperature differentials (in addition to current differentials) promote atomic motion.

There are many other causes of temperature gradients, such as external heating or cooling, and the heating of active circuit elements, like transistors. Thermal conduction can also dislocate TM damage from hotspots in wires towards cooling spots or areas of low thermal conductivity. This, and alternating current directions might be TM indicators, whereas EM is always linked to locations of high current and a dominant current direction.

SM is often coupled with EM as a counteracting force. EM-transported atoms induce mechanical stress that consequently leads to SM in the opposite direction to the causal EM. Hence, SM has the potential to moderate EM damage in short wire segments (Sect. 5) and in locations of low current densities.

SM stems not only from EM, but also from fabrication, mismatches between different coefficients of thermal expansion (CTE), and induced stress from obstacles like through-silicon vias (TSV). With the increase in 3D-IC applications [22], stress-induced damage near structures such as TSVs in 3D-stacked ICs (Fig. 8 (b)) are rapidly raising concerns [20].

Finally, we would like to point out that hillocks (Fig. 3) and whiskers [20] usually point to EM as their cause. However, SM can also participate in the overall diffusion flow, and, hence, must be considered as well.

4. EM ANALYSIS THROUGH SIMULATION

4.1 Migration analysis

Migration is a complex problem that can be mathematically modeled by a system of differential equations. Several solution strategies are available for this type of mathematical problem:

- Analytical methods
- Quasi-continuous methods,
- Concentrated or lumped element methods, and
- Meshed geometry methods, such as
  - Finite element method (FEM),
  - Finite volume method (FVM), and
  - Finite differences method (FDM).

The last of these methods, *meshed geometry methods*, offer several advantages for migration analysis. The degrees of freedom can be spatially resolved in a flexible manner by adjusting the mesh granularity. The calculation effort is limited due to the bounded degrees of freedom – the mesh is finite. Using only basic geometries for the mesh elements further simplifies simulation.

The *finite element method* (FEM) is a universal tool for calculating elliptic and parabolic equation systems. It is a numerically very robust method suitable for a wide range of applications. The system of equations is built from degrees of freedom for nodes and elements.

For reduced problem sizes, such as the EM analysis of power and ground nets, FEM delivers precise results in reasonable calculation times. However, model preparation and calculation efforts are high when meshed methods are applied to complex geometries. These challenges are encountered in EM analysis due to the increasing complexity of geometries in VLSI circuits. Since signal nets are increasingly infected with EM, filtering only EM-critical nets, as proposed in [23], is no longer a viable option for reducing problem complexity.

4.2 Efficient FEM for EM analysis

Quick simulations are called for in physical design. These simulations are only one part of the verification phase; they must be repeated iteratively in the design flow. For example, applying FEM for use in the full-chip verification of complex integrated circuits is far too slow [16,23,24].

In order to maintain FEM precision despite the increasing number of structures and geometries to be analyzed, we propose

that EM simulations are separated from the actual verification process. This means that FE analysis is performed prior to verification or even prior to layout synthesis. Routing, for example, will then be carried out exclusively with verified routing elements from a library. Hence, an entire library of routing elements with simplified parametric models attached will be verified by FE analysis. The complete chip can then be verified rapidly. The library should include all routing elements required to build a complete layout; the library size can be kept low by using only highly repetitive patterns. The verification is simplified to calculating only critical results from the actual boundary conditions by using the parametric models to check against current-density limits, or other migration metrics (Fig. 9).

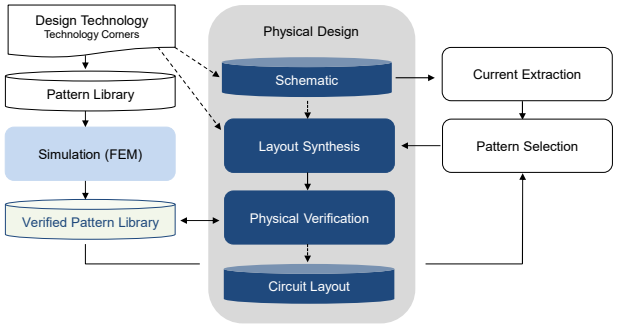

Figure 9: A full-chip EM simulation based on FEM should be uncoupled from the actual synthesis and verification process to compensate for the increasing circuit complexity. The resulting layout synthesis would then be restricted to pre-verified (routing) patterns to enable a fast pattern-based physical verification [24]

An important prerequisite for the above-mentioned verification method of combining several discrete FEM simulations is that the partial solutions equate with the respective parts of the complete solution. This requirement is met if the boundary conditions are transformed correctly between the full and partition models, as we discuss next.

The method's prerequisite can be best explained with a typical example, where a complete wire connection is simulated as a single entity and then split into separate parts. If we can transform the boundary conditions to the parts in a suitable manner, we will obtain equivalent simulation results.

There are several useful rules for finding the best locations to split the model. The best place to split is at locations where the boundary conditions are homogeneous, as they can easily be applied to FE models. Current-density regions in a straight wire some distance away from vias and branches are good places to split the model. If, however, the layout element of interest consists only of a via region, some adjuncts will have to be added to the wires in order to establish a homogeneous boundary condition.

The atomic flux, on the other hand, stops at diffusion barriers, that is, the transition from one material to another (this typically occurs near vias). These diffusion barriers provide ideal boundary conditions for this model.

Temperature influences and mechanical stress from "unmodeled" surroundings should not affect the simulation results. To this end, a sufficiently large volume surrounding a wire should be modeled, so that the difference between homogeneous model conditions and inhomogeneous real conditions can be neglected inside the wire.

The same applies when modelling temperature directly, as the surrounding dielectric distributes heat as well as the metal, only with lower conductivity.

Partitioning FE routing models without loss of accuracy is a prerequisite for applying FEM for full-chip current-density analysis. This is best done by comparing simulation results for generic sample patterns calculated both jointly and separately. Figures 10 and 11 visualize this using a T-shaped wire segment inside one metal layer and a via connection. Figure 10 (left) shows the current-density results from two separate (distinct) simulations. The simulation of both patterns combined is visualized in Fig. 10 (right); the combined results agree well with the individually calculated results. Figure 11 pictures the current-density distribution at the interface between the two patterns in a joint simulation; this is a measure of the error in the individual simulations. The maximum error is 3% in the visualized case; this is an acceptable value that has been verified for other patterns as well [24].

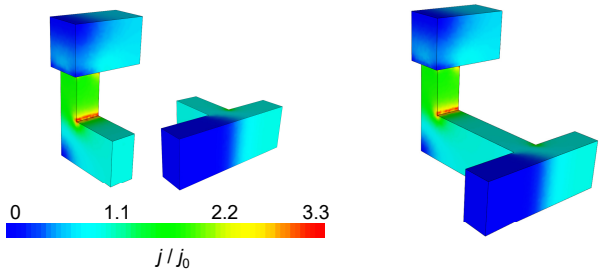

Figure 10: Current-density distribution using FEM for a T-shaped wire segment and a via connection. Results from separate simulations of the two individual patterns with homogeneous constraints at the cut surfaces are shown on the left. Joint FEM current-density simulation of the two patterns combined (on the right) produce a sufficiently similar outcome

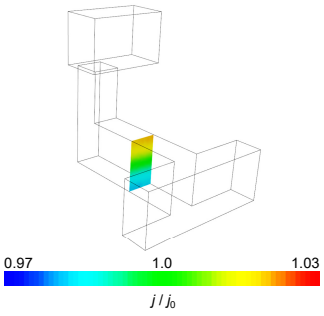

Figure 11: Verifying homogeneity of the current density at the cut surface between the two FEM sub-models (the maximum deviation is 3% here) can be used to ensure that joint and separate simulations show matching results

Evaluating interconnect structures in advance and building the layout exclusively from evaluated structures enables much faster verification: even a single circuit simulation, i.e., generating the (simulated) library patterns and using them only once, can be faster than a conventional, complete FEM simulation of the entire final layout [24].

With the aforementioned method of pre-verifying routing patterns, FEM, including its precision and spatial resolution, can be applied in the (full-chip) EM verification of complex, up-to-date circuit layouts.

4.3 Further simulation strategies

In addition to using FEM for current-density simulation, a host of other, more sophisticated simulation strategies are available for EM analysis (Fig. 12); please refer to [20] for a detailed description. Basically, the *atomic flux* can be calculated from current density and other driving forces to get a deeper insight into the damaging process. We can also simulate *mechanical stress* development as the driving force behind stress migration and compare it with the critical stress. *Void growth* can be simulated in order to better understand the damaging processes, in terms of both void nucleation (mechanical stress change) and void growth.

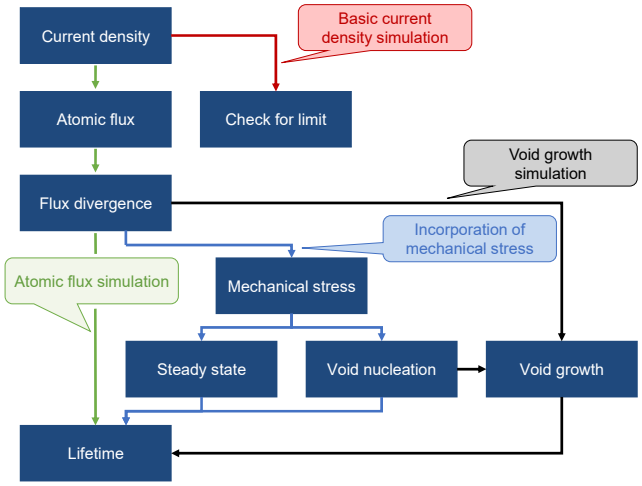

Figure 12: Overview of simulation strategies for EM analysis based on different parameters affecting migration; they are discussed in detail in [20]

5. MITIGATING EM IN PHYSICAL DESIGN

The most basic options for influencing current density and EM during the (physical) design of an electronic circuit are:

Wire material: Pure copper used for interconnect metallization is more EM-robust than aluminum at low temperatures.

Wire temperature: Interconnect MTF is greatly impacted by conductor temperature, as evidenced by Eq. (1) where it appears in the exponent. For an interconnect to remain reliable at high temperatures, the maximum tolerable current density of the conductor must necessarily decrease. On the other hand, lowering the temperature supports higher current densities while maintaining the reliability of the wire constant.

Wire width: Given that current density is the ratio of current I and cross-sectional area A, and given that most process technologies assume a constant thickness of the printed interconnects, it is the wire width that has a direct bearing on current density: the wider the wire, the lower the current density and the greater the resistance to EM.

The above mentioned three options have been discussed in detail in [25]. They are of limited use in today's technologies because they have been largely exploited and/or their application would be counter-intuitive to the new technology node itself, that is, its reduced structure size [26]. Therefore, tolerable current density limits need to be maximized by exploiting other EM-inhibiting measures, which we discussed in [20][27] and that are summarized next.

Bamboo effect: Diffusion typically occurs along the grain boundaries in a wire. High EM resilience can be achieved with conductor cross-sections smaller than grain sizes (in this case, grain boundaries are perpendicular to the direction of diffusion).

Short-length effect: Any wire length below a threshold length (Blech length) will not fail by EM. Here, mechanical stress buildup causes a reverse migration process which reduces, or even compensates for, the EM flow.

Reservoirs: Reservoirs increase the maximum permissible current density by supporting the stress-migration effect to partially neutralize EM. Reservoirs can, however, have an adverse effect on reliability in nets with current-flow reversals, as the (useful) stress migration is reduced in this case.

Via configurations: The robustness of interconnects fabricated with dual-Damascene technology depends on whether contact is made through vias from "above" (via-above) or "below" (via-below). It is easier to avoid EM with via-below configurations than with via-above configurations, as the former tolerate higher current densities due to their higher permissible void volumes.

Redundant vias: Multiple vias improve robustness against EM damage. They should be placed "in line" with the current direction so that all possible current paths have the same length. Current distribution is then uniform and there is no local detrimental increase in current density between vias.

Frequencies: The high frequencies normally encountered in signal nets reduce EM damage more than in power supply nets or very low-frequency nets under otherwise comparable operating conditions. Hence, different current-density boundary values (limits) must be assigned in EM analysis.

In order to prevent EM damage, the measures outlined above must be assessed with appropriate analysis tools, such as FEM (Sect. 4.2). Specifically, the impact of current density and other design parameters on the diffusion processes can be represented spatially by FEM, and the effects and measures analyzed by simulation. Many measures, such as the critical length effect, reservoirs, and the type of wire contacting, leverage stress migration as an effective EM inhibitor.

In summary, our investigations yield the following practical guidelines [20]:

- The critical length effect can be applied to obtain an EM-robust layout at the cost of no more than a slightly lower circuit performance.
- Reservoirs can be effective in power supply nets. However, signal nets do not significantly benefit from reservoirs due to the changing direction of the current; indeed on the contrary, incorporating them could negatively impact EM robustness, depending on the manufacturing process used.
- A via-below configuration, where the vias contact the critical segment from below, should be chosen in the dual-Damascene technology, if the layout permits.
- The product of length and current density must be bounded to a greater degree in the (remaining) via-above segments to compensate for their heightened EM susceptibility.
- Special care must be taken with multiple vias, as their geometrical configuration impacts time to failure. Redundant vias are generally better than an individual via. However, possible EM benefits depend on the inter-via configuration and the vias' relationships with the connected wire segments, as higher local current densities may adversely effect reliability.

6. OUTLOOK

This final section sketches a roadmap for EM-compliant layout design in future (EM-critical) technological nodes.

6.1 Segment lengths

The comparative evolutions of segment lengths and prospective Blech lengths due to IC downscaling are not encouraging. To illustrate this, technology-dependent, EM-robust segment lengths that are achievable solely with the short length effect (Blech length) are plotted in Fig. 13, based on data taken from the ITRS Roadmap [2]. These plots are based on maximum current densities predicted in the roadmap.

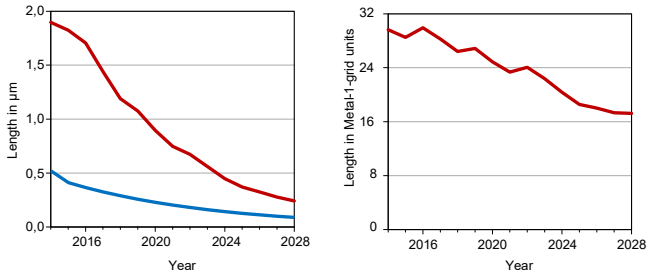

Figure 13: Segment lengths, up to which the short length effect alone suffices for EM robustness, depending on the respective technology node; absolute values in microns (red line on the left) and relative values in multiples of the routing grid (right) [20]. Also shown are the actual/expected mean segment lengths (blue line on the left) which fall off to a lesser degree. Values from ITRS [2] based on a maximum mechanical stress of 100 MPa

The red curves in Fig. 13 show that EM-robust segment lengths decrease significantly in pace with the structural miniaturization predicted in the ITRS Roadmap [2]. As can be seen as well, these Blech lengths drop more sharply than the actual mean segment lengths on the chip (blue line in Fig. 13 left). Furthermore, we can assume that the routing grid is almost proportional to the mean segment length, as the mainly short segment lengths are determined by the spacing between transistors. How alarmingly "less exploitable" EM-robust segment lengths really are becomes manifestly apparent if we plot these Blech lengths w.r.t. the routing grid, i.e., in multiples of the routing grid (Fig. 13 right).

Both observations imply that the number of nets benefiting from the short length effect drops with decreasing semiconductor scale. In other words, the Blech length is exceeded in an increasing proportion of the routing – up to approximately 5% by the year 2026 [20]. Countermeasures, such as the introduction of reservoirs, will be required for these segments.

6.2 Library of EM-robust elements

Increasingly, the required measures outlined in the preceding sections are being integrated in practical tools for layout design. However, these measures will need to be implemented as algorithms in the future, to automate the design of EM-robust integrated circuits.

One option to achieve this goal is to develop a *pattern generator* that produces routing elements for a given fabrication technology, that are EM robust when carrying a specified current density. These routing elements could be stored in a library, and the routing layout then drafted exclusively with routing elements from this library (Fig. 14).

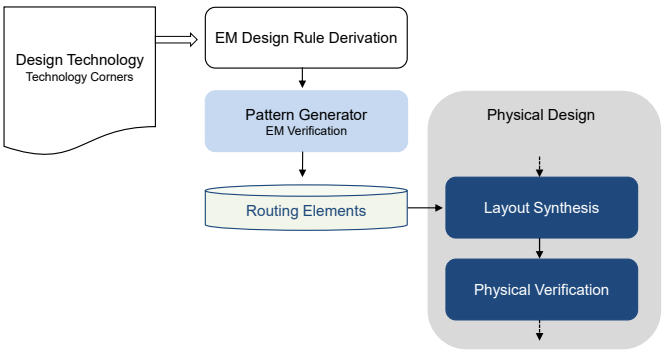

Figure 14: Improving the EM robustness of the generated layout by restricting physical design to EM-robust routing elements ("layout patterns") that have been generated for a given technology and verified with special emphasis on EM properties

Consequently, IC routing will be highly regulated, that is, *constraint-driven*, as only library elements may be used to create it. It will then be much easier to verify EM properties, as the robustness of individual elements is verified when the library is created. All that remains to be done in the complete layout is to examine the mutual interaction between elements when they are combined. The complexity of EM testing is thus reduced significantly, with the result that even for complex routing geometries no FE calculations are required for EM-robustness verification (Sect 4.2). Furthermore, parameters can be assigned to these analyses and the results stored in the library, allowing verification with a simplified (routing) model.

6.3 Constraint-driven physical design

Physical designs with ever-smaller feature sizes are subjected to a growing number of more complex constraints. These constraints are increasingly curtailing freedom in the design flow and are setting the boundaries of an ever-decreasing solution space. Hence, we are witnessing a slow, but steady evolution from a *constraint-correct* design flow to a *constraint-driven* one. In the latter case, design algorithms and methodologies are increasingly being governed by constraints instead of only verifying their correct implementation [28,29].

As has been shown throughout this paper, EM considerations are producing additional constraints in the design flow. The resultant reduction in the available solution space for physical design is illustrated in Fig. 15. Hence, a distinction must be made in the future between EM-robust and non-viable layout elements, whereby only EM-robust elements may be used for physical design. Thus, we expect constraint-driven physical design to predominate in future.

7. SUMMARY

EM has become an increasingly intractable design challenge due to IC-down-scaling. As has been shown, EM-aware design is no longer a design option; rather, it has become a prerequisite for producing reliable circuits. This paper summarizes our current understanding of EM and how its effects can be analyzed and moderated in practice. We also describe ways of facilitating EM-compliant layout design in future technology nodes.

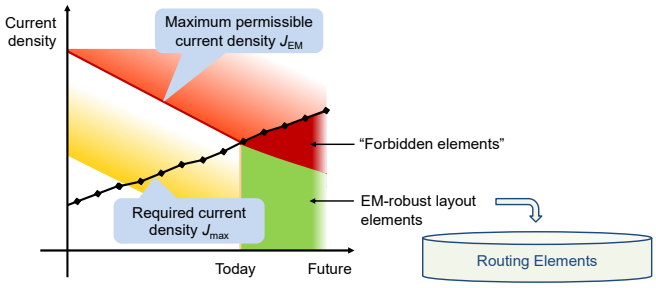

Figure 15: Projected evolution of the physical design (PD) solution space with falling current-density boundaries (red line) and increasing required current densities (black dots, cf. Fig. 1, right). The solution space for the allowed layout elements will be increasingly curtailed; hence, today's constraint-correct PD evolves into constraint-driven PD where only EM-robust layout elements may be used (see Fig. 14 for the generation of these elements)

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