Hierarchical Current-Density Verification in Arbitrarily Shaped Metallization Patterns of Analog Circuits

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***Abstract*—Electromigration is caused by high current-density stress in the metallization patterns and is a major source of breakdown in electronic devices. It is, therefore, an important reliability issue to verify current densities within all stressed metallization patterns. In this paper, we propose an efficient methodology for hierarchical verification of current densities in arbitrarily shaped custom-circuit layouts as commonly used in analog circuits and analog blocks in mixed-signal ICs. Our approach includes a quasi-three-dimensional model to verify irregularities, such as vias and incorporates thermal simulation data to account for the temperature dependency of the electrical field configuration and the electromigration process. The described methodology, which can be integrated into any IC design flow as a design rule check, has been successfully tested and verified in commercial design flows.**

***Index Terms*—Current-density verification, current-driven routing, custom circuit design, design rule check (DRC), electromigration, IR-drop, layout verification.**

I. Introduction

THE TERM "electromigration" is applied to mass transport in metals when the metals are stressed at high current densities. This results in a change of conductor dimensions, thereby causing spots of high resistance and eventual failure due to destruction of the conductor at this spot. Electromigration has been recognized as a wear-out failure mode in VLSI circuits employing metal layers of inadequate cross-sectional area.

The ongoing reduction of circuit feature sizes has aggravated the problem of electromigration in integrated circuits to a level where *current-density verification* is required to detect electromigration-related failures in critical signal and power nets in order to guarantee a specified interconnect lifetime. Since manual current-density verification of complex analog circuits is extremely time-consuming and error-prone, we have developed an automatic verification methodology for electromigration analysis of arbitrary metallization shapes.

The presented methodology and algorithms are especially tailored for current-density verification of analog circuits and analog blocks in mixed-signal circuits. These circuits usually incorporate high currents in their interconnects, ranging from several hundred microamperes up to several tens of amperes. The interconnect in these circuits mainly consists of arbitrarily shaped metallization patterns (i.e., custom shapes) such as 135° corners, circles, or arc-shaped bends of wire segments.

In this paper, we assume that all necessary current-density constraints are provided by the manufacturing process technology, thus enabling a correct layout design for the predefined circuit lifetime. Hence, the term "current-density verification" is considered as a design rule check (DRC) that verifies the ability to meet all given current-density constraints within the interconnect layout.

The main contributions of our approach are:

- an efficient methodology for *hierarchical* verification of current densities in *arbitrarily* shaped custom circuit layouts;
- a quasi-three-dimensional model for verifying irregularities like vias and via edge stress, using honeycomb-like structures;
- a current-density verification method that incorporates thermal simulation data to account for temperature dependence of the electrical field configuration and the electromigration process;
- the option of integrating the proposed methodology as an *automated* current-density DRC into virtually any IC design flow.

The remaining paper is organized as follows. Previous work done in the field of electromigration research and verification tool development is discussed in Section II. A brief introduction of the electromigration effect is given in Section III. Section IV presents an overview of our verification flow. Section V describes the current-value characterization in detail, followed by a presentation of our current-density calculation in Section VI. Section VII focuses on details of verifying and visualizing current densities. Finally, Section VIII presents our experimental results, Section IX describes the limitations of our approach, and Section X gives our conclusion.

II. Previous Works

The effect of electromigration and its relation to the mean time to failure (MTTF) of an electronic circuit has been extensively studied over the last three decades [6], [8], [20], [31]. Although the basic understanding of the failure mechanism has improved in recent years, many aspects are still not fully understood. A good summary of electromigration can be found in [21] and [24].

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The influence of thermal effects on interconnect reliability has been discussed in [3], [11], and [13]. Discussions of current values and their application to precise interconnect lifetime prediction can be found in [17]–[19], and [25]. Lifetime prediction incorporating short pulse effects is presented in [2].

Several electromigration analysis systems, which are limited to the verification of *digital* designs, have been presented [10], [25], [30]. Hajj *et al.* [10] reported a computer-aided design system for electromigration analysis based on current-density investigation for relatively simply shaped layout patterns in CMOS circuits. The approach divides the layout structure into several simple shapes that are transferred in an *RC* network. Each element of the network is then simulated independently. In 1997, Simplex Solutions [25] introduced "Thunder & Lightning," a commercial toolset for electromigration analysis of power and ground networks as well as for digital signal nets. Cadence Design Systems [30] also provides a verification system "ElectronStorm" for electromigration and Joule heating in power and signal nets in digital applications.

To the best of our knowledge, only one current-density simulator for *analog* applications has been published [1]. It decomposes all wires into rectangles and irregularities. The resistance of the rectangles is calculated and then used to extract a netlist that incorporates references to the corresponding geometrical dimensions. Irregularities with nonhomogeneous current distribution, such as wire bends, pins and vias, cannot be validated.

Since verification follows the layout step, generating the layout under consideration of current densities is a closely related topic. Methodologies for current-driven wire planning and current-driven routing have been presented in [15] and [16].

III. Electromigration Problem

The copper or aluminum interconnects of a chip are polycrystalline, i.e., they are made up of grains of lattice. While conducting a current through this interconnect, the electrons will interact with imperfections in the lattice, causing atoms from the lattice boundary to migrate in the direction of the current flow. In other words, atoms can be transported at the boundaries between the grains as a result of the "electron wind."

In the direction of the electron flow, copper or aluminum atoms will be deposited over time (so-called "hillocks," see Fig. 1), resulting in a buildup of mechanical stress at the hillock area. This can lead to cracks in the surrounding insulation layers with a subsequent material migration toward these cracks. In the opposite direction, voids will grow between some grain boundaries (Fig. 1). While the hillocks might introduce shorts to neighboring wires, voids will reduce the conductivity of the interconnect over time, which can eventually lead to interconnect failures.

It should be noted that the mechanical stress built up in the hillock area also causes a reversed migration process, which reduces or even compensates for the effective material flow toward the anode [7]. This compensation process depends on several factors: the amount of mechanical stress the insulating layer can sustain, the current density, and the length of the stressed wire segment. (Exploiting the compensation effect enables the design of so-called "immortal wires" that are not susceptible to the above-mentioned material migration processes.)

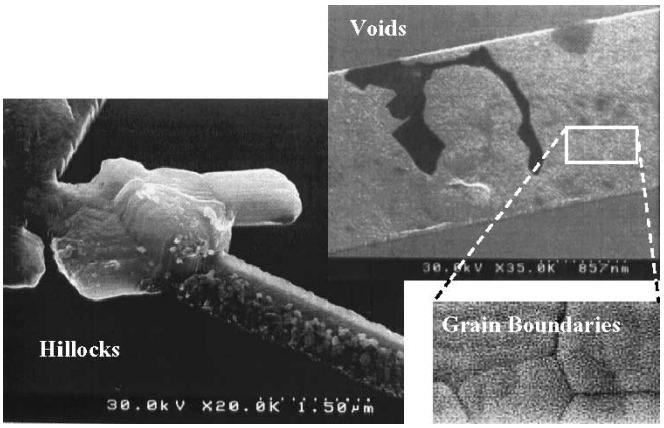

Fig. 1. Hillock and void formations in wires due to electromigration (Photo courtesy of G. H. Bernstein and R. Frankovic, University of Notre Dame).

The described mass transport in metals due to electron wind is termed "electromigration." The failure of a single wire due to electromigration will often cause the entire chip to fail.

Most chips must have a mean time to failure (MTTF) of at least ten years. Failure due to electromigration for a single wire is usually expressed by Black's equation [6]:

$$\mathrm{MTTF} = \frac{A}{J^n} \cdot \exp\left(\frac{E_a}{k \cdot T}\right) \tag{1}$$

where A is a cross-section-area-dependent constant, J is the current density, E_a is the activation energy, k is the Boltzmann constant, T is the temperature, and n a scaling factor (usually set to 2, according to Black [6] and computer-based modeling experiments reviewed in [24]).

As is obvious from (1), the MTTF due to electromigration depends on two factors that can be influenced by the chip designer: temperature and current density. This article will focus on current density as the major parameter in addressing electromigration during physical design.

Finally, it should be noted that copper wires have shown a better resistance against electromigration than aluminum wires. This is due to the higher activation energy of copper for the electromigration failure effect and its higher conductivity for both electricity and heat [9], [27].

IV. Current-Density Verification Flow

A. Overview

The current-density verification flow of our approach is illustrated in Fig. 2.

Each cell within a hierarchical design has to be simulated in order to verify its specification. The simulation stimuli should include the entire range of possible input values, including worst-case conditions. The simulation results in a set of postprocessed current values that are attached to the cell pins (*current characterization*, Section V).

Based on the processed simulation data, a module generator creates a layout representation of the schematic devices. Placement and routing are performed during the subsequent layout step.

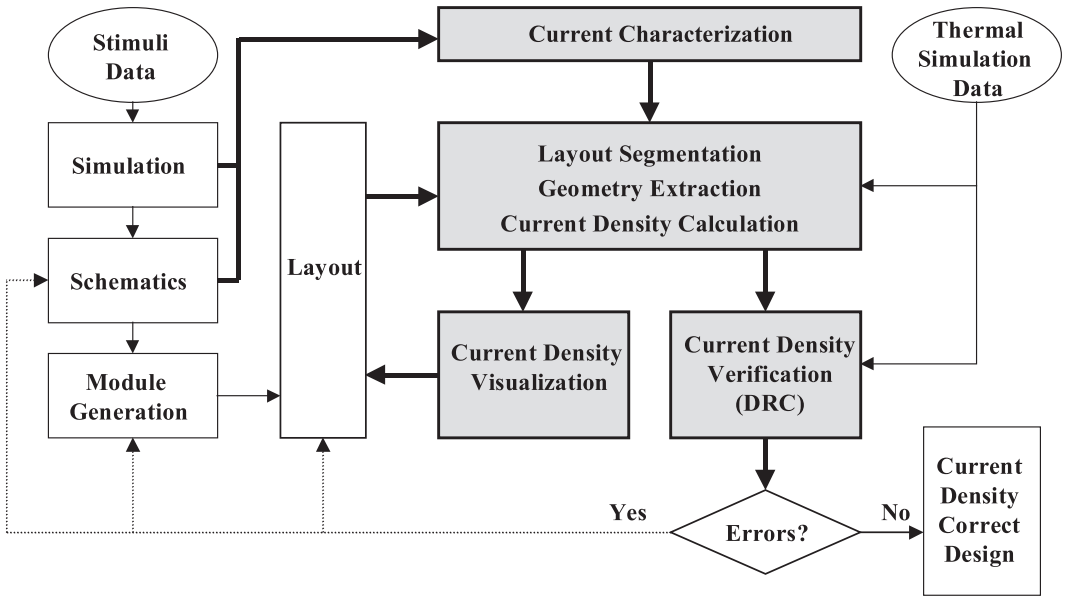

Fig. 2. Current-density verification flow.

The layout geometry of a completed net, pin currents, and process-relevant data are transferred to the *current-density calculation* tool, which calculates the current density within each layout element such as paths, vias, and via arrays (Section VI). The results are used to perform *current-density verification* (Section VII-A) or are transferred to a *visualization* tool (Section VII-B).

Current-density-related violations are detected during current-density verification. Depending on the type of violation, the verification results are returned: 1) to the layout step (e.g., if encountering paths with insufficient widths); 2) to the module generator (e.g., if pins cannot carry the attached currents); or 3) to the schematic entry (e.g., if a cell in another hierarchy must be adjusted).

Both current-density calculation and verification can make use of thermal simulation data in order to account for the temperature dependency of the electrical field configuration and the electromigration process.

B. Verification of Hierarchical Cells

An important aspect of a hierarchical design is the necessity of *independent* testability of hierarchical elements such as layout cells or blocks. Specific importance must be given to: 1) current values transferred between cells of different hierarchy levels and 2) location-dependent temperature data.

The current values of a pin located at a cell interface are attached as cell port properties. In the next higher hierarchy level, these values are visible as instance pin properties. In order to allow an independent verification of cells in different hierarchies, current values at the cell interfaces have to obey the following rules (Fig. 3).

- The equivalent current value $|I_{Pi}|$ attached to a cell port P_i has to be equal or greater than the equivalent current value $|I_{Qj}|$ attached to the derived instance pin Q_j of the cell in the next higher hierarchy level.

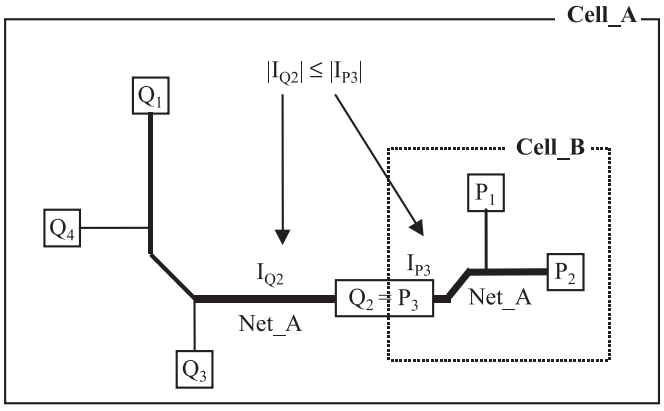

Fig. 3. Routed in two cells in different hierarchies, net Net_A is separated into subnet Cell_A:Net_A and subnet Cell_B:Net_A. In order to verify the subnet in Cell_B independently of the subnet in cell Cell_A, the "higher level" pin current $|I_{Q2}|$ must not exceed the assumed "lower level" pin current $|I_{P3}|$.

- The current value I_{Pi} attached to the cell port must be determined under the consideration of Kirchhoff's current law applied to this net.

Temperature data used in current-density calculation and verification is location-dependent. Thus, if the cell to be evaluated is instantiated, the various instance locations have to be known in advance (top-down design) in order to obtain correct temperature data. For example, temperature data can be obtained by superimposing all thermal field plots [28] of these cell instances and using the obtained maximum temperature at a position (x, y). If the instance location is not known (e.g., for bottom-up designs), a worst-case temperature field plot is used.

V. Current Characterization

Our methodology includes three methods to obtain current values: 1) using a circuit simulation tool that can deliver time-dependent and time-independent pin current values; 2) incorporating a cell or device library with predefined and appropriately scaled time-independent pin current values; or 3) using manu-

ally attached time-independent pin current values assigned by the circuit designer.

We use a standard circuit simulator for simulation of the circuit netlist, where parasitic wiring resistances, capacitances and inductances are neglected. The results from one or more simulations are postprocessed by calculating a set of *direction-dependent* pin current values representing the time-*independent* and/or time-*dependent* minimum and maximum currents at each pin.

The usage of time-*independent* minimum and maximum current values per pin (i.e., two values) has two advantages. Firstly, these values can be library-based, enabling a high degree of automation. Secondly, time-independent pin current values allow manual adjustment and hence, support the use of expert knowledge. However, this static approach bears the disadvantage of losing all information about a current flow between Steiner points and is therefore only suitable for nets with a small number of branches. Furthermore, all pin current values must be added up for upper and lower bound checks in the next net branch in order to verify a possible worst-case working condition.

Time-*dependent* current values assigned to pins are their respective minimum and maximum current values and the current values at the other pins' minimum and maximum point of time. (Please note that the direction of the currents is taken into account. According to Kirchhoff's current law, the sum of all current values at a specific point of time must be zero.) Using time-*dependent* current values leads to current vectors assigned to pins with a size of $2n$ current values per pin, where n is the number of pins of the net. Contrary to the above-mentioned method of time-independent current values, this "semidynamic" approach delivers a more precise prediction of the worst-case current flow between Steiner points. Furthermore, a time-dependent worst-case current flow in *all* net branches can be retrieved.

In order to exploit their respective advantages, we utilize time-independent current values for current-density calculation and time-dependent current values for the visualization of current density and voltage potential.

A closely linked topic is the relation between the current waveform and the estimated MTTF of the interconnect. Studies in [17] and [18] show an increased estimated lifetime for bidirectional and pulsed current stress compared to single direction current and constant current stress (due to the process of "self-healing"). The "ON-time model," based on root mean square (RMS) current, and "average model," based on average current, show a frequency dependence. The transition between these two models occurs at about 1 Hz, with the ON-time model having a better lifetime prediction quality below 1 Hz [18]. Furthermore, the use of RMS current values represents the more conservative approach and, hence, is the preferred model for critical applications. Due to these advantages we use the RMS current model in our approach.

VI. Calculation of Current Density

Common approaches to current-density calculation determine the electrical field configuration by using the finite element method (FEM) [4], [5], [12], [26], the boundary element method [12] or the finite difference method. Our current-density calculation utilizes the well-known FEM due to its excellent ability to handle arbitrarily shaped layout geometry and its ability to deliver fairly good approximations even for calculations with lower resolution.

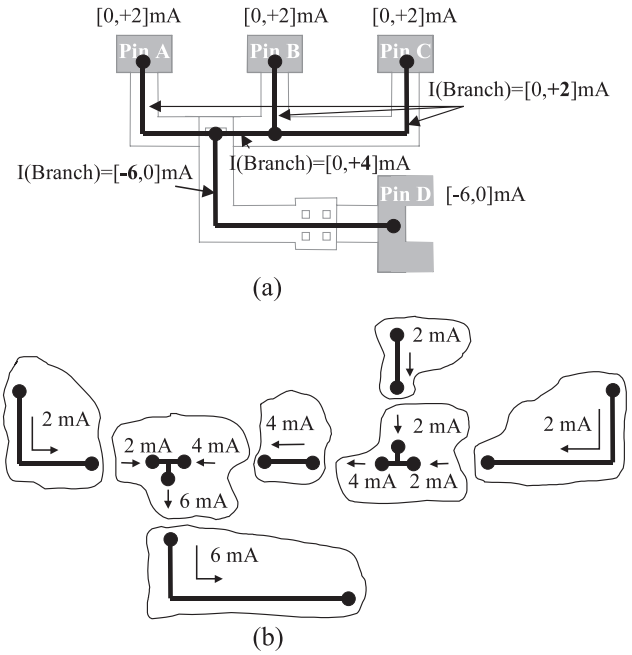

Fig. 4. (a) Layout segmentation of a net is achieved by first determining a current graph and performing a worst-case analysis within this graph. (b) Separated at Steiner points or pins, each "regular layout segment" can then be labeled with one maximum current for which a current-density calculation is performed. "Junction segments" derive their multiple currents from the adjacent layout segments.

Since the wire width of interconnects *carrying high currents* always exceeds the layer thickness by at least a factor of two, we consider the current flow in common layout structures as a two-dimensional problem.

Any current-density calculation method requires at minimum: 1) a set of current values as boundary values; 2) an appropriate representation of the layout geometry; 3) technology-dependent data (e.g., layer thickness); and 4) temperature data (e.g., average chip temperature or a temperature field plot).

Additionally, the verification step (Section VII) needs information about technology-dependent restrictions on the maximum permitted steady current density in each layer. A plot of thermal simulation data is used to account for temperature gradients near significant heat sinks and heat sources.

The methodology of the current-density calculation is presented in detail in Sections VI-A–VI-D.

A. Layout Segmentation

We have developed a procedure called "layout segmentation" in order to split an existing net layout into smaller and independent segments. Layout segmentation reduces verification time and memory consumption.

The first step of the segmentation translates the net layout into a current graph, with the nodes representing either pins or Steiner points [Fig. 4(a)]. The current values for each edge (i.e., each segment) are derived from the current values attached to the pins. The current values of Steiner points are determined

by propagating the worst-case current values within the current graph.

Special consideration must be given to T- or cross-section junctions because of nonhomogeneous current densities in these regions. Therefore, special *junction segments* representing the immediate junction region are generated, with the respective junction currents derived from the currents of the adjacent layout segments [Fig. 4(b)].

It is obvious that the usage of *time-independent* current values prevents Kirchhoff's current law from being applied for current determination. Hence, we create a current graph in order to determine one current value for each layout segment specified by two current constraints. (A net pin or a segmentation border represents a current constraint.) For junction segments (i.e., segments with more than two current constraints), the verification must be performed once for each existing constraint. Therefore, each current constraint is treated once as a temporary "virtual ground pin" by calculating its temporarily assigned current value in such a way that it fulfills Kirchhoff's current law, with respect to the other current constraints.

Special consideration must be given to the distribution of currents at the segmentation borders. We assume a homogeneous application of current shares in segmentation borders if the width of the segmentation border is smaller than its distance to the nearest other segmentation border within the same segment. Since all layout segments must be characterized by homogenous segmentation borders, segments with nonhomogenous borders are merged with the respective neighboring segment until all nonhomogenous segmentation borders are eliminated.

Hence, our rules for layout segmentation can be summarized as follows.

- A two-current-constraint segment connects two junction segments or two pins (or one of each).
- A junction segment is characterized by more than two segmentation borders.
- The distance between two neighboring segmentation borders within the same segment must always exceed their respective width in order to assume a homogenous current distribution at the segmentation borders.

Please note that nets with internal loops within the current graph cannot be verified using layout segmentation. These nets have to be filtered out prior to the current-density verification step and verified as a complete layout structure.

In that case (i.e., no layout segmentation is used), the verification methodology is required to check the complete net at once for both minimum and maximum pin current values. In order to obtain a current flow under worst-case conditions within all net branches, a virtual ground pin must be added to the net and placed at the layout location of the center of the layout-based current graph. Afterwards, the temporary current values attached to the virtual ground pin must be determined in order to fulfill Kirchhoff's current law while checking minimum and maximum current values.

B. Geometry Extraction

In order to apply the FEM, it is necessary to split each layout segment into even smaller "pieces," so-called finite elements.

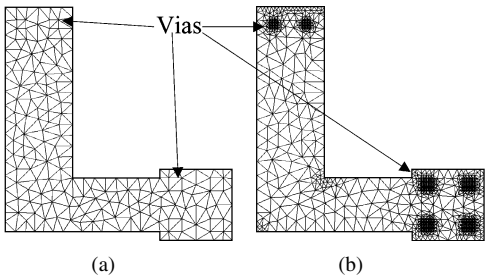

Fig. 5. (a) Generated mesh for a single layout segment and (b) refined mesh around corners and within vias.

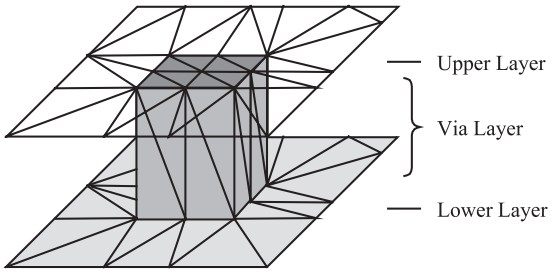

Fig. 6. Via modeled in a quasi-3D representation similar to a "honeycomb" structure.

Using triangles to represent these finite elements ensures a good matching of arbitrary layout geometry, including holes and circles and other oddly shaped geometrical patterns.

We use the Delaunay triangulation [14] with Ruppert's Delaunay refinement algorithm [22] to create a triangle mesh. Fig. 5(a) depicts a regular triangulation mesh of one layout segment from the example in Fig. 4.

A smaller mesh size might be applied around corners and within vias to account for increased current density in these areas [Fig. 5(b)]. The mesh size in all other areas is derived from a user-controlled magnification factor k and the size of the polygon region. We observed that the solution quality using coarse meshes (i.e., the length of the edge of the finite element is approximately equal to the width of the wire) is sufficiently exact for regions with homogeneous current flow. This variable mesh adjustment allows a good compromise between solution quality and calculation time.

Our layout model utilizes so-called "perfect corners" with no roundings. Hence, the simulation results include an intrinsically increased current-density spot directly at the corner coordinates. This high current-density spot at perfectly shaped corners must be filtered out from the obtained verification results to reduce the number of so-called "dummy errors." (We discuss an appropriate filter in Section VII.)

We introduce a quasi-three-dimensional honeycomb-like structure of triangles in order to model asymmetric current-density stress within contact and via structures (Fig. 6). Two "modes" are possible: a low-resolution mode of the via structure permits the check of the via's capability to carry a given current (i.e., to check if the cross-section area of the via is sufficiently large). Via edge stress is additionally detectable with a high resolution mode. (Please refer to Section VIII-B for examples.)

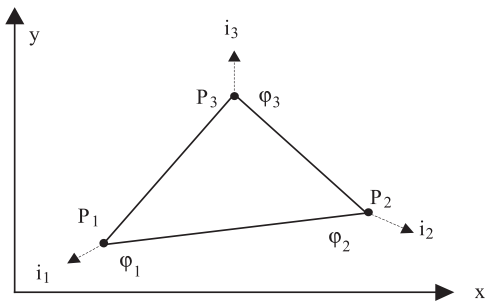

Fig. 7. Representation of a finite element using a triangle (φ voltage potentials, i currents, P mesh nodes).

C. Current-Density Calculation

We calculate the current density for each layout segment using the relationship between current density and an electric field

$$\underline{J} = -\frac{1}{\rho}\left(\frac{\partial\varphi}{\partial x}, \frac{\partial\varphi}{\partial y}, \frac{\partial\varphi}{\partial z}\right)^{\mathbf{T}} \tag{2}$$

where $\underline{J}$ is the current density, ρ is the electrical resistivity, φ is the voltage potential, and x, y, and z denote the coordinates in $\mathbf{R^3}$.

In order to obtain the potential field configuration $\varphi(x, y, z)$ needed in (2), Laplace's equation

$$\Delta\varphi = \frac{\partial^2\varphi}{\partial x^2} + \frac{\partial^2\varphi}{\partial y^2} + \frac{\partial^2\varphi}{\partial z^2} = 0 \tag{3}$$

has to be solved in the field $\boldsymbol{G}(G \in R^3)$ and for the given current boundary conditions. Since we consider current flow as a two-dimensional problem, the z-related third term can be omitted. Hence, (3) can be rewritten as a mathematical variation problem, which can be solved by the FEM as follows.

As mentioned before, our finite elements are triangles that were obtained by triangulation of a layout segment (Fig. 7).

Due to the linear relation between voltage and current in a conductor, a suitable linear assumption for a single triangle can be made

$$\varphi = a_0 + a_1 x + a_2 y. \tag{4}$$

The determination of the integral parts of a single triangle within the above-mentioned mathematical variation problem [derived from (3)] leads to the coefficients a_0, a_1, and a_2

$$\begin{bmatrix} a_0 \\ a_1 \\ a_2 \end{bmatrix} = \frac{1}{S}\begin{bmatrix} x_2y_3 - x_3y_2 & x_3y_1 - x_1y_3 & x_1y_2 - x_2y_1 \\ y_2 - y_3 & y_3 - y_1 & y_1 - y_2 \\ x_3 - x_2 & x_1 - x_3 & x_2 - x_1 \end{bmatrix}\begin{bmatrix} \varphi_1 \\ \varphi_2 \\ \varphi_3 \end{bmatrix} \tag{5}$$

where φ_1, φ_2, and φ_3 denote the voltage potential at the mesh nodes P_1, P_2, and P_3, and S denotes the determinant of the transformed triangle's Jacobi matrix (with S representing twice the triangle area size).

As mentioned earlier, we calculate the current density using (2) which can be rewritten as

$$\underline{J} = \frac{1}{R'_{SQ}(T, x, y) \cdot h}(a_1, a_2, 0)^{\mathbf{T}} \tag{6}$$

with $R'_{SQ}(T, x, y)$ representing the effective sheet resistance at temperature T at a specific mesh node (x, y), and h denoting the *smallest* layer thickness (lower-bound height due to process variations). The absolute value $|\underline{J}|$ of the current density J is given by

$$|\underline{J}| = \frac{1}{R'_{SQ}(T, x, y) \cdot h} \cdot \sqrt{a_1^2 + a_2^2}. \tag{7}$$

Hence, we obtain the following *triangle element equations*:

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \frac{1}{k}\begin{bmatrix} -c_1c_1 - d_1d_1 & c_2c_1 + d_2d_1 & c_3c_1 + d_3d_1 \\ c_1c_2 + d_1d_2 & -c_2c_2 - d_2d_2 & -c_3c_2 - d_3d_2 \\ c_1c_3 + d_1d_3 & -c_2c_3 - d_2d_3 & -c_3c_3 - d_3d_3 \end{bmatrix}\begin{bmatrix} \varphi_1 \\ \varphi_2 \\ \varphi_3 \end{bmatrix} \tag{8}$$

with

$$\begin{aligned} \mathrm{k} &= 2 \cdot S \cdot R'_{SQ}(T, x, y) \\ \underline{c} &= (y_3 - y_2, y_3 - y_1, y_1 - y_2)^{\mathbf{T}} \\ \underline{d} &= (x_3 - x_2, x_3 - x_1, x_1 - x_2)^{\mathbf{T}}. \end{aligned} \tag{9}$$

The element equations of all triangles have to be assembled to the *system matrix*

$$\underline{i} = \underline{Y} \cdot \underline{\varphi} \tag{10}$$

where $\underline{\mathbf{Y}}$ is the sparse, diagonal dominant and positive definite conductance matrix. In order to solve (10), the boundary conditions must be applied

$$\underline{i_{\mathbf{BC}}} = \underline{Y} \cdot \underline{\mathbf{E}^{\mathbf{BC}}} \cdot \underline{\varphi}. \tag{11}$$

Here, $\underline{\mathbf{E}^{\mathbf{BC}}}$ is an altered unitary matrix $\underline{\mathbf{E}}$ with all bulk-node elements set to 0. The vector $\underline{i_{\mathrm{BC}}}$ contains all current boundary values of the mesh nodes n, which are linked to the corresponding current-boundary condition. (The current value of a node in $\underline{i_{\mathrm{BC}}}$ not linked to a boundary condition is set to zero.)

Since we assume a homogeneous distribution of the current within the region linked to a boundary condition (segmentation border segments or pin shape), a current share i_n of

$$i_n = \frac{i_{\mathrm{bvalue}}}{m} \tag{12}$$

is applied to each single mesh node n of a given current boundary condition with a boundary value i_{bvalue} (where m represents the number of FEM mesh nodes assigned to this current boundary condition).

Finally, the equation system (11) can be solved with an iterative equation solving method [23]. Several conjugate gradient methods have been tested in order to determine the most preferable one in terms of execution time and memory consumption. Section VIII depicts the results of the conjugated gradient (CG) method and the biconjugated gradient (BiCG) method for different numbers of FEM nodes.

D. Incorporating Thermal Simulation Data

Thermal information needs to be considered at two places. Firstly, current-density calculation is temperature-dependent because a change in temperature influences the gradient of the electrical potential field within the conductor. This is due to the temperature dependency of the electrical conductivity of the metallization material. The electrical potential and the current are linked by electrical conductivity in Ohm's law. Specifically, any variation in the temperature distribution of the circuit (e.g., increased temperature of an electrical device) leads to a change

in the electrical field configuration, which in turn changes the gradient of the electrical potential field $\varphi(x, y)$ and, hence, the calculated current density.

In order to account for the temperature dependency in calculating the current density, we incorporate static thermal simulation data by using a thermal potential field generated during circuit simulation [28]. Specifically, the electrical resistivity ρ in (2) is determined from the effective sheet resistance $R'_{SQ}(T, x, y)$ under consideration of the thermal potential field in order to consider the temperature dependency of the gradient of the electrical potential field $\varphi(x, y)$ in (6), (7), and (9).

Second, the maximum permitted current density of an interconnect varies with the temperature due to the temperature dependency of the electromigration process. While performing current-density verification (see Section VII-A), we take this dependency into account by comparing the calculated current density with a reference current density scaled according to the actual working temperature.

VII. Verification and Visualization of Current Density

A. Current-Density Verification (DRC)

The simple calculation of current density is not sufficient in order to be used as a commercial current-density verification method. A verification method must also take temperature and the characteristics of the process, such as materials of different layers, into account and relate it to the current density that has been calculated. For example, different metallization materials of a given process technology may have different restrictions on their permitted permanent current densities. Furthermore, as already mentioned, the maximum permissible current density of a layer depends on the actual working temperature. Hence, we need to correlate a calculated current density with material characteristics and temperature in order to determine if an actual current-density violation occurs.

Based on Black's law [6] and the requirement of equal lifetimes of wires ($\mathrm{MTTF}(T) = \mathrm{MTTF}(T_{\mathrm{ref}})$) that are exposed to a temperature $T \neq T_{\mathrm{ref}}$, Inequality (13) can be derived. It determines the relation between an acceptable current density $J_{\max}(T)$ at an actual temperature T and a material-dependent maximum current density $J_{\max}(T_{\mathrm{ref}})$ at a given reference temperature T_{ref}

$$|\underline{J}_{\max}(T)| \leq |\underline{J}_{\max}(T_{\mathrm{ref}})| \cdot \exp\left(-\frac{E_a}{n \cdot k \cdot T_{\mathrm{ref}}}\left(1 - \frac{T_{\mathrm{ref}}}{T}\right)\right) \quad (13)$$

where E_a is the experimentally determined activation energy for electromigration failure mechanism ($E_a \approx 0.5 - 1.4\,\mathrm{eV}$), n is set to 2, according to Black's law [6], k is the Boltzmann constant ($k = 1.38 \cdot 10^{-23}\,\mathrm{J/K}$), T_{ref} is the reference temperature (usually $T_{\mathrm{ref}} = 150°\mathrm{C}$), and T is the actual maximum working temperature. For instance, a temperature rise of 25 K in a typical AlSiCu metallization with $E_a = 0.6\,\mathrm{eV}$ and $T_{\mathrm{ref}} = 150°\mathrm{C}$ reduces the permissible current density by about 27%.

We obtain the actual temperature of a layout segment from a thermal potential field calculated for the circuit under working conditions [28]. Current-density violations are determined by incorporating this temperature and the obtained current density into inequality (13) and, hence, comparing the calculated current density with a given material-dependent, maximum permissible current density that is valid at a certain reference temperature.

In order to minimize the number of so-called dummy errors (e.g., resulting from "perfect corners," Section VI-B), verification results must be filtered. Therefore, verification data are linked with the appropriate layout data and evaluated with the following guidelines.

- Given a minimum diameter $d_{\min}$ for *merged* current-density violation spots, all spots with a diameter smaller than $d_{\min}$ are filtered out.
- Given the critical current-density line-length product $(J_{\max} \cdot l_c)$, with l_c representing the so called "Blech length" [7], all two-constraint layout segments with an effective length smaller than l_c are not susceptible to electromigration and, hence, are filtered out.

The remaining verification results are written to a standardized DRC file format that can be used within most commercial DRC result browsers.

B. Current-Density and Voltage Potential Visualization

Visualizing current density and voltage potential requires two modifications while calculating the current density. First, no layout segmentation is performed. (The electrical field configuration would have to be known at the "segmentation borders" prior to segmentation, but this information is not available at the time of segmentation.)

Second, pin current values must be time-dependent in order to allow Kirchhoff's current law to be applied when calculating the current flow. Therefore, the results from one or more simulations of the circuit's netlist are postprocessed by calculating a set of pin current values satisfying Kirchhoff's current law at particular points of time. Specifically, they represent a snapshot of the circuit's operation at the time of minimum and maximum currents *at each pin* (Section V).

The resulting solution vector $\underline{\varphi}$ in (11) can then be used to visualize either the progression of the current density or the voltage potential. Each current-density value or voltage potential value is translated into a color, using a predefined set of visualization colors. (We present some examples in Section VIII-B.)

The current-density view helps to identify inadequate cross-sectional layout structures such as wires, vias, and via arrays. The voltage potential view enables the detection of mismatched nets that have matching requirements, such as connections to differential pairs of transistors.

Additionally, the voltage offset and resistance between two arbitrary points as well as IR-drop can be visualized from the data set.

VIII. Implementation and Results

The described algorithms have been implemented in about 90 000 lines of C++ code and proprietary userware.

An ASCII-based interface reads in layout data (including pin current values) from virtually any layout tool and returns current density data to the layout tool. Our verification method has been extensively tested in commercial analog and mixed-signal designs of various sizes.

TABLE I
COMPARISON OF OUR CURRENT-DENSITY VERIFICATION APPROACH (LABELED CDV) WITH A CONVENTIONAL METHOD BASED ON ANSYS [29]

	FEM Nodes	Verification Time[4] [sec]	Approx. Manual Model Preparation Time [min]	Memory Usage [MByte]
Net_1(CDV)[1]	4,122	2.1	none	2.50
Net_1 (ANSYS)[1,2]	2,889	2.0	10	3.75
Net_1(CDV)[3]	4,856	3.5	none	1.20
Net_1(CDV-M)[3,5]	4,856	1.9	none	1.90
Net_1 (ANSYS)[2,3]	5 x 2,889	5 x 2.0	10	3.75
Heater (CDV)	5,241	3.4	none	3.80
Heater (ANSYS)[2]	3,376	3.3	10	4.20

[1]– Check of one current value at each pin
[2]– Usage of ANSYS shell element 157 and the Frontal Solver
[3]– Check of entire set of pin current values (using layout segmentation)
[4]– Sun-Ultra10, 440 MHz (except CDV-M)
[5]– CDV-M – Multiprocessor option (2 x CPU Sun-Ultra60-450)

All benchmarks reported here were performed on a Sun-Ultra10 workstation with 440 MHz, a Pentium III PC with 650 MHz running Linux and a Sun Ultra60 DP with 450 MHz and two CPUs. Since commercial tools for current verification in arbitrarily shaped metallization patterns do not exist, we compare our automatic methodology with a conventional current-density verification method requiring *manual* layout inspection, *manual* model preparation for assumed critical nets and subsequent current-density calculation (using ANSYS version 5.7 [29]). Table I shows some results in order to compare the overall verification times between the conventional verification method and our approach. (The examples are presented in more detail in the following subsections.) It can be seen that the accuracy of our approach is not inferior compared with a conventional, more time-consuming manual verification method using ANSYS, providing at the same time a fully automated methodology by not requiring any specific model preparation. Furthermore, our methodology avoids manually mapping current density and temperature data to specific DRC errors as required in any manual approach.

The verification results of a complex, commercial analog IC (10 345 nets including 6211 current-density critical nets, 43 hierarchy cells) are presented in Table II. (Please note that it is impossible to *manually* verify current density of analog layouts of such complexity.) The presented results clearly demonstrate the impact of layout segmentation in reducing verification time and minimizing memory consumption due to the significantly reduced numbers of FEM nodes per segment. (In our example, a tenfold increase in the number of FEM nodes per segment roughly translates into a 31-fold increase in verification time and a 13-fold increase in memory consumption, see also Table III.) Based on the independence of each layout segment, even more time-efficient full-chip verification can be achieved by using multiprocessor systems or clusters of workstations.

Several types of iterative CG solvers have been tested in order to determine the solver with the best fitting properties for our problem. Table III and Fig. 8 show the results for CG and BiCG solvers. Both solvers show an almost linear relation between the number of FEM nodes, required iterations, and memory consumption with the CG solver clearly outperforming the BiCG solver regarding runtime and memory consumption.

TABLE II
IMPACT OF LAYOUT SEGMENTATION ON VERIFICATION TIME AND MEMORY CONSUMPTION OF A COMMERCIAL ANALOG CHIP

	No Layout Segmentation	With Layout Segmentation
Segments to Check[2]	2 x 6,211	45,247
Average Number of FEM Nodes per Segment	11,347	2,721
Verification Time[1] [h:min:sec]	47:12:54	13:21:57
Peak Memory Consumption [MByte]	178.89	70.24

[1]– Pentium III, 650 MHz, 512 MByte RAM, Linux Kernel 2.4.18
[2]– Every net must be checked twice without layout segmentation (lower and upper current bound)

TABLE III
COMPARISON OF CONJUGATED GRADIENT (CG) SOLVER AND BICONJUGATED GRADIENT (BICG) SOLVER

FEM Nodes	Run Time[1] [sec]		Iterations[2]		Memory Usage [MByte][3]	
	CG	BiCG	CG	BiCG	CG	BiCG
1,955	< 1	< 1	244	238	0.48	0.53
6,171	2	5	456	458	1.54	1.72
11,902	10	21	636	635	2.93	3.67
25,412	39	72	940	940	5.87	6.64
58,346	139	256	1,448	1,443	12.24	14.03
87,682	259	492	1,779	1,779	17.60	20.98
173,616	718	1,376	2,506	2,505	35.19	42.08
347,297	2,079	4,056	3,579	3,578	69.62	83.61
863,403	8,134	16,122	5,655	5,653	155.52	188.65

[1]– Pentium III, 650 MHz, 512 MByte RAM, Linux Kernel 2.4.18
[2]– Break condition was set to a maximum error of $\|\varphi^{(n)}\| \leq \pm 10^{-6}$ (n = number of iterations) during iterative solving of Equation (11)
[3]– Presented memory consumption considers only the memory consumption of the equation system solver and hence, is smaller than in Table I for the same number of FEM nodes.

A. Example of Current-Density Verification (DRC)

During current-density verification, the current-density violations are written to a standardized DRC file format and are visualized in a DRC file browser [Fig. 9(a)]. The violation level expressed in the DRC file (e.g., “>=20%, <50%”) can then be used to guide the subsequent wire and/or via sizing [Fig. 9(b)].

B. Examples of Current-Density Visualization

In the following, examples of current-density *visualization* are presented. (As outlined in Section VII, the visualized current densities must be compared with the maximum permissible current density of the layer material under consideration of the working temperature in order to determine actual current-density violations. Furthermore, current-density visualization re-

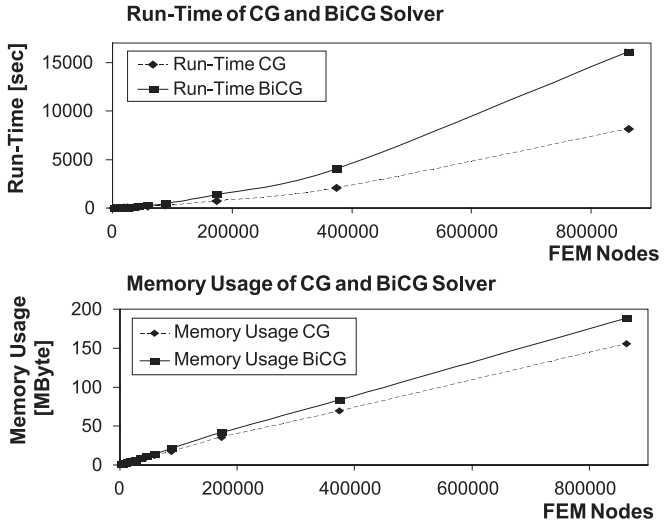

Fig. 8. Graphical comparison of CG solver (dashed line) and BiCG solver (solid line) in terms of CPU run time and memory consumption based on values of Table III.

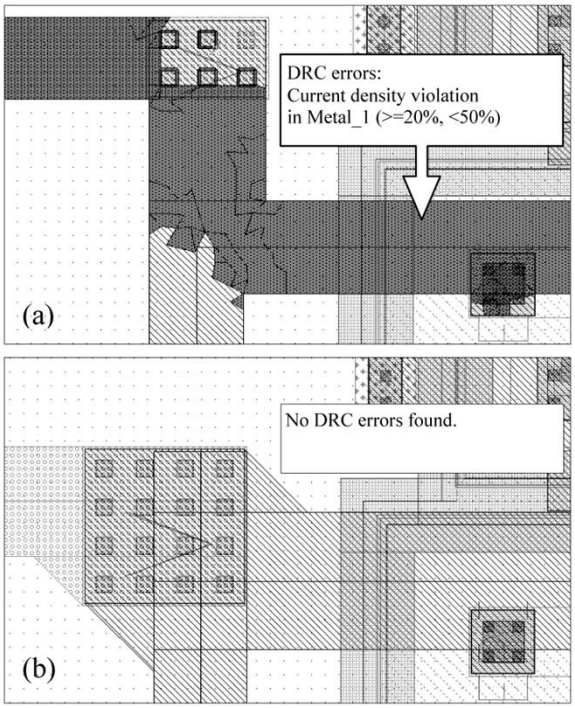

Fig. 9. (a) Excerpt of a current-density verification layout with a flagged violation area marked in dark grey. (b) Using the provided violation data, appropriate wire and via sizing delivers a current-density-correct layout.

quires time-dependent current values that obey Kirchhoff's current law at a specific point of time.)

1) Net With Via Arrays: Fig. 10 depicts an *excerpt* of Net_1 (Table I) laid out in three metallization layers. The color assignment of layer Metal_1 as well as within a tongue in layer Metal_2 exposes areas of high current density. The zoomed view of layer Metal_1 shows increased current density stress at the edges of the Metal_1 to Metal_2 vias, indicating a via array with an inappropriate layout.

2) Different Corner Bend Angles (Roundings): Any corner is a natural obstacle for a current flow. Electrons follow the least resistance path and, hence, are "jammed" close to a corner leading to a high current density at this point. Corners with bend angles larger than 90° enable a more homogeneous current flow due to their greater *effective* wire cross section area compared to 90° corners. Fig. 11 shows current-density visualization of different bend angles (90°, 135°, 150°) indicating the need for avoiding 90° corners in layouts with higher currents.

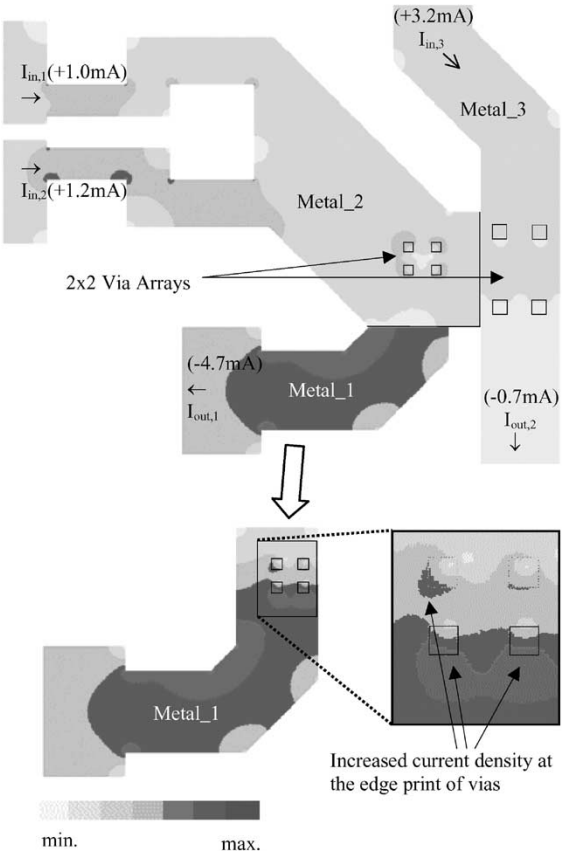

Fig. 10. Excerpt from current-density visualization of a net covering three layers. Areas of high current density (darker colors) are visible in layer Metal_1 and at corners of the Metal_2 shape. The enlarged view of the Metal_1 shape shows the current-density stress print of the via edges in the 2 × 2 via array.

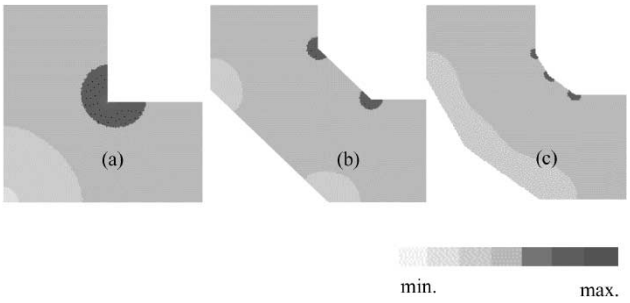

Fig. 11. Current-density visualization of different corner bend angles of (a) 90°, (b) 135°, and (c) 150°.

3) Via Example: Our methodology of modeling vias using "honeycomb"-like structures enables a detailed current-density verification at different "cut lines" of a via. Specifically, via layers that are normally invisible in conventional verification methods might carry excessive current densities that need to be analyzed in detail in order to prevent via degradation by electromigration (Fig. 12).

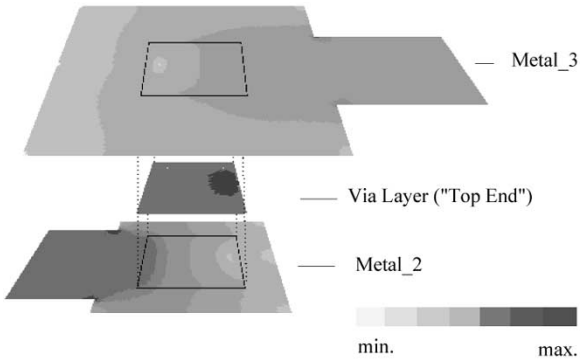

Fig. 12. Quasi-3D current-density visualization in a Metal_2 to Metal_3 via driven by an interconnect with increased current density. Please note that the via layer can be analyzed at both the top and the bottom end. In this example, the top surface of the via layer (adjacent to Metal_3) is depicted, showing an excessive current density on the side of the outgoing current.

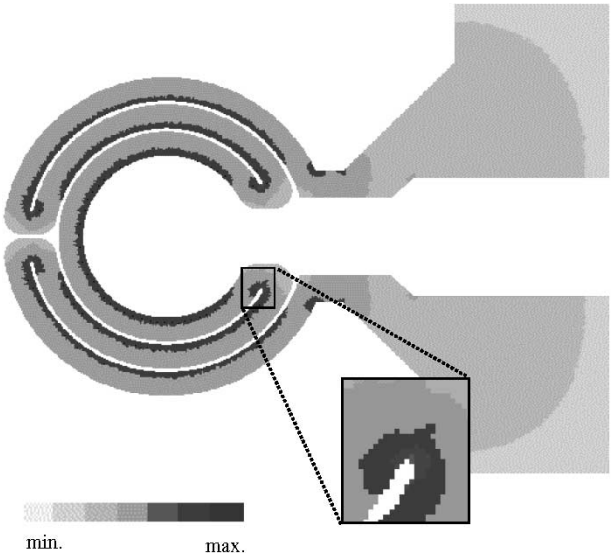

Fig. 13. Part of a heater segment with an excessive current density at the bends of the ring elements.

4) Heater Segment of a Sensor: In addition to current-density verification of on-chip interconnects, the developed verification tool can also be used for "non-IC" applications with arbitrarily shaped metallization patterns, such as various MEMS structures. A heater structure ("Heater" in Table I) as part of a sensor device is depicted in Fig. 13. Increased current-density stress is clearly visible at the inner edges of the ring elements while some outer parts barely carry any current at all. As a result of this current-density investigation, the layout of the heater segment was modified, resulting in significantly less current-density stress.

IX. Limitations

As mentioned before, *any* layout structure can be verified with our methodology with *any* desired resolution. However, the use of the FEM for current-density calculation might be computationally too expensive for the verification of *digital* nets in multimillion gate designs. A simpler approach tailored for digital nets that models all wire segments as homogeneous path elements with a constant width would certainly perform much faster without losing too much verification precision.

The modeling of via roundings in deep submicron designs has not yet been considered during layout preparation and subsequent current-density calculation. As stated before, the artificially increased current density at a perfect corner without any rounding is filtered out in order to prevent so-called dummy errors. Further research is required here in order to improve the proposed filter strategy which provides an effective, yet for some cases too simple approach.

The described algorithm does not account for self-heating within wire segments due to Joule heating. Our experimental investigations and theoretical research in [11] have shown no significant temperature rise for typical current densities up to $2\ \mathrm{mA}/\mu\mathrm{m}^2$. Therefore, we assume no significant self-induced temperature gradients that may influence the material migration process.

The proposed current-characterization method is well suited for reliability-oriented chip designs (such as those commonly used in automotive applications), but it can promote excessive wire and via widths in less critical applications. For that reason, current values obtained only by simulation with typical input stimuli should be used in volume production chips (rather than using library-based values).

The application of boundary constraints for any net pin is assumed to be homogeneous in (12). This approach might be too simplistic for large-sized pins (e.g., pins of large DMOS transistors) due to nonhomogeneous electrical field configurations in diffusion areas. In this case, a device simulation is required in order to obtain the nonhomogeneous distribution of current shares at these pins.

Our methodology has been especially tailored for analog circuits and analog blocks in mixed-signal ICs and, hence, does not consider influences of effective transistor and wiring capacitances or inductances that exist with fast switching currents in mainly digital designs. Additionally, the skin effect (which reduces the effective cross section area in very fast switching nets with large cross section areas) has not been considered here.

X. Conclusion

We presented a new current-density verification method that has been developed in order to cope with the steadily increasing problems of high current-density stress in modern integrated circuits. Our methodology allows for the first time an automatic, time-and memory-efficient verification of current densities in arbitrarily shaped layouts. We also address the temperature dependency of permissible current density stress by incorporating thermal simulation data into our calculation and verification method. The presented methodology has been extensively verified in commercial design flows thereby leading to significantly shorter development times in combination with more reliable electronic devices.

Our future work will concentrate on further reducing the discussed limitations of our verification methodology. Furthermore, the experience gained with the current-density verification tool underlines the urgent need for commercially available current-driven routing and verification methodologies.

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