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RESEARCH-ARTICLE

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PDF Download
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01 April 2026
Total Citations: 0
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Published: 27 March 2026

Citation in BibTeX format

ISPD '26: International Symposium on Physical Design
March 15 - 18, 2026
Bonn, Germany

Conference Sponsors:
SIGDA

ISPD '26: Proceedings of the 2026 International Symposium on Physical Design (March 2026)
https://doi.org/10.1145/3764386.3779613
ISBN: 9798400723148

Invited: From Evolutionary Algorithms to Analog Design, Electromigration, 3D Integration, and Beyond: On Jens Lienig's Contributions to Advance Physical Design

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Abstract

The 2026 International Symposium on Physical Design (ISPD) honors Jens Lienig with the Lifetime Achievement Award, recognizing his multi-decade impact on physical design automation, education, and professional service. While the semiconductor industry has relentlessly pursued power, performance, and area scaling, Lienig's research has consistently highlighted a fourth, critical dimension: *robustness and reliability*. This paper reviews the trajectory of his contributions, beginning with foundational work on evolutionary algorithms for routing in the 1990s, moving through the rigorous automation of analog constraint handling, and culminating in his pioneering research on electromigration-aware physical design. We further examine his contributions for automating physical design for 3D integration, in particular handling thermal and mechanical challenges, and his recent collaborations to establish security as an emerging physical design objective. Beyond his technical achievements, this paper acknowledges his profound influence as an educator, whose textbooks and curriculum reforms have bridged the gap between theoretical algorithms and industrial reality for a generation of engineers.

CCS Concepts

• **Hardware** → **Physical design (EDA)**; **Wire routing**; **Reliability and testing**; *Analog and mixed-signal circuits*; *3D integrated circuits*; • **Security and privacy** → *Hardware security*.

Keywords

Physical Design, Evolutionary Algorithms, Analog IC Design, Electromigration, Reliability, 3D Integration, Hardware Security

ACM Reference Format:
Johann Knechtel, Susann Rothe, Robert Fischbach, Matthias Thiele, Tilo Meister, and Andreas Krinke. 2026. Invited: From Evolutionary Algorithms to Analog Design, Electromigration, 3D Integration, and Beyond: On Jens Lienig's Contributions to Advance Physical Design. In *Proceedings of the 2026 International Symposium on Physical Design (ISPD '26), March 15–18, 2026, Bonn, Germany*. ACM, New York, NY, USA, 10 pages. https://doi.org/10.1145/3764386.3779613

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ISPD '26, Bonn, Germany
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ACM ISBN 979-8-4007-2314-8/2026/03
https://doi.org/10.1145/3764386.3779613

1 Introduction

The ISPD Lifetime Achievement Award is reserved for individuals who have fundamentally shaped the field of physical design through outstanding research, education, and service. Following distinguished recipients such as Ernest Kuh, C.-L. Liu, and Jason Cong, the 2026 symposium pays tribute to Professor Jens Lienig. His career is distinguished not only by the breadth of his technical contributions – ranging from bio-inspired algorithms to 3D integration and beyond – but also by a unifying philosophy: the insistence that physical design must ensure reliability alongside functionality.

1.1 Biographical Sketch

Jens Lienig's academic journey began at the Dresden University of Technology (TU Dresden), where he received his M.Sc. (Diploma), Ph.D. (Dr.-Ing.), and Habilitation degrees in 1988, 1991, and 1996, respectively. His early research career was characterized by a distinct international perspective; he served as a Postdoctoral Fellow at Concordia University in Montréal, Canada (1991–1994), and subsequently as a Visiting Assistant Professor at the University of Virginia in Charlottesville (1994–1996).

Crucially, Lienig's academic rigor is informed by significant industrial experience. From 1996 to 1999, he worked with Tanner Research Inc. in Pasadena, CA, and later served as a Tool Manager at Robert Bosch GmbH in Reutlingen, Germany, from 1999 to 2002. This exposure to the practical realities of automotive and commercial IC design deeply influenced his later research, grounding his algorithmic solutions in the physical constraints of manufacturing realities. Since 2002, he has served as a Full Professor and the Director of the Institute of Electromechanical and Electronic Design (IFTE) at TU Dresden, where he has cultivated a research environment that merges computer science algorithms with electromechanical engineering fundamentals. He is a Senior Member of the IEEE and has served on the Technical Program Committees of DATE, SLIP, and ISPD, including as General Chair of ISPD 2021.

1.2 Paper Organization

This paper serves as a retrospective on Lienig's scientific contributions, organized by the major technical domains he has advanced. It is designed to provide a technical survey of his joint works and the evolution of his research group. Readers may also look to the complementary contribution by Professor Andrew Kahng in this session, which is expected to offer further perspectives on Lienig's early work in metaheuristics and his foundational textbooks.

The remainder of this paper is organized as follows: Section 2 reviews his early work on applying evolutionary and genetic algorithms to the NP-hard problems of channel and switchbox routing. Section 3 discusses his pivot to analog design automation, specifically the shift from schematic-driven to constraint-driven layouts. Section 4 details his perhaps most recognized contribution: the development of electromigration-aware physical design flows that replace pessimistic current limits with physics-based reliability models. Section 5 examines his solutions for 3D integration, focusing on thermal management and floorplanning. Section 6 explores his current research frontiers, including hardware security and optical computing. Finally, Section 7 highlights his legacy as an educator and author of standard textbooks that define the modern physical design curriculum.

2 Evolutionary Algorithms

Jens Lienig dedicated the first decade of his scientific career to the application of nature-inspired optimization techniques to physical design [41]. In the 1990s, as the complexity of integrated circuits (ICs) began to challenge traditional deterministic routing algorithms, Lienig investigated evolutionary algorithms (EAs), specifically genetic algorithms (GAs), as a robust alternative for solving NP-hard routing problems.

His research in this field, outlined in this section, established foundational methodologies for applying these stochastic processes to detailed routing tasks, such as channel and switchbox routing, while simultaneously addressing the high computational costs associated with EAs through novel parallelization strategies.

2.1 Genetic Algorithms for Routing

A central contribution was the development of *GASBOR* (Genetic Algorithm for Switchbox Routing) [59, 60]. Lienig demonstrated that GAs could effectively navigate the immense search space of detailed-routing configurations to identify near-optimal solutions where constructive heuristics often struggled. He subsequently extended these algorithms to handle performance-driven constraints, integrating crosstalk minimization directly into the routing objectives early on [43]. This work highlighted the flexibility of EAs in handling multi-objective optimization problems, a theme that would recur in his later works on 3D floorplanning (Section 5). Furthermore, he applied these strategies to the routing of multichip modules (MCMs) [48], a precursor to the modern advanced packaging technologies tackled in his later works as well (Section 5).

2.2 Parallelism and Island Models

While GAs offered high-quality solutions, their runtime posed a significant bottleneck for practical VLSI design cycles. To overcome this, Lienig extensively researched parallelization strategies, focusing on distributed genetic algorithms and specifically the coarse-grained "island model" approach [62]. In this approach, based on the biological theory of punctuated equilibria, the population is divided into subpopulations (islands) that evolve independently and periodically exchange individuals (migration). His research demonstrated that this topology not only accelerated convergence via parallel processing but also preserved genetic diversity, preventing premature convergence to local optima [42, 44]. These works provided a framework for scalable, performance-driven routing capable of leveraging parallel computing architectures [51].

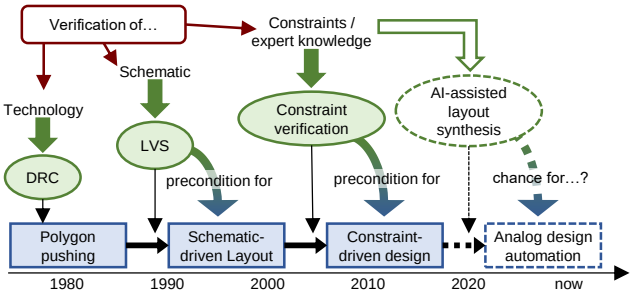

Figure 1: History and future of analog physical design methodologies (cf. [74]).

3 Analog IC Design

Around 2001, Jens Lienig extended his focus to analog circuit design. In parallel with his research on current-driven routing to avoid electromigration (Section 4), he also investigated the fundamental reasons why automating analog design remains notably more challenging than digital design. He identified the multitude and heterogeneous nature of design constraints as a primary cause.

To solve this challenge, he and Göran Jerke proposed a paradigm shift from schematic-driven layout (SDL) to constraint-driven design [18], which has since been partially implemented in commercial tools for electronic design automation (EDA). Figure 1 shows this evolution of design methods for analog ICs. This section details constraint propagation as a cornerstone of this flow, followed by a discussion on the group's recent initiatives in open-source EDA for analog design.

3.1 Constraint Propagation

A comprehensive constraint-driven design flow involves several key aspects that need to be examined, including

- a formal constraint definition [37],
- constraint management [38], especially constraint propagation [36],
- data modeling [35], and
- constraint verification and budget calculation [34].

Constraints are requirements for the values of design parameters that must be met before tape-out. Each constraint belongs to a specific cell that provides its context and must be fulfilled for the context cell itself and for all its instances in the design. Each constraint applies to a set of design elements, which can be its context

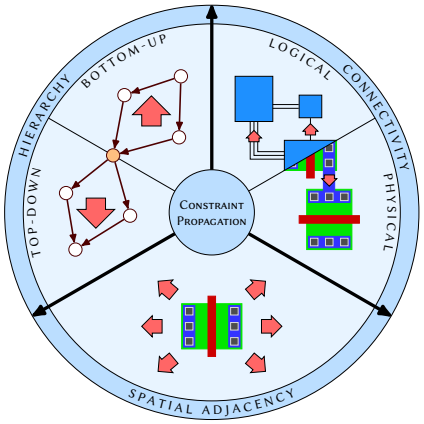

Figure 2: Classification of propagation types. Constraints can be propagated using a combination of these methods [36].

cell, instances, or nets. Since the context cell anchors a constraint in the design hierarchy, these members are always defined with a path relative to the context cell. In such a context, constraints can be described as functions that associate design parameters of members with a Boolean value that represents the constraint's state (fulfilled or violated).

For a constraint-driven design flow, constraints should be visible and verifiable in all cells where a designer can influence their state. The primary goal of *constraint propagation* is to identify all cells that are relevant to a constraint and subsequently instantiate propagated constraints within these cells. For each instance of a constraint's context cell and for each associated design parameter, a propagation tree is created that captures all corresponding relevant cells. A key insight by Jens Lienig and colleagues was that there is a small, fundamental set of five different types of propagation, despite the possibility of defining arbitrarily complex constraint functions.

Figure 2 provides an overview of these propagation types. They describe how design parameters influence the set of relevant cells, which is a key component of constraint propagation.

3.2 Open-Source EDA

In recent years, both analog and digital design domains have witnessed a rapid and synergistic development of open-source EDA tools (e.g., [1, 30, 61, 68]), open process design kits (OpenPDKs, e.g., [10, 15, 76]), and open-source designs. A primary goal of this trend is to lower the barrier to entry for small businesses and start-ups by eliminating licensing costs. Perhaps even more critical, however, is the reduced dependence on major EDA tool providers and the standardization of design data, which significantly facilitates the exchange of research results.

A major challenge for every new OpenPDK is that the layout rules of the underlying process are often available only in proprietary formats. To enable layout verification steps, such as design rule checks (DRC) and layout-versus-schematic checks (LVS), complex scripts must be created for open-source tools. A significant contribution by Lienig's group to this ecosystem is the automated generation of verification runsets for the open-source layout editor KLayout. The developed framework utilizes an input format

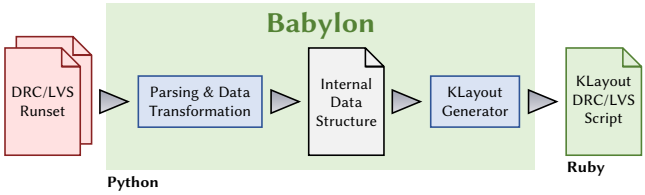

Figure 3: Generation of DRC and LVS commands for the open-source layout editor KLayout [33].

based on the KLayout DRC API, extended to support methods with additional parameters or entirely new commands.

Figure 3 illustrates the workflow for generating these DRC and LVS runsets [33]. The scripts are generated by topologically sorting and translating complex operations, allowing them to be executed directly within KLayout. Currently, Lienig's group is formalizing and expanding this input description into a comprehensive open format designed to enable tasks such as automated generation of layout manuals, along with executable verification decks.

4 Electromigration-Aware Physical Design

Jens Lienig started his work in the field of electromigration (EM) in the industry, at the Robert Bosch GmbH in Reutlingen, and continues his research on this increasingly pressing reliability issue at TU Dresden to this day [45, 46, 54]. This section covers his contributions to the tremendous development that EM-aware physical design has undergone in the last 25 years.

4.1 EM-Aware Analog Design Automation

At the beginning of the 21st century, the impact of EM on the reliability of analog circuits grew, yet industry lacked suitable design strategies to ensure EM robustness. While there was experience with current-driven routing of power and ground networks, analog circuits are more complex to design – automating this process remains an open challenge.

Thus, EM as a routing constraint presented significant algorithmic hurdles. Specifically, as shown in Fig. 4, the following steps were researched and developed by Lienig's group to be integrated into the analog design flow in order to achieve EM awareness:

- terminal current determination [19, 54],
- current-driven wire planning [53],
- hierarchical current-density verification of arbitrary routing polygons [16], and
- current-driven interconnect post-processing and layout decompaction [20].

Since their publication, these techniques have become industry standards; notably, current-density verification endures as the most common verification approach. All of these steps were integrated into commercial design flows and could be used with established tool chains [17]. They have been validated by applying them to industry-scale designs. This shows that these works not only held significant scientific value but also offered direct benefits to industry and the physical design community.

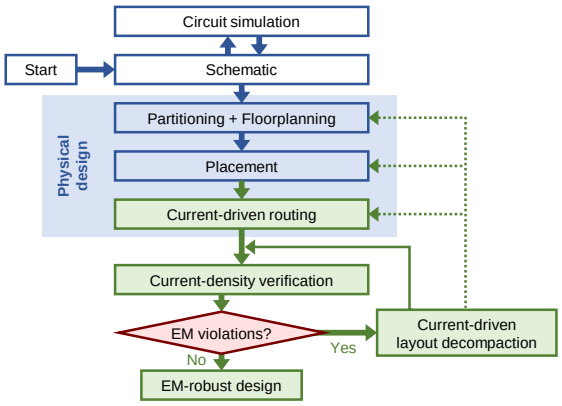

Figure 4: EM-aware design flow with the proposed methods, applicable for analog and mixed-signal ICs.

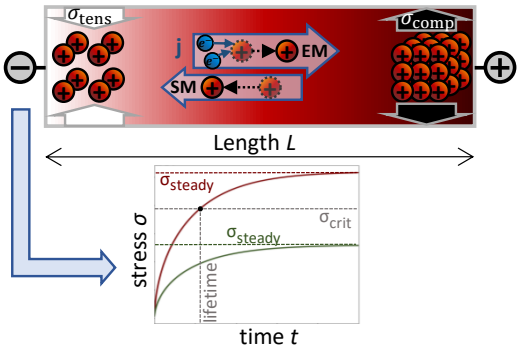

Figure 5: The principle of stress evolution driven by EM [54].

4.2 Advancing EM Robustness: Countermeasures and Modeling

With technology scaling, EM became an increasingly problematic reliability concern [58]. While interconnects became more vulnerable to high current densities, the currents did not scale as strongly as the interconnect cross-sections. Thus, the current densities in the designs were rising, while their limits were shrinking. The remaining design space diminished with each new semiconductor technology. Roadmaps like the International Technology Roadmap for Semiconductors (ITRS) predicted this trend would continue, emphasizing the need for innovative approaches to handle EM.

4.2.1 EM Countermeasures. There are numerous known EM countermeasures that can be applied to increase the EM robustness at the layout design stage. Specifically, designers can make use of cathode reservoirs, via-below configurations, short-length effects, and/or redundant vias [3]. Additionally, knowledge of the material properties can help improve the layout, e.g., by leveraging the bamboo effect. To successfully apply these measures and to quantify their impact on EM robustness, the underlying mechanisms were explored and, based on these insights, design guidelines have been formulated by Lienig and colleagues [54].

4.2.2 Physics-Based Modeling. As standard current-density verification proved overly pessimistic – unnecessarily restricting design freedom – the research community shifted focus toward novel physics-based EM models. The notion of *hydrostatic stress* replaced current density as the measure for EM robustness. Physics-based models describe the stress that builds up in an interconnect due to EM and other migration mechanisms, i.e., stress migration (SM) and thermal migration (TM).

Figure 5 shows the principle of stress evolution driven by EM. Specifically, the stress building up causes SM as a counteracting force; EM and SM will eventually reach an equilibrium, the so-called *steady-state stress*. If the steady-state stress does not exceed the critical stress for failure, the wire can be considered immortal. Otherwise, the moment when the critical stress is reached can be understood as the lifetime of the wire.

Physics-based modeling offers the advantage that EM risks in general multi-segment interconnects can be precisely evaluated; both immortality assessment and lifetime estimation are possible. A net is not only assessed as violated or robust, but designers also gain insights into which parts of the interconnects experience the highest EM risk and, thus, where exactly EM countermeasures must be applied. This significantly increases the locally allowed current density, thus relaxing the strict global current-density limits that are in place today.

However, applying these models in the design flow comes with multiple challenges. For example, fast verification schemes for full-chip EM assessment had to be developed [4]. Moreover, the impact of the migration mechanisms and material properties on stress evolution and circuit reliability had to be evaluated [72].

4.3 Proactive EM-Aware Routing

While technology improvements increased the inherent EM robustness of interconnects, it was not readily clear whether this would suffice to face the growing reliability concerns. In that situation, there was a need for completely new ideas on how to handle EM-aware IC design – the established post-layout verification approach resulted in a growing number of detected EM violations and, thus, required time-consuming repair steps.

The design flow shown in Fig. 4 already includes an EM-aware routing step. This idea has been revisited and adapted to the needs of new technology nodes and digital signal routing [4]. Such *proactive* EM routing was tailored for digital signal nets. While individual nets have a relatively low EM risk, the sheer number of millions of nets in industrial designs along with their highly optimized routing made an automated EM-aware routing flow inevitable.

The successfully developed, proactive EM-robust design flow shown in Fig. 6 includes an EM-driven net ordering to ensure that there are enough routing resources for EM-critical nets and necessary countermeasures. The flow also incorporates a fast and efficient steady-state analysis of all nets to evaluate their EM-robustness and need for implementing EM countermeasures. Net topology management helps to minimize the EM risk of the net by keeping segments stressed with high current density short. For nets that require EM countermeasures, dedicated algorithms for their efficient implementation are in place.

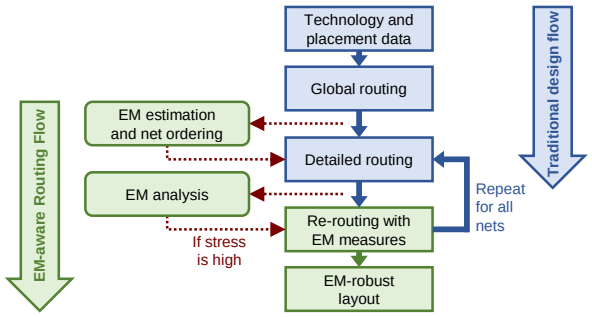

Figure 6: Proactive EM-aware design flow for signal nets [4].

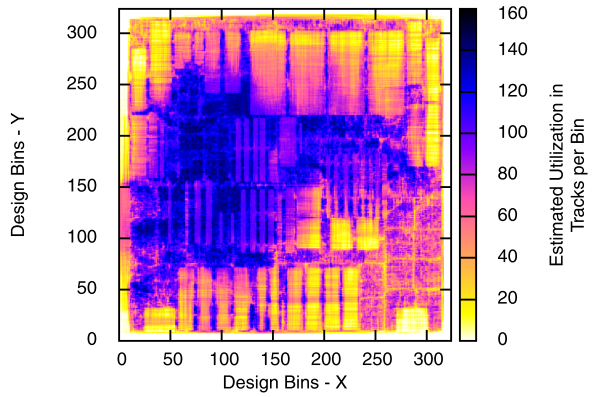

Figure 7: Predicted routing utilization for the design *adaptec1* of the ISPD global routing benchmark suite [65, 67]. Copyright IEEE 2011. Used with permission from [65].

4.4 From Theory to Practice: Applying Physics-Based Models

Although physics-based modeling has dominated the research field for a decade, it still did not find its way into industrial design practice. This is because adopting these benefits requires overcoming major practical obstacles. First, regular EDA tool chains do not offer convenient integration of physics-based EM verification. However, there are academic tools and publicly available finite-element method (FEM) models [72] that could be applied with some tooling effort. Also, recent works utilize the analogy/mapping between migration-induced stress evolution and equivalent RC networks. Those RC circuits can be efficiently solved using SPICE, to accurately simulate stress evolution driven by EM, SM, and TM in interconnects [73]. Second, there are no established methods to experimentally characterize a semiconductor technology to find the modeling parameters for stress evolution. Recent efforts to fill this gap include an interpolation method based on standard EM lifetime tests [73].

Currently, Lienig and his group closely collaborate with multiple industry partners to validate the known approaches for parameter characterization and, at the same time, experimentally explore the physics-based migration models and their practical applicability and potential limitations. These collaborations aim to transfer the knowledge and insights that researchers gained in the field of physics-based modeling into industry.

5 3D Integration and Packaging-Aware Design

With Moore's Law recently shifting toward both "More Moore" (further scaling) and "More than Moore" (system-level diversification), integration density increases not only on the chip but also on the package level. Throughout the past 20 years, Jens Lienig fostered research and development in chip-level EDA. This transition was driven by the industry's need for diversification through heterogeneous system integration, where an interposer serves as a unifying integration backbone for both legacy 2D chips and customized 3D components [22, 27].

Early works in Lienig's group focused on chip-level pin assignment and routability evaluation, followed by floorplanning for 2.5 and 3D ICs. Specialized data structures were developed to make the design space accessible to EDA algorithms. Over time, this experience enabled the demonstration of EDA tools applicable to modern packaging problems including micro-transfer printing. This section outlines works by Lienig and his group in this field.

5.1 Pin Assignment and Routability Evaluation

The increasing integration densities on all system levels from the chip across the package down to the board required hierarchical co-design strategies. An important aspect of these strategies is the simultaneous optimization of the interfaces between all hierarchy levels. This has been necessary to overcome routing and performance bottlenecks. Lienig's research group successfully developed a set of optimization algorithms for pin assignment [63]. They were demonstrated to minimize routing congestion and thus maximize system performance by implementing them in a real-world industrial design flow. To enable this real-world application, the group also developed methods to universally handle the special requirements of differential pairs regarding signal integrity [64].

A crucial underlying advancement for pin assignment optimization was the development of fast and comprehensive methods to evaluate overall routability in heterogeneous systems. The group achieved this by developing probabilistic routing models and by combining them with efficient, real-world based heuristics [65]. Figure 7 shows a routing utilization prediction generated by applying these models to a chip design from the ISPD global routing benchmark suite from 2008. Ultimately, these new means for routability predictions enabled efficient global interface optimizations that outperformed earlier global-routing-based approaches. These underlying probabilistic models are highly flexible, and the group was also able to expand them from their original hierarchical 2-dimensional use case to efficiently deliver blockage-aware 3D-routing predictions [7]. Notably, all these optimization and prediction techniques predate the use of machine learning, further emphasizing their inherent accuracy and efficiency.

5.2 Data Structures and Floorplanning

In order to represent and modify a geometrical layout of rectangular and/or rectilinear blocks computationally, a multitude of different layout representations evolved in our field. Traditionally, they are

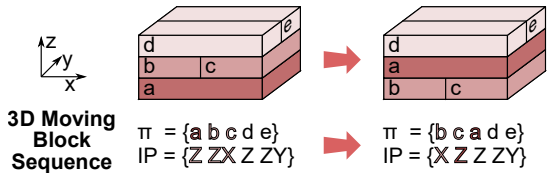

Figure 8: The 3D-MBS data structure represents a 3D layout by two sequences which can be altered, e.g., to exchange block a with blocks b and c as shown here [6].

simplified to flat (2D) shapes. However, with the advent of 3D integration, several of them were adapted to enable layered 2.5D or native 3D blocks. Thus, Lienig's group carried out a thorough evaluation to identify which representation could be applied for which use-cases, as they all differ in capabilities and runtime behavior [8].

Based on these efforts and insights, they next developed a new 3D layout representation illustrated in Figure 8. The *3D Moving Block Sequence (3D-MBS)* was inspired by the main features of the traditional MBS. In order to address the continuous 3D space, the constructive block insertion process was extended accordingly. Furthermore, orthogonal polyhedra and efficient collision detection were introduced. Like the original MBS, the 3D-MBS is a non-slicing, packing representation. Various case studies confirmed the efficiency of the proposed 3D-MBS data structure [6].

Subsequently, research efforts in Lienig's group shifted toward multiobjective optimization. One proposed methodology, *MoDo*, simultaneously optimizes interconnects, voltage drop, clock-tree size, and maximum temperature by improving deadspace distribution [26]. To further improve design closure, the group facilitated the reuse of existing 2D IP blocks by clustering through-silicon vias (TSVs) in the deadspace between blocks [24, 25]. This approach was extended by *Corblivar*, a floorplanning methodology with a novel alignment concept designed to plan massive interconnect structures, such as large vertical buses and TSV stacks, across multiple dies [28, 29]. Recent work further refined these concepts by introducing parallel branch-and-bound techniques for optimal die placement on interposers, significantly outperforming prior art in solution quality and scaling up to many more dies [69]. To further reduce power consumption and thermal footprints, the group integrated voltage assignment directly into the 3D floorplanning loop, enabling effective trade-offs between performance and power [23].

5.3 WaferPlanner for Micro-Transfer Printing

The group's extensive experience with 3D integration and packaging-aware design recently culminated in *WaferPlanner*, an EDA demonstrator for micro-transfer printing, an emerging integration technology. Figure 9 illustrates the micro-transfer printing process.

The primary challenge lay in managing new cross-die layout dependencies, specifically the constraints induced by the elastomer stamp, which enforces compatible layouts at the wafer level – a consideration that is out-of-scope during chip design. Furthermore, the decision where the source dies (chiplets) are printed on the target die has a strong impact on the achievable utilization and yield at the wafer level. Thus, in order to evaluate a given layout,

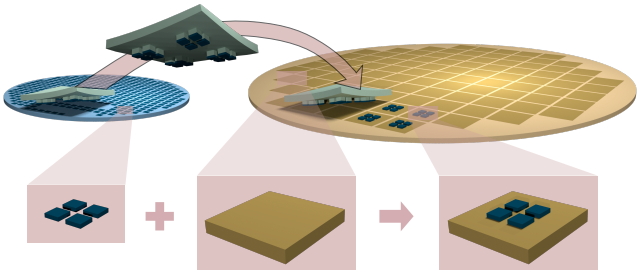

Figure 9: Visualization of the micro-transfer printing process. An elastomer stamp transfers dies originating from a source wafer (left) onto a target wafer (right) to create heterogeneous chip stacks [5].

post-layout steps such as mask tooling and the printing process had to be holistically considered [5].

6 Beyond

While the previous sections covered Jens Lienig's foundational contributions to established domains of physical design, he and his research group continue to address the frontiers of emerging topics and technologies, as outlined in this section.

6.1 Hardware Security

Following their extensive research into reliability, around 2020, Lienig and his group extended their collaboration with Johann Knechtel and others to the field of hardware security [55, 81]. This work established the paradigm of *security closure of physical layouts*, which advocates for the formal assessment and hardening of layout-level artifacts against malicious exploitation [55]. This approach, also outlined in Fig. 10, treats physical effects as potential attack surfaces that must be addressed within the CAD flow to prevent the subtle exploitation of related reliability mechanisms [54, 55, 73].

6.1.1 Migration-Effects-Based Trojans. A significant focus of this collaboration has been the identification of migration-effects-based Trojans [55]. Unlike traditional logic-based modifications, these are zero-gate implementations that reside entirely within interconnects, rendering them invisible to gate-level netlist inspection as well as inspection of front-end-of-line layers. These stealthy modifications weaponize physical phenomena such as EM, TM, and SM, all to induce delayed failures in critical signals or power delivery networks [55, 81]. For example, their research showed that, by shifting via configurations from upstream to downstream or removing cathode reservoirs, an adversary can drastically reduce the mean time to failure of an interconnect while ensuring the Trojan remains inactive during initial post-silicon testing [55, 73]. Such risks call for more thorough post-silicon inspection and assurance.

6.1.2 Risks in Advanced Packaging. The collaboration recently extended this threat model to advanced packaging, specifically CoWoS interposer systems [81]. This research revealed that Trojans can be strategically placed to "lurk in the shadows" of imaging artifacts caused by established X-ray inspections. The team proved that specifically designed modifications can remain concealed in over 88% of X-ray exposures, even under idealized detection conditions.

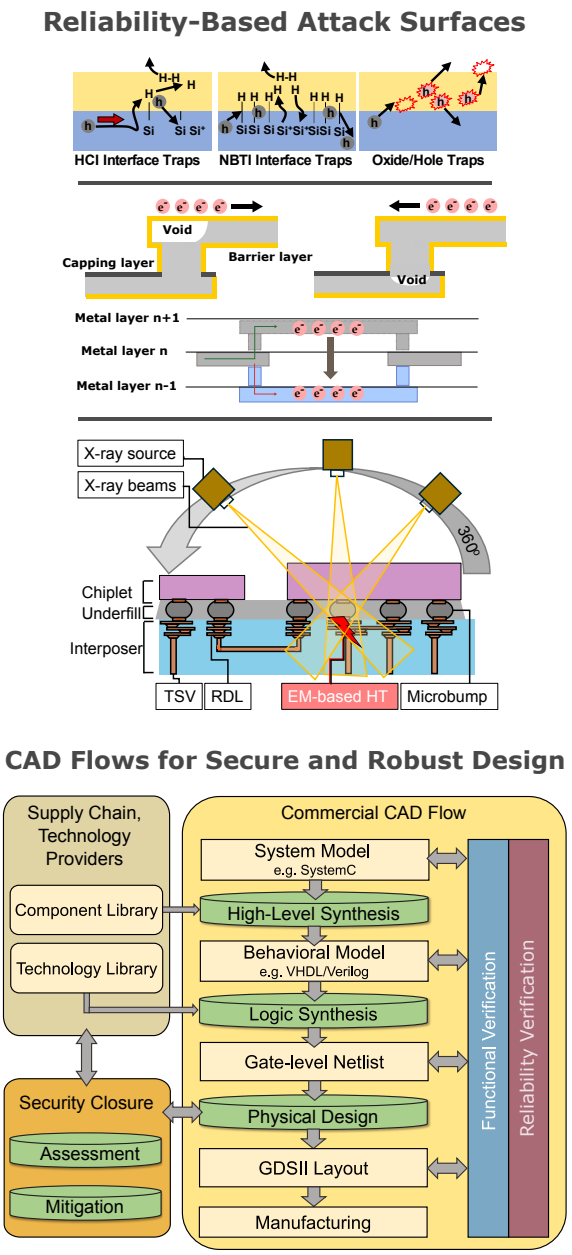

Figure 10: From reliability-based attack surfaces to CAD flows with reliability-aware security closure [55, 81].

To further evade detection, they proposed an advanced Trojan topology that utilizes center-hole cuts rather than edge modifications, preventing the characteristic dent shapes that otherwise would alert inspections at sensitive imaging angles. They also showed that such Trojans can remain hidden during parametric testing.

6.1.3 Transistor Aging. Beyond interconnects, the collaboration has addressed the security implications of transistor aging, including negative bias temperature instability (NBTI) and hot-carrier injection (HCI) [55]. Their research shows that, as circuits age, the dynamic power for different switching transitions becomes less differentiated in certain technology nodes, which can assist power side-channel attacks. This led to the call for aging-aware security closure, where logic synthesis utilizes fully characterized standard-cell libraries to synergistically optimize netlists against both physical degradation and information leakage.

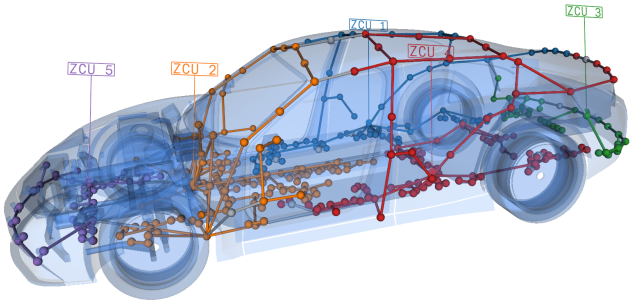

Figure 11: Wiring harness for a zonal architecture with five ZCUs [66]. Colors encode the mapping of components.

6.2 Flexible PCBs and Wiring Harnesses

In addition to EDA for ICs, Lienig's group has also developed algorithms and software tools for larger electronic systems. One example is the development of a design flow based entirely on open-source tools for modeling flexible printed circuits (FPCs) in a bent state [2]. Modeling the mechanical stress impact on electrical performance in these bent states requires coupled multi-physics simulations; thus, the developed workflow automates the generation of ready-to-use meshes for external FEM simulators.

Furthermore, the group has addressed the design of automotive wiring harnesses. Driven by the automotive industry's transition from domain-based to zonal architectures, early planning of the wiring harness has become increasingly critical. Here, algorithmic concepts from IC physical design were adapted to determine the optimal number and location of zone control units (ZCUs). In this framework, components are assigned to zones and ZCUs are positioned by solving a location covering problem, while the actual routing is modeled as a multi-commodity flow problem. Solving these formulations using integer linear programming (ILP) yields fast and optimal results [66], as illustrated by the generated zonal architecture in Figure 11.

6.3 Emerging Technologies

Beyond the optimization of standard technologies, Lienig's group also investigates physical design methodologies for emerging nanotechnologies, with some of those works outlined next.

6.3.1 Ising Machines. Recent efforts for design optimization include photonic ICs. Simulation and EDA expertise are applied and transferred to the photonic domain, aimed particularly at the development of silicon-based coherent Ising machines (CIM) [78]. CIMs use a network of degenerate optical parametric oscillators to solve optimization problems faster than classical computers based on the *von Neumann* architecture. The working principle of CIMs is based on a quantum-like behavior of the Ising spins modeled by

the oscillators. The adiabatic process of finding the ground state that represents the problem's solution is particularly temperature-sensitive, especially when using silicon-on-insulator waveguides. Hence, a strong focus on thermal analysis is important for the group's work in this emerging domain [12].

6.3.2 Reconfigurable Nanotechnologies. Reconfigurable field-effect transistors (RFETs) are based on ambipolar nanotechnologies, allowing for runtime reconfiguration of circuit functions and offering low area and power overheads compared to conventional CMOS. However, standard physical synthesis flows yield sub-optimal results for RFETs because they ignore the additional program gate terminal required for reconfiguration. To address this, Lienig's group developed a dedicated synthesis flow for RFET-based circuits [39]. This approach optimizes three specific aspects: (1) the design of optimized layouts for reconfigurable gates, (2) the use of special driver cells for the reconfigurable portions of the circuit, and (3) the optimized placement of these parts in separate power domains.

6.3.3 Carbon Nanotubes for Thermal Management. In the domain of high-density nano-scale systems, thermal management is a critical bottleneck. As power densities rise, traditional vertical interconnects (copper vias) often fail to provide sufficient heat dissipation through low-conductivity substrate layers. Lienig's group has explored carbon nanotubes (CNTs), which possess thermal conductivity exceeding that of metallic materials. They introduced a hierarchical modeling approach for CNT-based composites [14], which combines micromechanical models with macroscopic simulations. This allows designers to accurately evaluate the thermal behavior of CNT-filled vias, enabling the creation of "heat pipes" that diffusively transport thermal energy from hot device clusters to heat sinks, thereby ensuring reliability in dense 3D stacks.

6.4 Further Research at the Institute

Jens Lienig's emphasis on all aspects of electronic systems design extends to the broader research profile of the institute. Apart from CAD and EDA, there is also a strong focus on precision engineering [31, 32, 77]. For example, medical devices such as insulin pens and blood pumps [71] have been developed. Furthermore, research addresses energy management methods applied to electrical systems of large aircraft [75], innovative LED lighting systems and spectrometers [13, 80], etc. Specific reliability issues have been analyzed and simulated for different electronic/electromechanical systems, e.g., the wear behavior of linear stepper motors, ball-screw drives and ventilation systems [9, 11, 79]. Researchers of the institute hold a large number of patents across these fields [70].

7 Education and Textbooks

Beyond his research contributions, Jens Lienig has also had a profound impact on education for physical design and electronic systems engineering. Upon his appointment to TU Dresden and becoming director of the IFTE, he reformed the institute's curriculum by augmenting the prior focus on mechanical design with electronic design education. The teaching program now covers the development of electronic devices from undergraduate level through advanced elective courses. This includes both the theoretical foundation and practical classes where students gain experience in CAD for mechanical systems, PCB design, and IC layout synthesis. A particular emphasis is placed on design methodology, supported by specialized courses on optimization, FEM simulation, and EDA.

Multiple textbooks authored by Lienig and colleagues bridge the gap between theory and industrial reality, a philosophy also central to TU Dresden's educational model. *VLSI Physical Design: From Graph Partitioning to Timing Closure* [21] serves as a standard reference for the field, detailing the algorithmic foundations necessary to solve modern EDA challenges. Recognizing the need for a holistic systems view, Lienig also co-authored *Fundamentals of Electronic Systems Design* [49] and the German version *Elektronische Gerätetechnik* [50], which expand the curriculum to cover the entire lifecycle, from component protection to reliability analysis. Building upon his group's extensive work in the field, their recent book *Fundamentals of Electromigration-Aware Integrated Circuit Design* [54] provides the rigorous physics-based treatment of interconnect reliability required to understand modern failure mechanisms. Additionally, his co-authored books on layout design, available in both English [56] and German [57], educate on modern design methodologies for PCBs and ICs. One must also acknowledge the German monographs covering his research on evolutionary algorithms [41] and routing strategies [40], as well as his early German textbooks on layout synthesis [47] and 3D system design [52].

8 Summary

Jens Lienig's career offers a compelling narrative for advancing physical design. His early work on evolutionary algorithms (Section 2) demonstrated that nature-inspired heuristics could solve routing complexities where deterministic methods struggled. As technology nodes shrank and physical effects became dominant, his focus shifted toward reliability by construction. His contributions to constraint-driven analog design (Section 3) and electromigration-aware routing (Section 4) provided the industry with the methodologies needed to handle the "physical" reality of physical design – ensuring that chips do not fail due to current density, heat, or stress. Furthermore, his foresight in addressing system-level challenges is evident in his work on 3D integration (Section 5) and his recent efforts in emerging topics such as hardware security (Section 6). Perhaps most importantly, he has ensured that this knowledge is not confined to research papers. Through his leadership at IFTE and his comprehensive textbooks (Section 7), he has codified the principles of robust physical design for future generations.

As Jens Lienig receives the ISPD 2026 Lifetime Achievement Award, we celebrate a career that has made the physical design landscape significantly more reliable and robust. By grounding algorithmic abstraction in industrial reality and championing this philosophy through research, education, and mentorship, he has established a legacy for the community as it navigates the challenges of the post-Moore era.

Acknowledgments

This work was supported in part by the Deutsche Forschungsgemeinschaft (DFG, German Research Foundation) under Grant Nos. 525041614, 466323332, and 20046032, as well as by the German Federal Ministry of Research, Technology and Space (BMFTR) under Grant Nos. 16ME0473, 16ME0484, and 16ME0781.

References

[1] T. Ajayi, V. A. Chhabria, M. Fogaça, S. Hashemi, A. Hosny, A. B. Kahng, M. Kim, J. Lee, U. Mallappa, M. Neseem, G. Pradipta, S. Reda, M. Saligane, S. S. Sapatnekar, C. Sechen, M. Shalan, W. Swartz, L. Wang, Z. Wang, M. Woo, and B. Xu. 2019. Toward an Open-Source Digital Flow: First Learnings from the OpenROAD Project. In *Proc. IEEE/ACM Des. Autom. Conf. (DAC)*. doi:10.1145/3316781.3326334

[2] N. Arnold, A. Krinke, M. Dietrich, and J. Lienig. 2025. An Open-Source Tool for FEM Modeling of Bent Flexible Circuits. *IEEE J. Flex. Electron.* 4, 8 (2025), 333–341. doi:10.1109/JFLEX.2025.3594658

[3] S. Bigalke and J. Lienig. 2016. Load-Aware Redundant Via Insertion for Electromigration Avoidance. In *Proc. ACM Int. Symp. Phys. Des. (ISPD)*. 99–106. doi:10.1145/2872334.2872355

[4] S. Bigalke and J. Lienig. 2020. Avoidance vs. repair: New approaches to increasing electromigration robustness in VLSI routing. *Elsevier Integration* 75 (2020), 189–198. doi:10.1016/j.vlsi.2020.04.009

[5] R. Fischbach, T. Horst, and J. Lienig. 2019. A Graph-Based Model of Micro-Transfer Printing for Cost-Optimized Heterogeneous 2.5D Systems. In *Proc. IEEE Int. 3D Sys. Integr. Conf. (3DIC)*. 1–6. doi:10.1109/3DIC48104.2019.9058886

[6] R. Fischbach, J. Knechtel, and J. Lienig. 2013. Utilizing 2D and 3D rectilinear blocks for efficient IP reuse and floorplanning of 3D-integrated systems. In *Proc. ACM Int. Symp. Phys. Des. (ISPD)* (Stateline, Nevada, USA). 11–16. doi:10.1145/2451916.2451921

[7] R. Fischbach, J. Lienig, and T. Meister. 2009. From 3D circuit technologies and data structures to interconnect prediction. In *Proc. IEEE Int. Worksh. Sys. Interconn. Pred. (SLIP)* (San Francisco, CA, USA). 77–84. doi:10.1145/1572471.1572485

[8] R. Fischbach, J. Lienig, and M. Thiele. 2010. Solution space investigation and comparison of modern data structures for heterogeneous 3D designs. In *Proc. IEEE Int. 3D Sys. Integr. Conf. (3DIC)*. 1–8. doi:10.1109/3DIC.2010.5751476

[9] S. Fraulob, M. Thiele, S. Marth, and J. Gundermann. 2015. Wear and Aging Simulation of Electrical-Mechanical Systems. In *Proc. 18th ITI Symp.* 435–443.

[10] GlobalFoundries PDK Authors. 2022. *GF180 PDK*. https://github.com/google/gf180mcu-pdk

[11] J. Gundermann, M. Thiele, S. Fraulob, S. Walther, K. Todtermuschke, and U. Schnabel. 2017. The Embedded Simulation via FMI and its Application to the Simulation of Lifetime Tests Including Wear. In *Proc. 12th Int. Modelica Conf.* 541–545. doi:10.3384/ecp17132541

[12] M. He, M. Thiele, A. Shetewy, J. Lienig, and K. Jamshidi. 2025. Performance Analysis of Silicon Microring Resonators using Newtonian Cooling and Non-Fourier Heat Conduction Models. In *Proc. Asia Commun. Photonics Conf. (ACP)*.

[13] T. Heimpold, F. Reifegerste, S. Drechsel, and J. Lienig. 2018. LED for hyperspectral imaging – a new selection method. *Biomedical Engineering / Biomedizinische Technik* 63, 5 (2018), 529–535. doi:doi:10.1515/bmt-2017-0120

[14] J. Hertwig, H. Neubert, and J. Lienig. 2012. A Hierarchical Modeling Approach of Thermal Vias Using CNT-Based Composites. In *Bio and Nano Packaging Techniques for Electron Devices*, G. Gerlach and K.-J. Wolter (Eds.). Springer, New York, 601–620. doi:10.1007/978-3-642-28522-6_29

[15] IHP PDK authors. 2023. *IHP Open Source PDK*. https://github.com/IHP-GmbH/IHP-Open-PDK/

[16] G. Jerke and J. Lienig. 2002. Hierarchical current density verification for electromigration analysis in arbitrarily shaped metallization patterns of analog circuits. In *Proc. EDAA/ACM/IEEE Des. Autom. Test Eur. (DATE)*. 464–469. doi:10.1109/DATE.2002.998314

[17] G. Jerke and J. Lienig. 2004. Hierarchical current-density verification in arbitrarily shaped metallization patterns of analog circuits. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst. (TCAD)* 23, 1 (2004), 80–90. doi:10.1109/TCAD.2003.819899

[18] G. Jerke and J. Lienig. 2009. Constraint-driven Design — The Next Step Towards Analog Design Automation. In *Proc. ACM Int. Symp. Phys. Des. (ISPD)* (San Diego, California, USA). 75–82. doi:10.1145/1514932.1514952

[19] G. Jerke and J. Lienig. 2010. Early-stage determination of current-density criticality in interconnects. In *Proc. IEEE Int. Symp. Qual. Elec. Des. (ISQED)*. 667–674. doi:10.1109/ISQED.2010.5450505

[20] G. Jerke, J. Lienig, and J. Scheible. 2004. Reliability-driven layout decompaction for electromigration failure avoidance in complex mixed-signal IC designs. In *Proc. IEEE/ACM Des. Autom. Conf. (DAC)*. 181–184. doi:10.1145/996566.996618

[21] A. B. Kahng, J. Lienig, I. L. Markov, and J. Hu. 2022. *VLSI Physical Design: From Graph Partitioning to Timing Closure* (2nd ed.). Springer. doi:10.1007/978-3-030-96415-3

[22] J. Knechtel and J. Lienig. 2016. Physical Design Automation for 3D Chip Stacks – Challenges and Solutions. In *Proc. ACM Int. Symp. Phys. Des. (ISPD)*. 3–10. doi:10.1145/2872334.2872335

[23] J. Knechtel, J. Lienig, and I. Elfadel. 2017. Multi-Objective 3D Floorplanning with Integrated Voltage Assignment. *ACM Trans. Des. Autom. Electron. Syst. (TODAES)* 23, 2 (2017), 22. doi:10.1145/3149817

[24] J. Knechtel, I. L. Markov, and J. Lienig. 2011. Assembling 2D blocks into 3D chips. In *Proc. ACM Int. Symp. Phys. Des. (ISPD)*. 81–88. doi:10.1145/1960397.1960417

[25] J. Knechtel, I. L. Markov, and J. Lienig. 2012. Assembling 2-D blocks into 3-D chips. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst. (TCAD)* 31, 2 (2012), 228–241. doi:10.1109/TCAD.2011.2174640

[26] J. Knechtel, I. L. Markov, J. Lienig, and M. Thiele. 2012. Multiobjective Optimization of Deadspace, a Critical Resource for 3D-IC Integration. In *Proc. IEEE/ACM Int. Conf. Comput.-Aided Des. (ICCAD)*. 705–712. doi:10.1145/2429384.2429538

[27] J. Knechtel, O. Sinanoglu, I. A. M. Elfadel, J. Lienig, and C. C. N. Sze. 2017. Large-Scale 3D Chips: Challenges and Solutions for Design Automation, Testing, and Trustworthy Integration. *IPSJ Trans. Syst. LSI Des. Methodol. (T-SLDM)* 10 (2017), 45–62. doi:10.2197/ipsjtsldm.10.45

[28] J. Knechtel, E. F. Y. Young, and J. Lienig. 2014. Structural Planning of 3D-IC Interconnects by Block Alignment. In *Proc. IEEE/ACM Asia S. Pac. Des. Autom. Conf. (ASPDAC)*. 53–60. doi:10.1109/ASPDAC.2014.6742866

[29] J. Knechtel, E. F. Y. Young, and J. Lienig. 2015. Planning Massive Interconnects in 3-D Chips. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst. (TCAD)* 34, 11 (2015), 1808–1821. doi:10.1109/TCAD.2015.2432141

[30] M. Köfferlein and contributors. 2023. *KLayout*. https://www.klayout.de/

[31] W. Krause. 2018. *Grundlagen der Konstruktion* (10th ed.). Carl Hanser Verlag, München.

[32] W. Krause. 2018. *Konstruktionselemente der Feinmechanik* (4th ed.). Carl Hanser Verlag, München.

[33] A. Krinke, R. Fischbach, and J. Lienig. 2024. Layout Verification Using Open-Source Software. In *Proc. ACM Int. Symp. Phys. Des. (ISPD)* (Taipei, Taiwan). 137–142. doi:10.1145/3626184.3635289

[34] A. Krinke, T. Horst, G. Gläser, M. Grabmann, T. Markus, B. Prautsch, U. Hatnik, and J. Lienig. 2019. From Constraints to Tape-Out: Towards a Continuous AMS Design Flow. In *Proc. Int. Symp. Des. Diag. Elec. Circ. & Sys. (DDECS)*. 1–10. doi:10.1109/DDECS.2019.8724669

[35] A. Krinke, G. Jerke, and J. Lienig. 2013. Adaptive data model for efficient constraint handling in AMS IC design. In *Proc. IEEE Int. Conf. Electron. Circuits Syst. (ICECS)*. 285–288. doi:10.1109/ICECS.2013.6815410

[36] A. Krinke, G. Jerke, and J. Lienig. 2015. Constraint Propagation Methods for Robust IC Design. In *ZuE 2015; 8. GMM/ITG/GI-Symposium Reliability by Design*. 1–8.

[37] A. Krinke and J. Lienig. 2011. An ontology for constraints in custom IC design. In *Proc. Eur. Conf. Circ. Theory and Design (ECCTD)*. 338–340. doi:10.1109/ECCTD.2011.6043355

[38] A. Krinke, M. Mittag, G. Jerke, and J. Lienig. 2013. Extended constraint management for analog and mixed-signal IC design. In *Proc. Eur. Conf. Circ. Theory and Design (ECCTD)*. 1–4. doi:10.1109/ECCTD.2013.6662319

[39] A. Krinke, S. Rai, A. Kumar, and J. Lienig. 2021. Exploring Physical Synthesis for Circuits Based on Emerging Reconfigurable Nanotechnologies. In *Proc. IEEE/ACM Int. Conf. Comput.-Aided Des. (ICCAD)*. Munich. doi:10.1109/ICCAD51958.2021.9643439

[40] J. Lienig. 1991. *Ein Verdrahtungssystem für den rechnergestützten Layoutentwurf von Multichipträgern*. Number 119 in Fortschritt-Berichte VDI. VDI-Verlag, Düsseldorf.

[41] J. Lienig. 1996. *Anwendung evolutionärer Algorithmen für den rechnergestützten Entwurf des Schaltungslayouts*. Number 228 in Fortschritt-Berichte VDI. VDI-Verlag, Düsseldorf.

[42] J. Lienig. 1996. A Parallel Genetic Algorithm for Two Detailed Routing Problems. In *Proc. IEEE Int. Symp. Circ. Sys. (ISCAS)*. Atlanta, Georgia, 508–511. doi:10.1109/ISCAS.1996.541764

[43] J. Lienig. 1997. Channel and Switchbox Routing With Minimized Crosstalk — A Parallel Genetic Algorithm Approach. In *Proc. 10th Int. Conf. VLSI Des.* Hyderabad, India, 27–31. doi:10.1109/ICVD.1997.567993

[44] J. Lienig. 1997. A Parallel Genetic Algorithm for Performance-Driven VLSI Routing. *IEEE Trans. Evol. Comput.* 1, 1 (1997), 29–39. doi:10.1109/4235.585891

[45] J. Lienig. 2006. Introduction to Electromigration-Aware Physical Design. In *Proc. ACM Int. Symp. Phys. Des. (ISPD)*. 39–46. doi:10.1145/1123008.1123019

[46] J. Lienig. 2013. Electromigration and Its Impact on Physical Design in Future Technologies. In *Proc. ACM Int. Symp. Phys. Des. (ISPD)*. 33–40. doi:10.1145/2451916.2451925

[47] J. Lienig. 2016. *Layoutsynthese elektronischer Schaltungen: Grundlegende Algorithmen für die Entwurfsautomatisierung* (2nd ed.). Springer Vieweg, Berlin, Heidelberg. doi:10.1007/978-3-662-49815-6

[48] J. Lienig and H. Brandt. 1994. An Evolutionary Algorithm for the Routing of Multi-Chip Modules. In *Parallel Problem Solving from Nature (LNCS, Vol. 866)*. 588–597. doi:10.1007/3-540-58484-6_300

[49] J. Lienig and H. Brümmer. 2017. *Fundamentals of Electronic Systems Design*. Springer. doi:10.1007/978-3-319-55840-0

[50] J. Lienig and H. Brümmer. 2024. *Elektronische Gerätetechnik: Grundlagen des Entwickelns elektronischer Baugruppen und Geräte* (2nd ed.). Springer Vieweg, Berlin. doi:10.1007/978-3-662-68708-6

[51] J. Lienig and J. P. Cohoon. 1996. Genetic Algorithms Applied to the Physical Design of VLSI Circuits: A Survey. In *Parallel Problem Solving from Nature*, H.-M. Voigt, W. Ebeling, I. Rechenberg, and H.-P. Schwefel (Eds.). LNCS, Vol. 1141. Springer, Berlin, 839–848. doi:10.1007/3-540-61723-X_1054

[52] J. Lienig and M. Dietrich (Eds.). 2012. *Entwurf integrierter 3D-Systeme der Elektronik*. Springer Vieweg, Berlin, Heidelberg. doi:10.1007/978-3-642-30572-6

[53] J. Lienig and G. Jerke. 2003. Current-driven wire planning for electromigration avoidance in analog circuits. In *Proc. IEEE/ACM Asia S. Pac. Des. Autom. Conf. (ASPDAC)*. 783–788. doi:10.1109/ASPDAC.2003.1195125

[54] J. Lienig, S. Rothe, and M. Thiele. 2025. *Fundamentals of Electromigration-Aware Integrated Circuit Design* (2nd ed.). Springer, Cham, Switzerland. doi:10.1007/978-3-031-80023-8

[55] J. Lienig, S. Rothe, M. Thiele, N. Rangarajan, M. Ashraf, M. Nabeel, H. Amrouch, O. Sinanoglu, and J. Knechtel. 2021. Toward Security Closure in the Face of Reliability Effects. In *Proc. IEEE/ACM Int. Conf. Comput.-Aided Des. (ICCAD)*. 1–9. doi:10.1109/ICCAD51958.2021.9643447

[56] J. Lienig and J. Scheible. 2020. *Fundamentals of Layout Design for Electronic Circuits*. Springer. doi:10.1007/978-3-030-39284-0

[57] J. Lienig and J. Scheible. 2023. *Grundlagen des Layoutentwurfs elektronischer Schaltungen*. Springer Vieweg, Cham. doi:10.1007/978-3-031-15768-4

[58] J. Lienig and M. Thiele. 2018. The Pressing Need for Electromigration-Aware Physical Design. In *Proc. ACM Int. Symp. Phys. Des. (ISPD)* (Monterey, California, USA). 144–151. doi:10.1145/3177540.3177560

[59] J. Lienig and K. Thulasiraman. 1994. GASBOR: A Genetic Algorithm for Switchbox Routing in Integrated Circuits. In *Proc. AI'94 Worksh. Evol. Comput.* Armidale, 199–212.

[60] J. Lienig and K. Thulasiraman. 1996. GASBOR: A Genetic Algorithm Approach for Solving the Switchbox Routing Problem. *J. Circuits Syst. Comput.* 6, 4 (1996), 359–373. doi:10.1142/S021812669600025X

[61] Magic authors. 2020. *Magic*. http://opencircuitdesign.com/magic/

[62] W. N. Martin, J. Lienig, and J. P. Cohoon. 1997. Island (Migration) Models: Evolutionary Algorithms Based on Punctuated Equilibria. In *Handbook of Evolutionary Computation*. Oxford University Press, New York, NY, C6.3:1–C6.3:16.

[63] T. Meister, J. Lienig, and G. Thomke. 2008. Novel Pin Assignment Algorithms for Components with Very High Pin Counts. In *Proc. EDAA/ACM/IEEE Des. Autom. Test Eur. (DATE)*. 837–842. doi:10.1109/DATE.2008.4484778

[64] T. Meister, J. Lienig, and G. Thomke. 2010. Universal Methodology to Handle Differential Pairs during Pin Assignment. In *Proc. IEEE Int. Conf. VLSI (VLSI-SoC)*, C. Piguet, R. Reis, and D. Soudris (Eds.). Springer, Berlin, Heidelberg, 22–42. doi:10.1007/978-3-642-12267-5_2

[65] T. Meister, J. Lienig, and G. Thomke. 2011. Interface Optimization for Improved Routability in Chip-Package-Board Co-Design. In *Proc. IEEE Int. Worksh. Sys. Interconn. Pred. (SLIP)*. 1–8. doi:10.1109/SLIP.2011.6135430

[66] P. Näke, F. Stein, A. Krinke, and J. Lienig. 2025. Efficient Architecture Evaluation and Generation of Automotive Wiring Harnesses. In *Proc. IEEE Transp. Electrif. Conf. Expo Asia-Pac. (ITEC Asia-Pacific)* (Singapore).

[67] G.-J. Nam, C. Sze, and M. Yildiz. 2008. The ISPD global routing benchmark suite. In *Proc. ACM Int. Symp. Phys. Des. (ISPD)* (Portland, Oregon, USA). 156–159. doi:10.1145/1353629.1353663

[68] OpenRoad Team. 2023. *OpenROAD Website*. https://theopenroadproject.org/

[69] S. Osmolovskyi, J. Knechtel, I. L. Markov, and J. Lienig. 2018. Optimal Die Placement for Interposer-Based 3D ICs. In *Proc. IEEE/ACM Asia S. Pac. Des. Autom. Conf. (ASPDAC)*. 513–520. doi:10.1109/ASPDAC.2018.8297375

[70] Patents IFTE [n. d.]. Patents IFTE. https://www.ifte.de/infos/publikationen/patente/index.html

[71] S. Pech, R. Richter, and J. Lienig. 2020. Peristaltic Pump with Continuous Flow and Programmable Flow Pulsation. In *Proc. IEEE 8th Electron. Syst.-Integr. Tech. Conf. (ESTC)*. 1–5. doi:10.1109/ESTC48849.2020.9229731

[72] S. Rothe and J. Lienig. 2023. Combined Modeling of Electromigration, Thermal and Stress Migration in AC Interconnect Lines. In *Proc. ACM Int. Symp. Phys. Des. (ISPD)* (Virtual Event, USA). 107–114. doi:10.1145/3569052.3571880

[73] S. Rothe, J. Lienig, and S. S. Sapatnekar. 2025. Temperature-aware stress-based migration modeling in IC design: Moving from theory to practice. *AEU - Int. J. Electron. Commun.* 200 (2025), 155909. doi:10.1016/j.aeue.2025.155909

[74] J. Scheible and J. Lienig. 2015. Automation of Analog IC Layout: Challenges and Solutions. In *Proc. ACM Int. Symp. Phys. Des. (ISPD)* (Monterey, California, USA). 33–40. doi:10.1145/2717764.2717781

[75] D. Schlabe and J. Lienig. 2012. Energy management of aircraft electrical systems - state of the art and further directions. In *Electrical Systems for Aircraft, Railway and Ship Propulsion*. 1–6. doi:10.1109/ESARS.2012.6387387

[76] SkyWater PDK Authors. 2020. *SKY130 PDK*. https://skywater-pdk.readthedocs.io/

[77] C. Steinmann, K. Wrede, J. Schirmer, and J. Lienig. 2025. Integration of Geometric Tolerance Analysis in System Simulations via Functional Mock-up Units. In *Proc. 16th Int. Modelica and FMI Conf.* doi:10.3384/ecp218765

[78] M. Thiele, J. Lienig, M. He, and K. Jamshidi. 2025. Thermal Modeling of Silicon Photonic Waveguides. In *Proc. 21st Int. Conf. Synth. Model. Anal. Simul. Methods Appl. Circ. Des. (SMACD)*. 1–4. doi:10.1109/SMACD65553.2025.11092117

[79] S. Walther, K. Todtermuschke, U. Schnabel, and M. Thiele. 2016. Embedded Simulation via FMI for Wear and Tear Processes. In *Proc. ESI SimulationX User Forum*. 126–132.

[80] K. Wichler and F. Reifegerste. 2025. Enhancing Spectral Resolution by Fusing Data from Multiple Commercial Sensors. *J. Sci. Tech. Lighting* advpub (2025), IEIJ240000668. doi:10.2150/jstl.IEIJ240000668

[81] K. Yahyaei, S. Rothe, M. V. D. Naina, A. Roy, M. S. M. Khan, O. Sinanoglu, J. Lienig, J. Knechtel, and N. Asadizanjani. 2025. Lurking in the Shadows: Challenges for X-Ray Inspection to Uncover Electromigration-Based Hardware Trojans in Advanced Packaging. In *Proc. IEEE Int. Conf. Phys. Assur. Insp. Electr. (PAINE)*.